1995

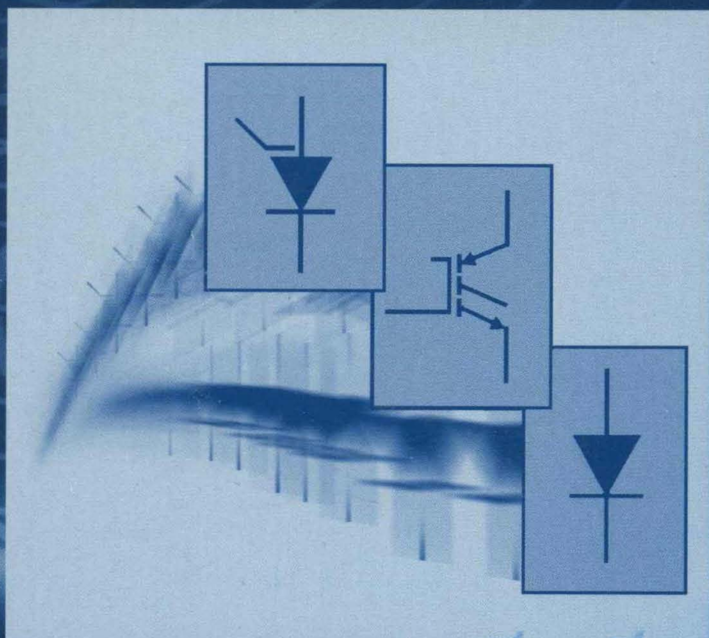
MCT/IGBTs/Diodes

HARRIS

DB 309.1

MCT/IGBTs/Diodes

1995



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TEL: 1-800-442-7747
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FAX: (407) 729-5321

ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

EUROPEAN HEADQUARTERS
Harris Semiconductor
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Printed in U.S.A., 7/1995

MCT/IGBT/DIODES PRODUCTS

Harris Semiconductor is a pioneer in developing and producing Discrete Power products for the most demanding commercial applications in this world and beyond.

This databook fully describes Harris Semiconductor's line of MOS Controlled Thyristors (MCTs), Insulated Gate Bipolar Transistors (IGBTs) and Power Diodes/Rectifiers. It includes a complete set of datasheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program. A New AnswerFAX section has bee added which allows customers to request the very latest datasheets and have them delivered immediately to their own fax machine. A detailed listing of product Packaging dimensions provides a wide variety of information at your fingertips.

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HARRIS
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MCT/IGBT/DIODES

FOR COMMERCIAL APPLICATIONS

* Product Selection Guide located at the beginning of section.

TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

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ITALY	Milano	39-2-262-0761
JAPAN	Tokyo	81-3-3265-7571
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MCT/IGBT/DIODES 1

GENERAL INFORMATION

Alpha Numeric Product Index

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

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Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

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Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

MOS CONTROLLED THYRISTORS

PREVIEW PRODUCTS

ULTRAFAST DUAL DIODES

ULTRAFAST SINGLE DIODES

Product Index by Family (Continued)

Product Index by Family (Continued)

MCT Ordering Information

MCT - V - 35 - P - 60 - F - 1 - D

HARRIS MCT — MCT

PACKAGE — V
- V: 5 Lead TO-247
- A: MO-093AA
- G: TO-247

CONTINUOUS CURRENT RATING — 35
- T_C = 90°C or T_C = 115°C

POLARITY — P
- P: P Channel
- N: N Channel

VOLTAGE RATING /10 — 60
- 60 = 600V
- 100 = 1000V

MAX: FALL TIME AT T_J = 125°C — F
- A: ≤100ns
- B: ≤200ns
- C: ≤500ns
- D: ≤750ns
- E: ≤1μs
- F: ≤2μs

1: First Generation

OPTIONS — D
- D: Integral Reverse Diode

IGBT Ordering Information

HGT - G - 12 - N - 60 - D - 1 - D

HARRIS IGBT — HGT

PACKAGE — G
- A: 5 Lead TO-218
- P: 3 Lead TO-220
- G: 3 Lead TO-247
- H: 3 Lead TO-218
- D: TO-251/TO-252 D-Pak
- V: 5 Lead TO-247

CONTINUOUS CURRENT RATING — 12
- T_C = +90°C or 25°C

POLARITY — N
- P: P Channel
- N: N Channel

VOLTAGE RATING /10 — 60
- 50 = 500V
- 60 = 600V
- 100 = 1000V

MAX. FALL TIME AT T_J = +125°C — D
- A: ≤100ns
- B: ≤200ns
- C: ≤500ns
- D: ≤750ns
- E: ≤1μs
- F: ≤2μs
- G: ≤5μs

Generation — 1
- 1: First Generation
- 2: Second Generation
- 3: Third Generation

OPTIONS — D
- L: Logic Level Gate
- D: Integral Reverse Diode
- S: Surface Mount
- C: Current Sense
- V: Voltage Clamping

Rectifier Ordering Information

R X R X XX XX XX

RECOVERY SPEED
- U: Ultrafast
- H: Hyperfast

PACKAGE
- P: 2 and 3 Lead TO-220
- G: 2 and 3 Lead TO-247
- H: 2 and 3 Lead TO-218
- D: 2 and 3 Lead TO-251/TO-252
- U: 1 Lead TO-218

CONTINUOUS CURRENT RATING
- 8 = 8A
- 50 = 50A
- 150 = 150A

VOLTAGE RATING /10
- 20 = 200V
- 60 = 600V
- 100 = 1000V

OPTIONS
- CC: Common Cathode DUAL
- S: Surface Mount

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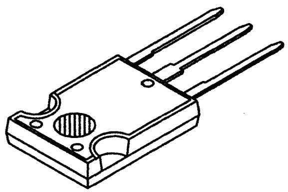
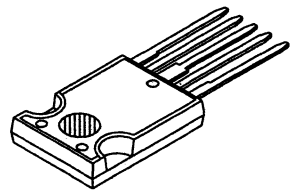
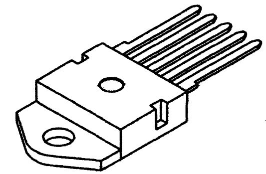
MCT/IGBT/DIODES 2

MOS CONTROLLED THYRISTORS

MOS CONTROLLED THYRISTOR PRODUCT MATRIX

	 TO-247	 5 LEAD TO-247			 MO-093AA		
	MCTG35P60F1	MCTV35P60F1D	MCTV75P60E1	MCTV75P100E1	MCTA65P100F1	MCTA75P60E1	UNITS
V_{DRM}	600	600	600	1000	1000	600	V
I_{K90}	35†	35†	75	65	65	75	A
I_{KM}	50	50	120	100	100	120	A
V_{TM} at I_{K90}	1.35††	1.35††	1.3	1.4	1.4	1.3	V
t_{FI}	1.4	1.4	1.4	1.9	1.9	1.4	µs
Diode V_F	-	1.4††	-	-	-	-	V
Diode t_{RR}	-	600	-	-	-	-	ns

† I_{K115}; Continuous Cathode Current rated at $T_C = +115^oC$.
†† Measured at I_{K115}.

HARRIS SEMICONDUCTOR

MCTG35P60F1

April 1995

35A, 600V
P-Type MOS Controlled Thyristor (MCT)

Features

- 35A, -600V
- V_{TM} = -1.3V(Maximum) at I = 35A and +150°C
- 800A Surge Current Capability
- 800A/µs di/dt Capability
- MOS Insulated Gate Control
- 50A Gate Turn-Off Capability at +150°C

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150°C with active switching.

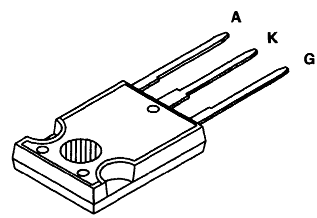
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MCTG35P60F1	TO-247	M35P60F1

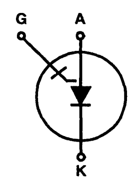
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MCTG35P60F1	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-600	V
Peak Reverse Voltage	V_{RRM}	+5	V
Continuous Cathode Current (See Figure 2)			
T_C = +25°C (Package Limited)	I_{K25}	60	A
T_C = +115°C	I_{K115}	35	A
Non-Repetitive Peak Cathode Current (Note 1)	I_{KSM}	800	A
Peak Controllable Current (See Figure 10)	I_{KC}	50	A
Gate-Anode Voltage (Continuous)	V_{GA}	±20	V
Gate-Anode Voltage (Peak)	V_{GAM}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	800	A/µs
Maximum Power Dissipation	P_T	178	W
Linear Derating Factor		1.43	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	°C

NOTE:

1. Maximum Pulse Width of 250µs (Half Sine) Assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -600V, V_{GA} = +18V	T_C = +150°C	-	-	1.5	mA
			T_C = +25°C	-	-	50	µA
Peak Reverse Blocking Current	I_{RRM}	V_{KA} = +5V V_{GA} = +18V	T_C = +150°C	-	-	2	mA
			T_C = +25°C	-	-	50	µA
On-State Voltage	V_{TM}	$I_K = I_{K115}$, V_{GA} = -10V	T_C = +150°C	-	-	1.35	V
			T_C = +25°C	-	-	1.4	V
Gate-Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		-	-	100	nA
Input Capacitance	C_{ISS}	V_{KA} = -20V, T_J = +25°C V_{GA} = +18V		-	5	-	nF
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 200µH, $I_K = I_{K115}$ R_G = 1Ω, V_{GA} = +18V, -7V T_J = +125°C V_{KA} = -300V		-	140	-	ns
Current Rise Time	t_{RI}			-	180	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	640	-	ns
Current Fall Time	t_{FI}			-	1.1	1.4	µs
Turn-off Energy	E_{OFF}			-	5.6	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.6	0.7	°C/W

Typical Performance Curves

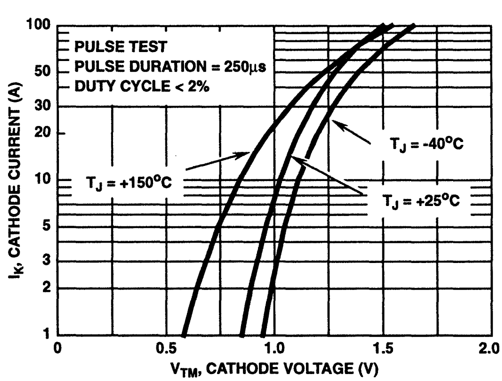


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

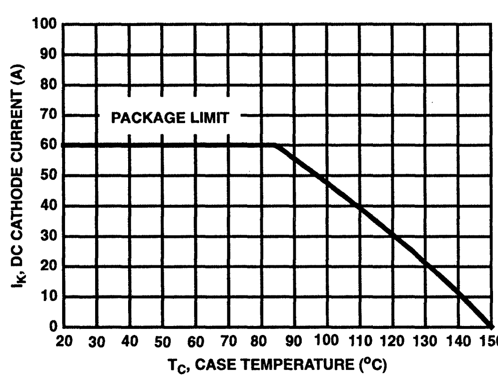


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

Typical Performance Curves (Continued)

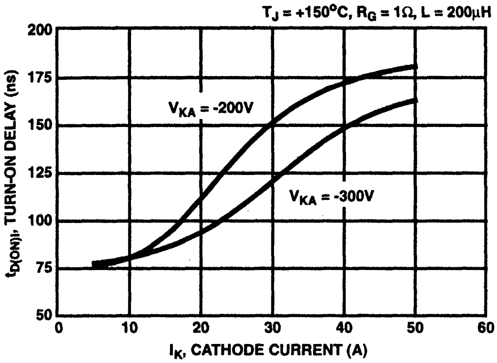


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

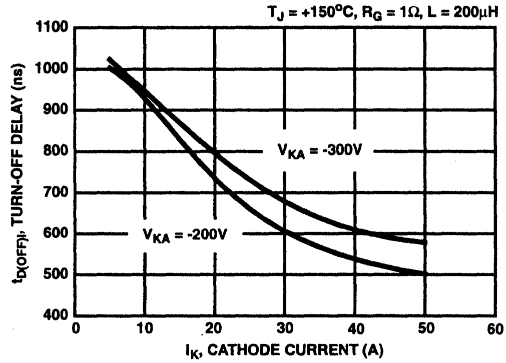


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

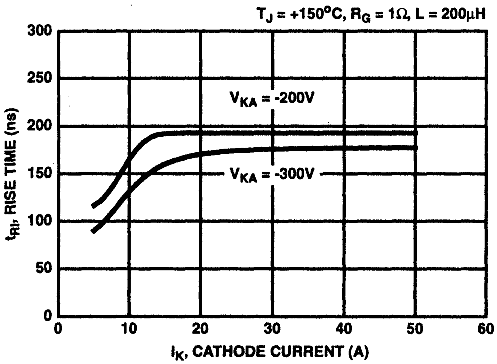


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

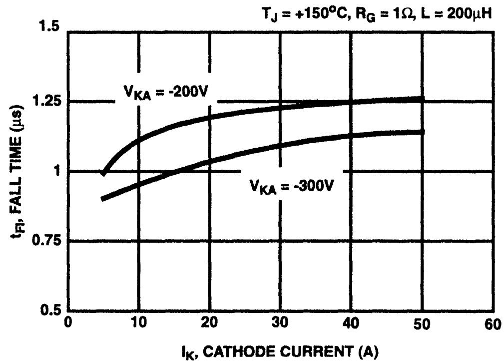


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

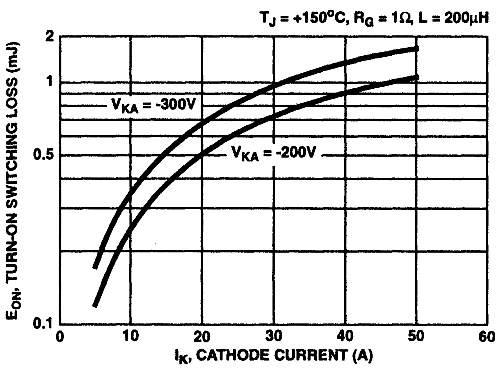


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

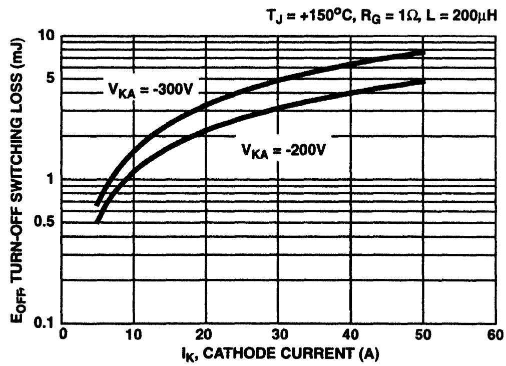


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

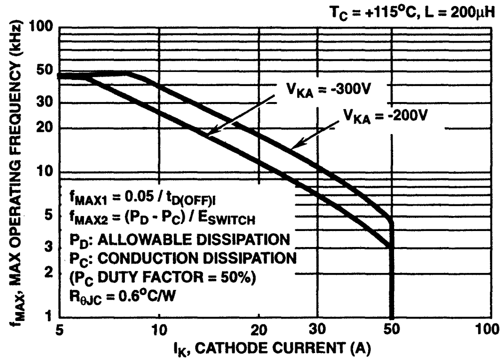


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

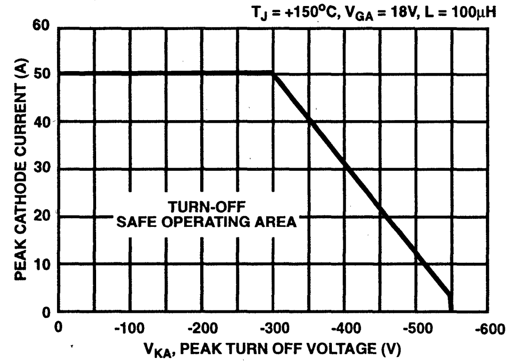


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

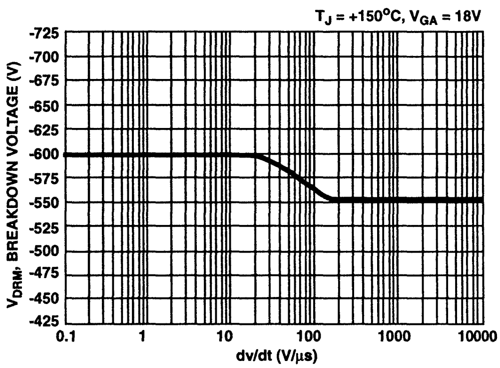


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

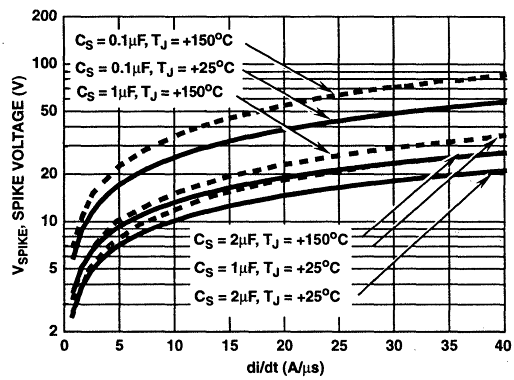


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figure 3 to Figure 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is lower at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON}+E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by PC = ($V_{AK} \bullet I_{AK}$) / (duty factor/100). E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{AK} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

Test Circuits

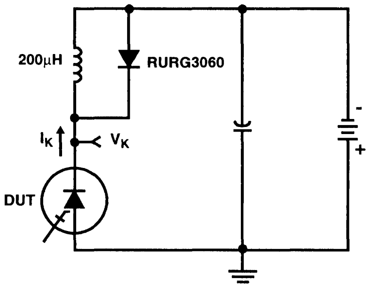


FIGURE 13. SWITCHING TEST CIRCUIT

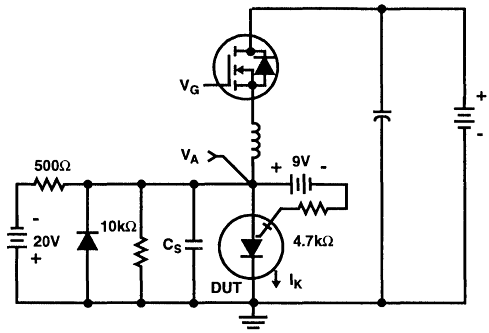


FIGURE 14. V_{SPIKE} TEST CIRCUIT

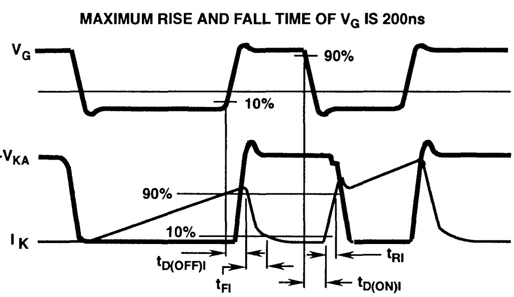


FIGURE 15. SWITCHING TEST WAVEFORMS

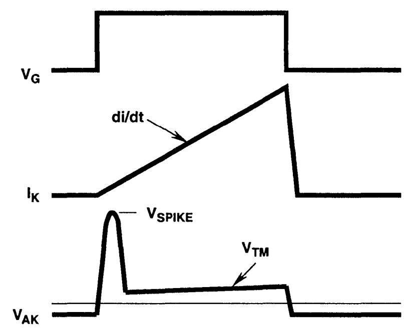


FIGURE 16. V_{SPIKE} TEST WAVEFORMS

Handling Precautions for MCTs

MOS Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORB LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating - Never exceed the gate-voltage rating of V_{GA}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR MCTV35P60F1D

35A, 600V P-Type MOS Controlled Thyristor (MCT) with Anti-Parallel Diode

March 1995

Features

- 35A, -600V
- V_{TM} = -1.35V (Max) at I = 35A and +150°C
- 800A Surge Current Capability
- 800A/μs di/dt Capability
- MOS Insulated Gate Control
- 50A Gate Turn-Off Capability at +150°C
- Anti-Parallel Diode

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications. The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150°C with active switching. This device features a discrete anti-parallel diode that shunts current around the MCT in the reverse direction without introducing carriers into the depletion region.

PACKAGING AVAILABILITY

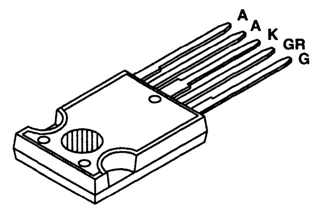
PART NUMBER	PACKAGE	BRAND
MCTV35P60F1D	TO-247	M35P60F1D

NOTE: When ordering, use the entire part number.

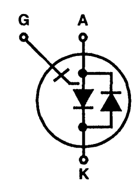
Formerly developmental type TA9789 (MCT) and TA49054 (diode).

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MCTV35P60F1D	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-600	V
Continuous Cathode Current (See Figure 2)			
T_C = +25°C (Package Limited)	I_{K25}	60	A
T_C = +90°C	I_{K115}	35	A
Non-repetitive Peak Cathode Current (Note 1)	I_{KSM}	800	A
Peak Controllable Current (See Figure 10)	I_{KC}	50	A
Gate-Anode Voltage (Continuous)	V_{GA1}	±20	V
Gate-Anode Voltage (Peak)	V_{GAM}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	800	A/μs
Maximum Power Dissipation	P_T	178	W
Linear Derating Factor		1.43	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	°C

NOTE: 1. Maximum Pulse Width of 250μs (Half Sine) Assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -600V	T_C = +150°C	-	-	5	mA
		V_{GA} = +18V	T_C = +25°C	-	-	200	µA
On-State Voltage	V_{TM}	$I_K = I_{K115}$	T_C = +150°C	-	-	1.35	V
		V_{GA} = -7V	T_C = +25°C	-	-	1.4	V
Gate-Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		-	-	100	nA
Input Capacitance	C_{ISS}	V_{KA} = -20V, T_J = +25°C V_{GA} = +18V		-	5	-	nF
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 200µH, $I_K = I_{K115}$ R_G = 1Ω, V_{GA} = +18V, -7V T_J = +125°C V_{KA} = -300V		-	140	-	ns
Current Rise Time	t_{RI}			-	180	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	640	-	ns
Current Fall Time	t_{FI}			-	1.1	1.4	µs
Turn-Off Energy	E_{OFF}			-	5.6	-	mJ
Thermal Resistance (MCT)	$R_{\theta JC}$			-	.6	.7	°C/W
Thermal Resistance (Diode)	$R_{\theta JC}$			-	1.1	1.2	°C/W
Diode Forward Voltage	V_{KA}	I_{KA} = 35A		-	-	1.4	V
Diode Reverse Recovery Time	t_{RR}	I_{KA} = 35A, di/dt = 100A/µs		-	-	600	ns

Typical Performance Curves

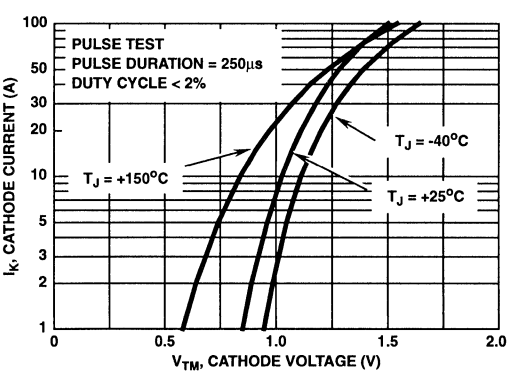


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

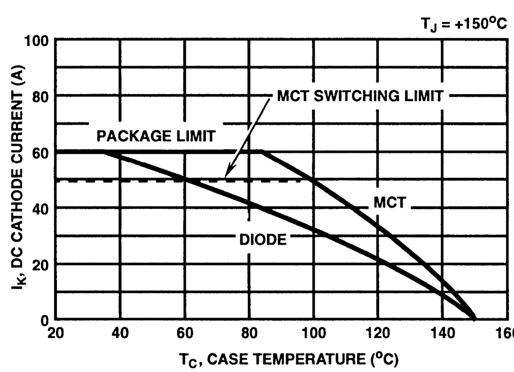


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

2

MCTs

Typical Performance Curves (Continued)

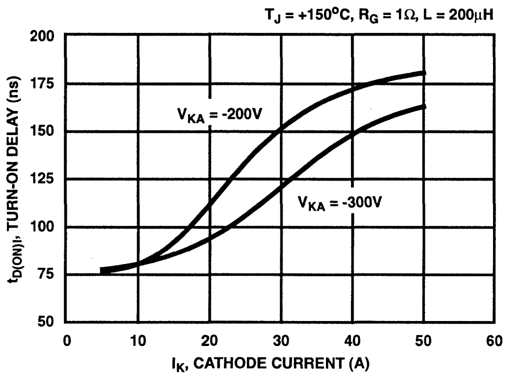


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

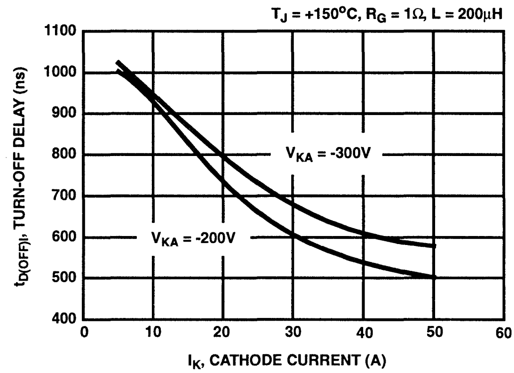


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

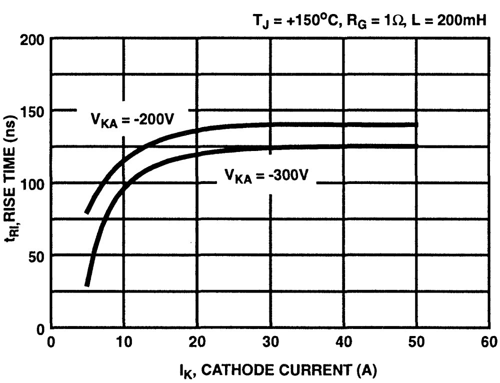


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

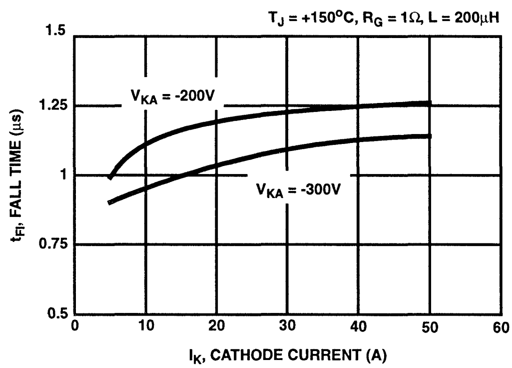


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

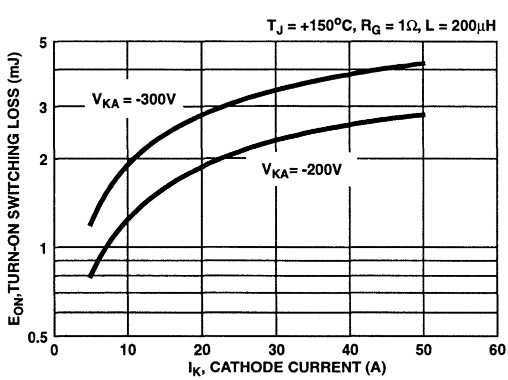


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

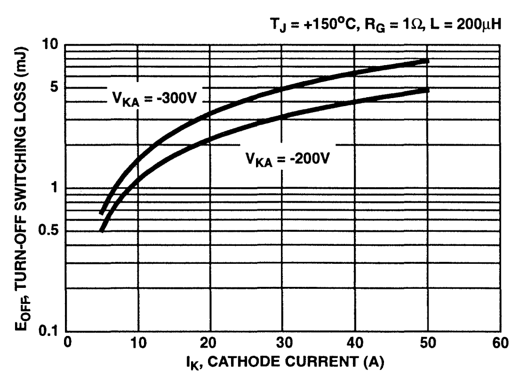


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

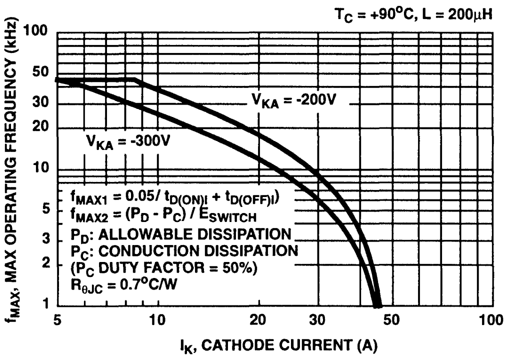


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

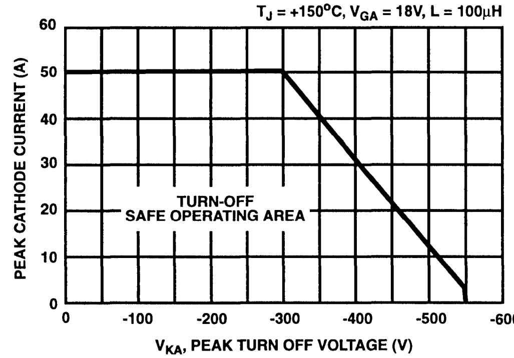


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

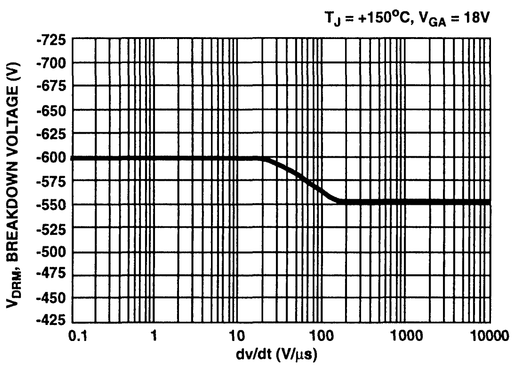


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

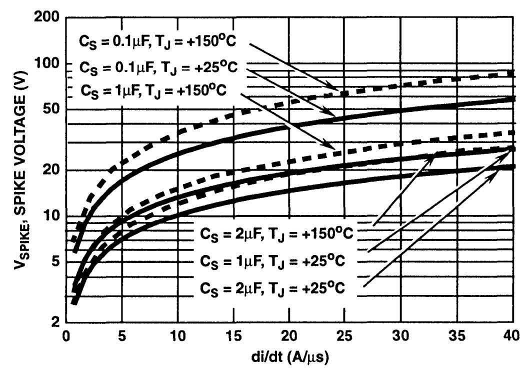


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

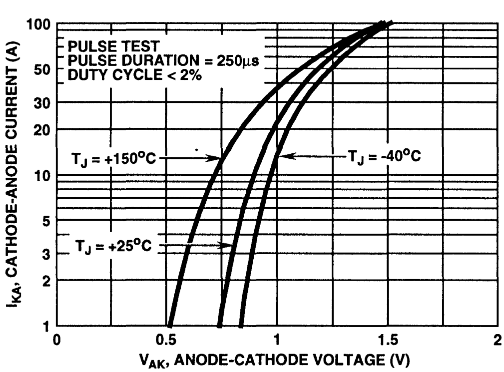


FIGURE 13. DIODE CATHODE-ANODE CURRENT vs VOLTAGE (TYPICAL)

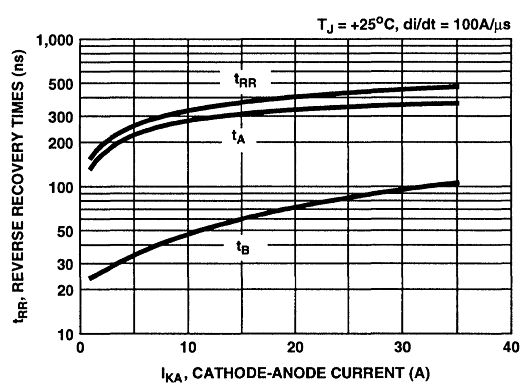


FIGURE 14. DIODE REVERSE RECOVERY TIMES vs CURRENT (TYPICAL)

Test Circuits

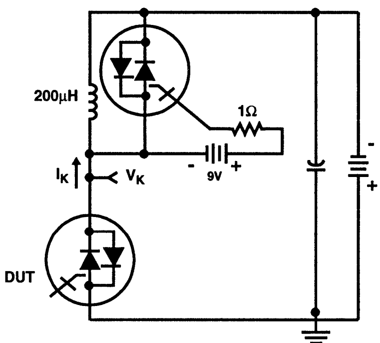


FIGURE 15. SWITCHING TEST CIRCUIT

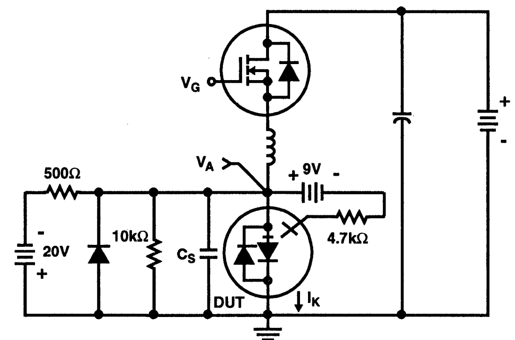


FIGURE 16. V_{SPIKE} TEST CIRCUIT

MAXIMUM RISE AND FALL TIME OF V_G IS 200ns

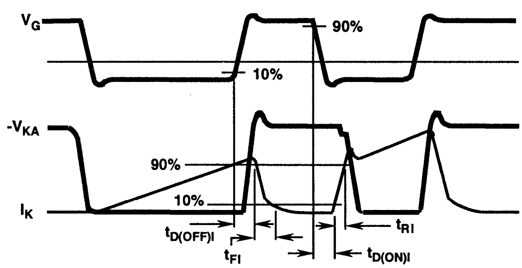


FIGURE 17. SWITCHING TEST WAVEFORMS

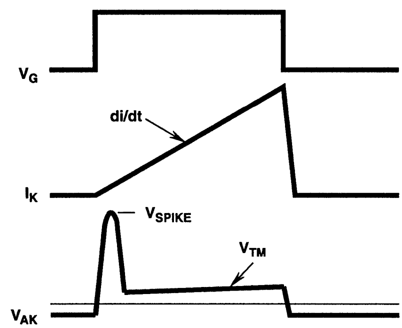


FIGURE 18. V_{SPIKE} TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is lower at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON} + E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 9) and the conduction losses (P_C) are approximated by $P_C = (V_{AK} \bullet I_{AK}) / (\text{duty factor}/100)$. E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{AK} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

MCTV65P100F1, MCTA65P100F1

65A, 1000V P-Type MOS Controlled Thyristor (MCT)

April 1995

Features

- 65A, -1000V
- $V_{TM} \leq$ -1.4V at I = 65A and +150°C
- 2000A Surge Current Capability
- 2000A/µs di/dt Capability
- MOS Insulated Gate Control
- 100A Gate Turn-Off Capability at +150°C

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive voltage control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150°C with active switching.

PACKAGING AVAILABILITY

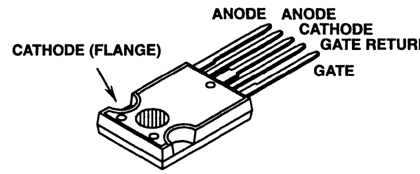
PART NUMBER	PACKAGE	BRAND
MCTV65P100F1	TO-247	M65P100F1
MCTA65P100F1	MO-093AA	M65P100F1

NOTE: When ordering, use the entire part number.

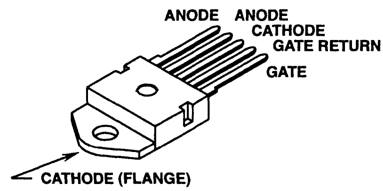
Formerly TA9900.

Package

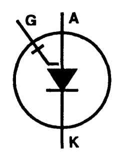
JEDEC STYLE TO-247



JEDEC MO-093AA (5-LEAD TO-218)



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MCTV65P100F1 MCTA65P100F1	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-1000	V
Peak Reverse Voltage	V_{RRM}	+5	V
Continuous Cathode Current (See Figure 2)			
T_C = +25°C (Package Limited)	I_{K25}	85	A
T_C = +90°C	I_{K90}	65	A
Non-Repetitive Peak Cathode Current (Note 1)	I_{TSM}	2000	A
Peak Controllable Current (See Figure 10)	I_{TC}	100	A
Gate-Anode Voltage (Continuous)	V_{GA}	±20	V
Gate-Anode Voltage (Peak)	V_{GA}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	2000	A/µs
Maximum Power Dissipation	P_T	208	W
Linear Derating Factor		1.67	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	°C

NOTE:

1. Maximum Pulse Width of 200µs (Half Sine) Assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3516.3**

Electrical Specifications $T_C = +25^oC$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	$V_{KA} = -1000V$, $V_{GA} = +18V$	$T_C = +150^oC$	-	-	3	mA
			$T_C = +25^oC$	-	-	100	μA
Peak Reverse Blocking Current	I_{RRM}	$V_{KA} = +5V$, $V_{GA} = +18V$	$T_C = +150^oC$	-	-	4	mA
			$T_C = +25^oC$	-	-	100	μA
On-State Voltage	V_{TM}	$I_K = I_{K90}$, $V_{GA} = -10V$	$T_C = +150^oC$	-	-	1.4	V
			$T_C = +25^oC$	-	-	1.5	V
Gate-Anode Leakage Current	I_{GAS}	$V_{GA} = \pm 20V$		-	-	200	nA
Input Capacitance	C_{ISS}	$V_{KA} = -20V$, $T_J = +25^oC$ $V_{GA} = +18V$		-	10	-	nF
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 200\mu H$, $I_K = I_{K90} = 65A$ $R_G = 1\Omega$, $V_{GA} = +18V, -7V$ $T_J = +125^oC$ $V_{KA} = -400V$		-	120	-	ns
Current Rise Time	t_{RI}			-	160	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	750	-	ns
Current Fall Time	t_{FI}			-	1.45	1.9	μs
Turn-Off Energy	E_{OFF}			-	18	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

Typical Performance Curves

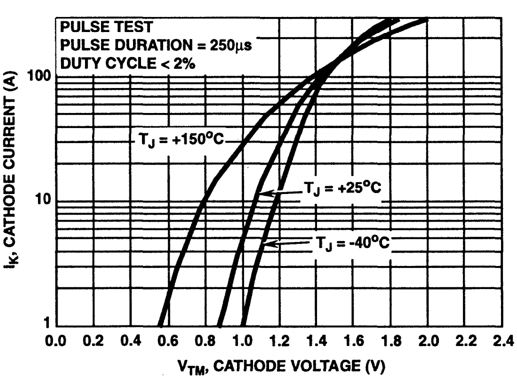


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

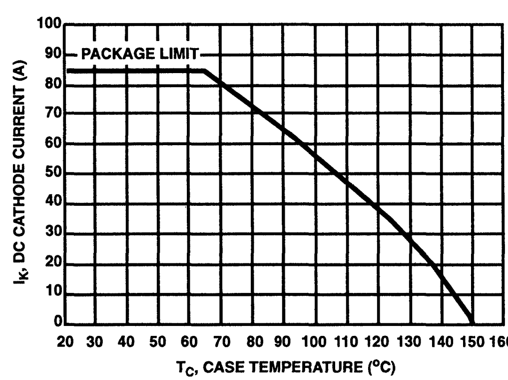


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

Typical Performance Curves (Continued)

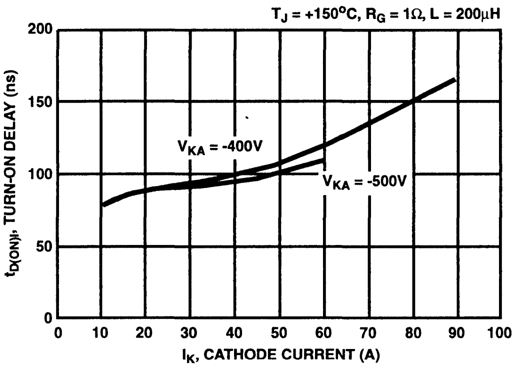


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

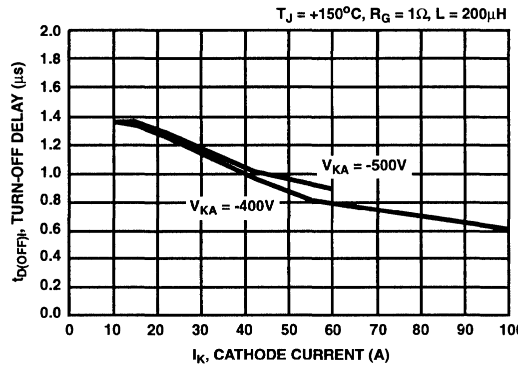


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

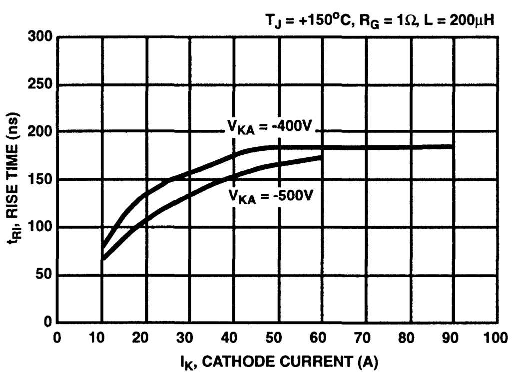


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

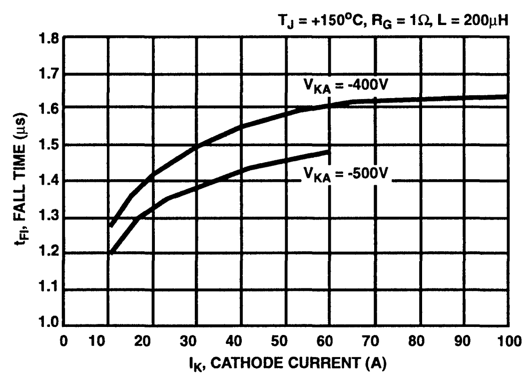


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

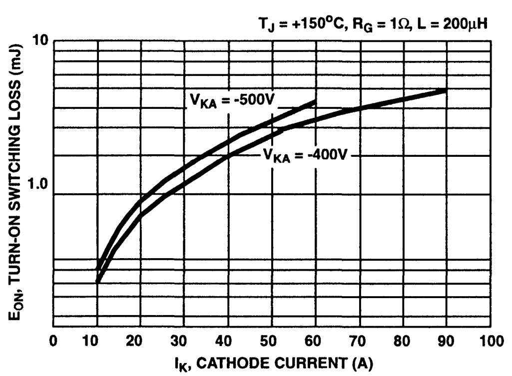


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

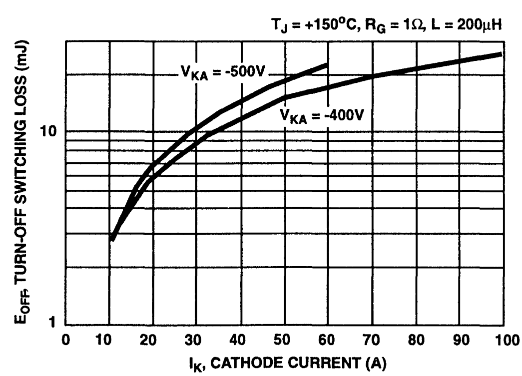


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

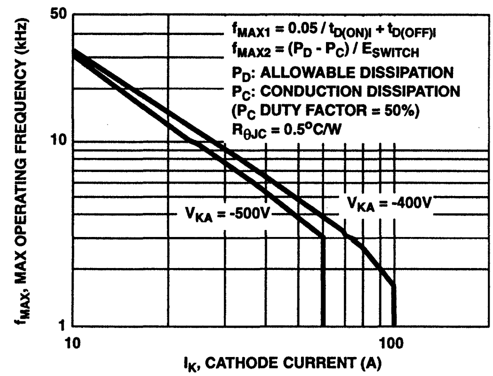


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

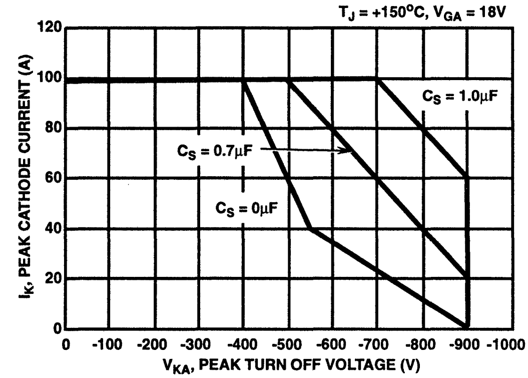


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

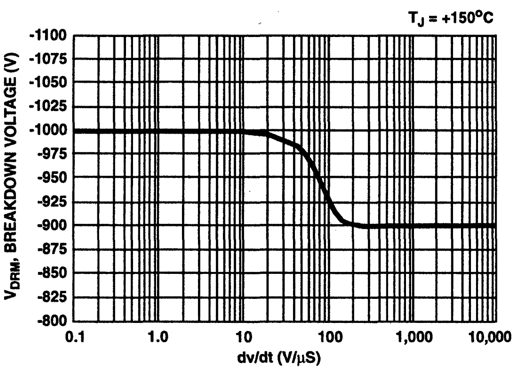


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

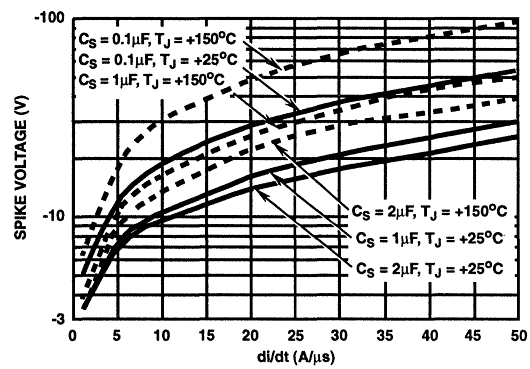


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_K) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value.

Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition. f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON}+E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used and the conduction losses (P_C) are approximated by $P_C = (V_{KA} \bullet I_K) / 2$. E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{KA} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

Test Circuits

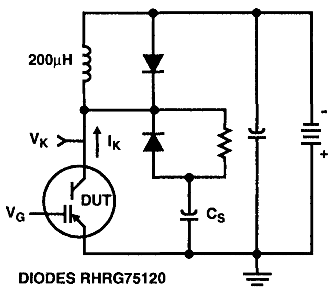


FIGURE 13. SWITCHING TEST CIRCUIT

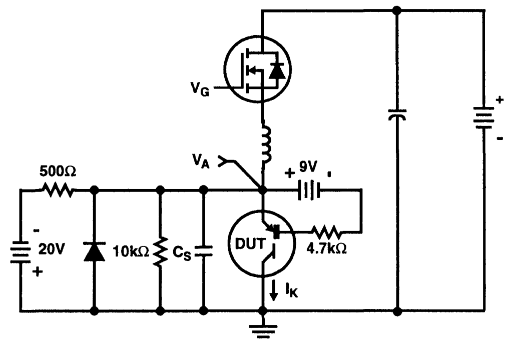


FIGURE 14. V_{SPIKE} TEST CIRCUIT

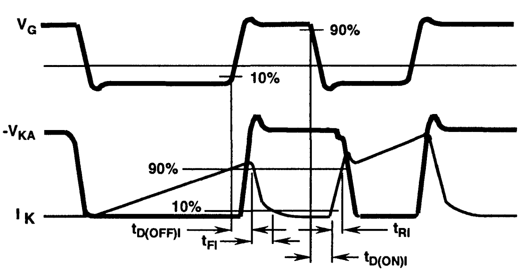


FIGURE 15. SWITCHING TEST WAVEFORMS

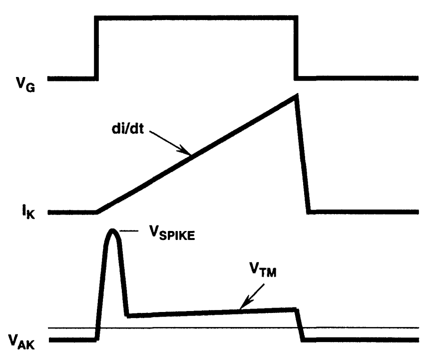


FIGURE 16. V_{SPIKE} TEST WAVEFORMS

Handling Precautions for MCT's

Mos Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †"ECCOSORB LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating - Never exceed the gate-voltage rating of V_{GA}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

2

MCTs

HARRIS SEMICONDUCTOR

MCTV75P60E1, MCTA75P60E1

75A, 600V
P-Type MOS Controlled Thyristor (MCT)

April 1995

Features

- 75A, -600V
- V_{TM} = -1.3V(Maximum) at I = 75A and +150°C
- 2000A Surge Current Capability
- 2000A/µs di/dt Capability
- MOS Insulated Gate Control
- 120A Gate Turn-Off Capability at +150°C

Description

The MCT is an MOS Controlled Thyristor designed for switching currents on and off by negative and positive pulsed control of an insulated MOS gate. It is designed for use in motor controls, inverters, line switches and other power switching applications.

The MCT is especially suited for resonant (zero voltage or zero current switching) applications. The SCR like forward drop greatly reduces conduction power loss.

MCTs allow the control of high power circuits with very small amounts of input energy. They feature the high peak current capability common to SCR type thyristors, and operate at junction temperatures up to +150°C with active switching.

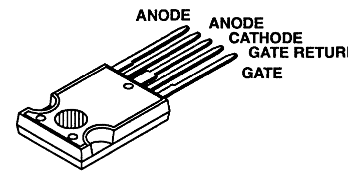
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MCTV75P60E1	TO-247	MV75P60E1
MCTA75P60E1	MO-093AA	MA75P60E1

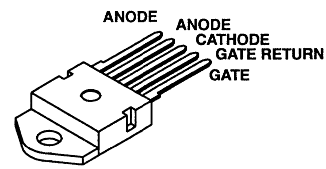
NOTE: When ordering, use the entire part number.

Package

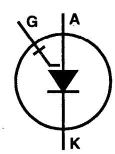
JEDEC STYLE TO-247 5-LEAD



JEDEC MO-093AA (5-LEAD TO-218)



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MCTV75P60E1 MCTA75P60E1	UNITS
Peak Off-State Voltage (See Figure 11)	V_{DRM}	-600	V
Peak Reverse Voltage	V_{RRM}	+5	V
Continuous Cathode Current (See Figure 2)			
T_C = +25°C (Package Limited)	I_{K25}	85	A
T_C = +90°C	I_{K90}	75	A
Non-Repetitive Peak Cathode Current (Note 1)	I_{KSM}	2000	A
Peak Controllable Current (See Figure 10)	I_{KC}	120	A
Gate-Anode Voltage (Continuous)	V_{GA}	±20	V
Gate-Anode Voltage (Peak)	V_{GAM}	±25	V
Rate of Change of Voltage	dv/dt	See Figure 11	
Rate of Change of Current	di/dt	2000	A/µs
Maximum Power Dissipation	P_T	208	W
Linear Derating Factor		1.67	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	260	°C

NOTE:

1. Maximum Pulse Width of 250µs (Half Sine) Assume T_J (Initial) = +90°C and T_J (Final) = T_J (Max) = +150°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_C = +25°C Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Peak Off-State Blocking Current	I_{DRM}	V_{KA} = -600V,	T_C = +150°C	-	-	3	mA
		V_{GA} = +18V	T_C = +25°C	-	-	100	μA
Peak Reverse Blocking Current	I_{RRM}	V_{KA} = +5V	T_C = +150°C	-	-	4	mA
		V_{GA} = +18V	T_C = +25°C	-	-	100	μA
On-State Voltage	V_{TM}	$I_K = I_{K90}$,	T_C = +150°C	-	-	1.3	V
		V_{GA} = -10V	T_C = +25°C	-	-	1.4	V
Gate-Anode Leakage Current	I_{GAS}	V_{GA} = ±20V		-	-	200	nA
Input capacitance	C_{ISS}	V_{KA} = -20V, T_J = +25°C V_{GA} = +18V		-	10	-	nF
Current Turn-on Delay Time	$t_{D(ON)I}$	L = 200μH, $I_K = I_{K90}$ R_G = 1Ω, V_{GA} = +18V, -7V T_J = +125°C V_{KA} = -300V		-	300	-	ns
Current Rise Time	t_{RI}			-	200	-	ns
Current Turn-off Delay Time	$t_{D(OFF)I}$			-	700	-	ns
Current Fall Time	t_{FI}			-	1.15	1.4	μs
Turn-off Energy	E_{OFF}			-	10	-	mJ
Thermal Resistance	$R_{θJC}$			-	.5	.6	°C/W

Typical Performance Curves

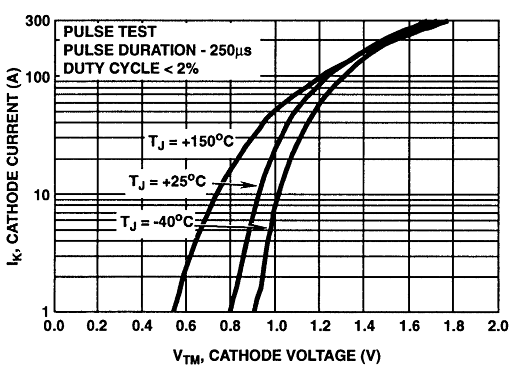


FIGURE 1. CATHODE CURRENT vs SATURATION VOLTAGE (TYPICAL)

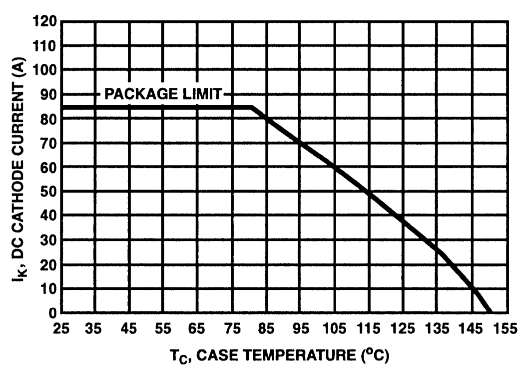


FIGURE 2. MAXIMUM CONTINUOUS CATHODE CURRENT

Typical Performance Curves (Continued)

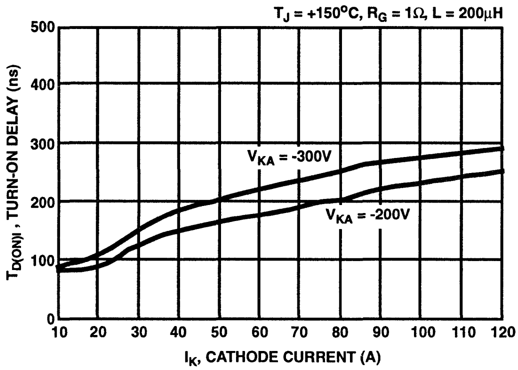


FIGURE 3. TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

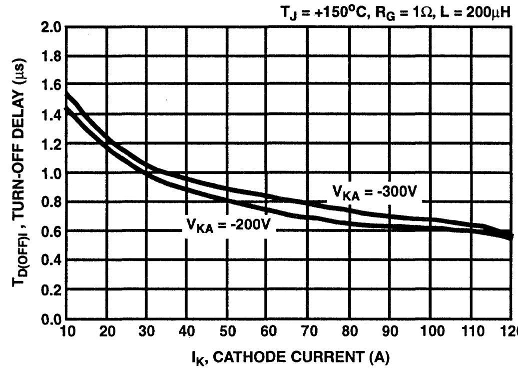


FIGURE 4. TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

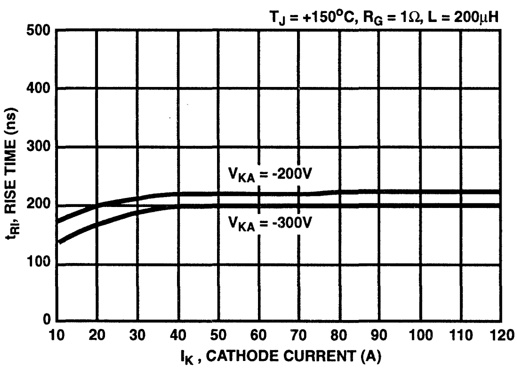


FIGURE 5. TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

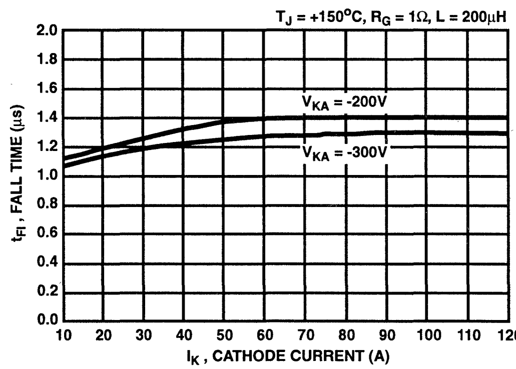


FIGURE 6. TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

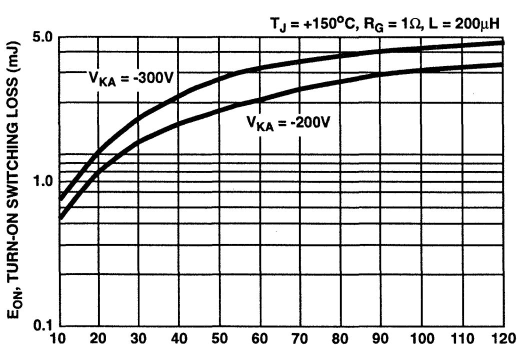


FIGURE 7. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

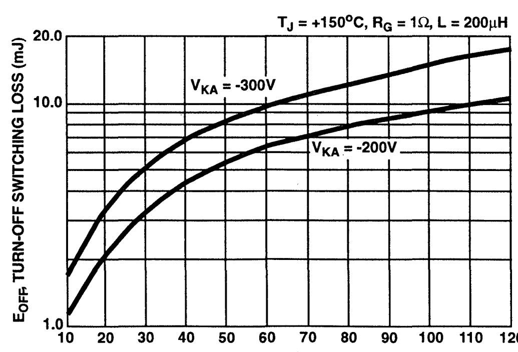


FIGURE 8. TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

Typical Performance Curves (Continued)

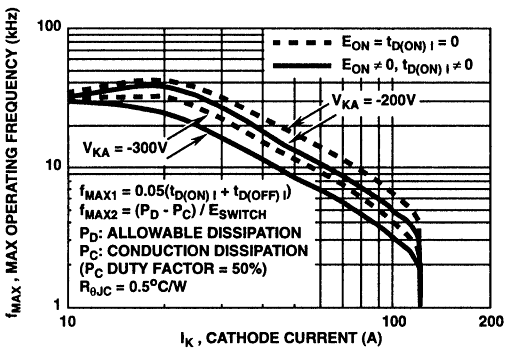


FIGURE 9. OPERATING FREQUENCY vs CATHODE CURRENT (TYPICAL)

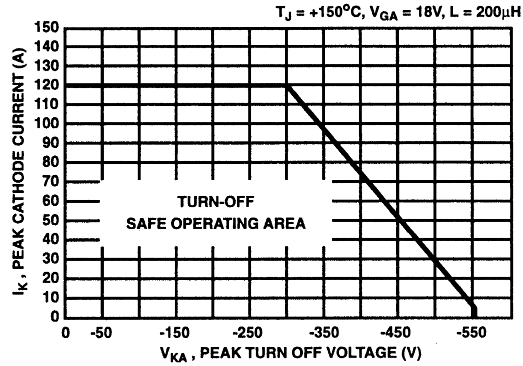


FIGURE 10. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

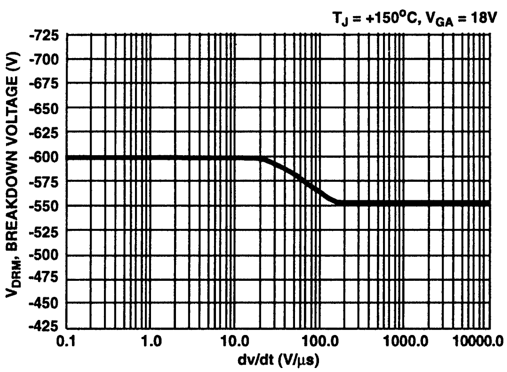


FIGURE 11. BLOCKING VOLTAGE vs dv/dt

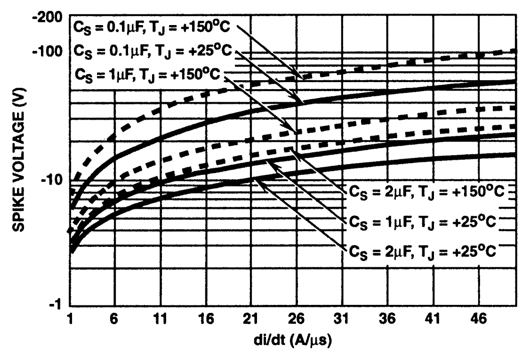


FIGURE 12. SPIKE VOLTAGE vs di/dt (TYPICAL)

Operating Frequency Information

Operating frequency information for a typical device (Figure 9) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 3 to 8. The operating frequency plot (Figure 9) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05 / (t_{D(ON)I} + t_{D(OFF)I})$. $t_{D(ON)I} + t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(ON)I}$ is defined as the 10% point of the leading edge of the input pulse and the point where the cathode current rises to 10% of its maximum value. $t_{D(OFF)I}$ is defined as the 90% point of the trailing edge of the input pulse and the point where the cathode current falls to 90% of its maximum value. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C) / (E_{ON} + E_{OFF})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{AK} \bullet I_{AK}) / (\text{duty factor}/100)$. E_{ON} is defined as the sum of the instantaneous power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals saturation voltage ($V_{AK} = V_{TM}$). E_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet (E_{ON} + E_{OFF})$. Because Turn-on switching losses can be greatly influenced by external circuit conditions and components, f_{MAX} curves are plotted both including and neglecting turn-on losses.

2

MCTs

Test Circuits

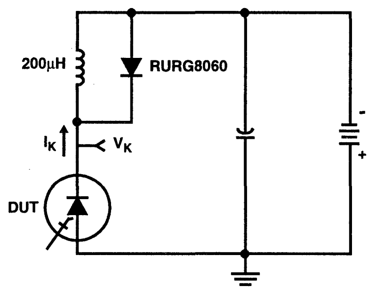


FIGURE 13. SWITCHING TEST CIRCUIT

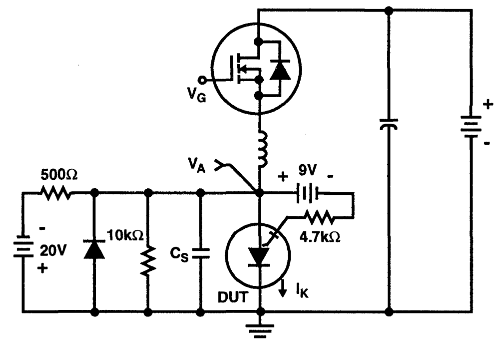


FIGURE 14. V_{SPIKE} TEST CIRCUIT

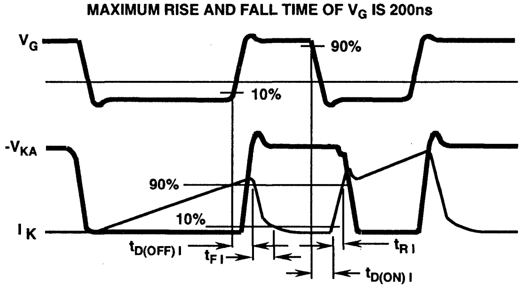


FIGURE 15. SWITCHING TEST WAVEFORMS

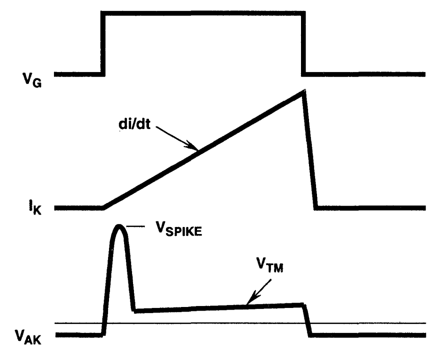


FIGURE 16. V_{SPIKE} TEST WAVEFORMS

Handling Precautions for MCT's

MOS Controlled Thyristors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. MCT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORB LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating - Never exceed the gate-voltage rating of V_{GA}. Exceeding the rated V_{GA} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. Gate Protection - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR

HIP2030

March 1995

30V MCT/IGBT Gate Driver

2

MCTs

Features

- ± Polarity Gate Drive
- High Output Voltage Swing 30V
- Peak Output Current 6.0A
- Fast Rise Time .... 200ns at 60,000pF
- Ability to Interface and Drive P-MCTs
- Programmable Minimum ON/OFF Time
- Gate Output Inhibit Latch
- 5V Reference .... Sinks Up to 30mA
- High Side Charge Pump
- 120kHz Operation. .... at 15,000pF

Applications

- Motor Controllers
- Uninterruptible Power Supplies
- Resonant Inverters
- Static Circuit Breakers
- Inverters
- Converters
- Arc Welders

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP2030IM	-40°C to +110°C	28 Lead PLCC

Description

The HIP2030 is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dv/dts). This device is optimized for driving 60nF of MOS gate capacitance at 30V peak to peak in less than 200ns. The half bridge gate driver is ideal for driving MOS Controlled Thyristor (MCT) and IGBT modules.

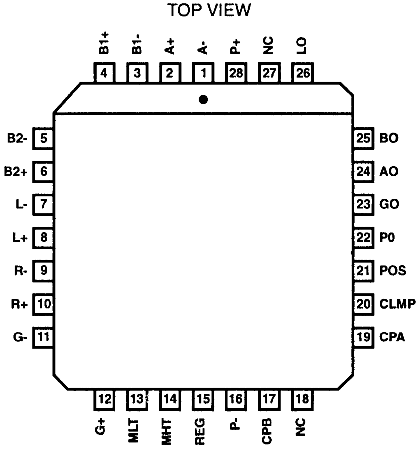
The architecture of the HIP2030 includes four comparator input channels, a 5V regulator, a 12V clamp, and a high side charge pump. The device provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (channels A and B) that can be used as monitors (temperature sensing), indicators (LEDs or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators.

The power requirements of the HIP2030 are low. The driver can be easily configured to operate in one of three power configurations. This allows the use of a small PCB mountable transformer or battery to provide isolated power to the driver chip.

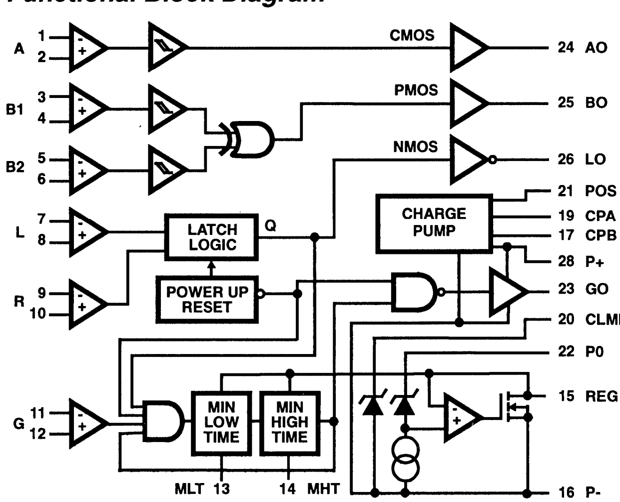
The HIP2030 supplies high output current drive to large capacitive loads and requires few external components to implement a wide variety of MOS gate driver circuits.

Pinout

HIP2030 (PLCC)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3691.2

Absolute Maximum Ratings

Gate Channel Supply Voltage, P+ to P- . . . . -0.5V to 32V
Logic Supply Voltage, P0 to P- . . . . 7V to 18V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) . . . . .(P-)-0.5 to (P+)+0.5

Thermal Information

Thermal Resistance θ_{JA}
PLCC Package . . . . 60°C/W
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions T_J = -40°C to +150°C Unless Otherwise Noted, All Voltages Referenced to P-

Gate Channel Supply Voltage, P+ to P- . . . . -0.5V to 30V
Logic Supply Voltage, P0 to P- . . . . 10V to 15V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) . . . . .(P-)+2V to (P0)+2V

Max Output Source Current, Channels A, B 10mA
Max Output Sink Current, Channels A, L. 10mA
Min Load Current, Reg to P- 2mA
(Required for Proper Chip Operation)
Max Load Current, Reg to P- 30mA

Static Electrical Specifications P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Reg to P- = 2mA. Full Temp T_J = -40°C to +150°C

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
I_{P0}	P0 Quiescent Supply Current		Full	-	3.5	5	mA
I_{P+}	P+ Quiescent Supply Current		+25°C	-	1	10	µA
			Full	-	-	250	µA
I_{QPOS}	POS Quiescent Supply Current	Osc Freq = 100kHz	Full	-	3	5	mA
BV_{P+}	P+ to P- Breakdown Voltage	I_{BV} = 100µA	Full	30	35	-	V
V_{REG}	Regulator Voltage, P0 to Reg	I_{REG} = 2mA	+25°C	4.4	5.2	6.0	V
			Full	4.0	-	6.5	V
R_{REG}	Regulator Impedance, P0 to Reg	I_{REG} = 10mA, 30mA	Full	3	8	17	Ω
V_{CLMP}	Clamp Voltage, CLMP to P-	I_{CLMP} = 15mA	Full	11	12.5	14	V
R_{CLMP}	Clamp Impedance, CLMP to P-	I_{CLMP} = 15mA, 30mA	Full	7	20	32	Ω
F_{CP}	Charge Pump Frequency		Full	-	200	-	kHz
D_{CP}	Charge Pump Duty Cycle		Full	-	50	-	%
VO_{CP}	Charge Pump V_{OUT}, P+ to P-	IP+ = 500µA	Full	28	28.5	29	V
VO_{CP}	Charge Pump V_{OUT}, P+ to P-	IP+ = 4mA	Full	26.5	27.5	28.5	V
I_{IN}	Comparator Input Leakage	VIN_{CMP} = VP0/2	Full	-	.01	1	µA
V_{OS}	Comparator Offset Voltage	V_{CM} = VP0/2	Full	-	10	50	mV
VCM	Comparator Common Mode Voltage Range		Full	(VP-)+2	-	VP0+2	V
RGO_{SRC}	GO Output RDS, Sourcing	I_{SRC} = 2A	+25°C	-	.6	1	Ω
			Full	-	-	1.5	Ω
RGO_{SNK}	GO Output RDS, Sinking	I_{SNK} = 2A	+25°C	-	2	3	Ω
			Full	-	-	4	Ω
RDS_{SRC}	AO, BO Output RDS, Sourcing	I_{SRC} = 10mA	+25°C	-	85	150	Ω
			Full	-	-	175	Ω
RDS_{SNK}	AO, LO Output RDS, Sinking	I_{SNK} = 10mA	+25°C	-	75	125	Ω
			Full	-	-	150	Ω

Dynamic Electrical Specifications P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Ref to P- = 2mA. Full Temp T_J = -40°C to +150°C

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
TH_{MIN}	Min GO Output Hi Duration	C_{LOAD} = 20pF	Full	600	1100	1600	ns
TL_{MIN}	Min GO Output Lo Duration	C_{LOAD} = 20pF	Full	200	750	1500	ns
TP_{LHAB}	Prop Delay, Lo - Hi, Chs. A, B	C_{LOAD} = 300pF	Full	-	90	150	ns
TP_{LHL}	Prop Delay, Lo - Hi, Ch. L	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	115	170	ns

Dynamic Electrical Specifications P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Ref to P- = 2mA. Full Temp T_J = -40°C to +150°C **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
TP_{HLA}	Prop Delay, Hi - Lo, Ch. A	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	200	320	ns
TR_{AB}	Rise Time, Channels A, B	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	20	50	ns
TF_{AL}	Fall Time Channels A, L	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	50	75	ns
TP_{LHG}	Prop Delay, Lo - Hi, Ch. G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	135	200	ns
			Full	-	-	275	ns
TP_{HLG}	Prop Delay, Hi - Lo, Ch. G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	280	400	ns
			Full	-	-	475	ns
TR_G	Rise Time, Channel G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	150	300	ns
			Full	-	-	450	ns
TF_G	Fall Time Channel G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	235	340	ns
			Full	-	-	500	ns

Timing Waveforms

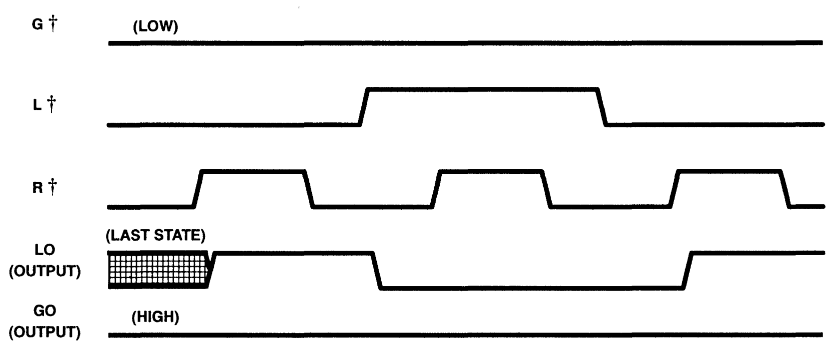
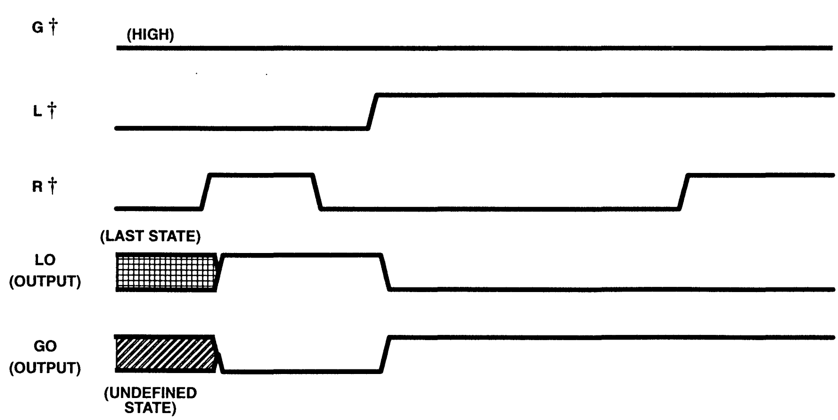


FIGURE 1.



† Refers to the state of the input comparator output

FIGURE 2.

2

MCTs

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	A-	Negative Comparator input for A channel. This input has a Protected Comparator Input that is clamped to P+ and P- through a 330 ohm resistor. The common mode input voltage, for the Protected Comparator Input, ranges from (VP-) +2V and (VP0) +2V. The CMOS output AO (Pin 24) is low when input A- is "True" and input A+ is "False".
2	A+	Positive Comparator Input for A channel. The CMOS output AO (Pin 24) is high when input A+ is "True" and input A- is "False".
3	B1-	Negative Comparator input for B1 channel. The output of the internal B1-channel comparator is low when input B1- is "True" and input B1+ is "False".
4	B1+	Positive Comparator Input for B1 channel. The output of the internal B1-channel comparator is high when input B1+ is "True" and input B1- is "False".
5	B2-	Negative Comparator Input for B2 channel. The output of the internal B2-channel comparator is low when input B2- is "True" and input B2+ is "False".
6	B2+	Positive Comparator Input for B2 channel. The output of the internal B2-channel comparator is high when input B2+ is "True" and input B2- is "False".
7	L-	Negative Comparator Input for L (Latch) channel. Latch mode operation is disabled when L- is "True" and L+ is "False". NMOS output LO (Pin 26) is active high in a no latch state. The GO output (Pin 23) is controlled by G-channel inputs.
8	L+	Positive Comparator Input for L (Latch) channel. Latch mode operation is enabled when L+ is "True" and L- is "False". NMOS output LO (Pin 26) is active low in latch state. The GO output (Pin 23) goes to a "P-MCT OFF" state (VGO = VP+) and is controlled by the internal L-channel latch; which bypasses the G-channel inputs. Latch mode always overrides the R-channel.
9	R-	Negative Comparator Input for R (Reset) channel. Reset mode, for the internal L-channel latch, is disabled when R- is "True" and R+ is "False".
10	R+	Positive Comparator Input for R (Reset) channel. Reset mode, for the internal L-channel latch, is enabled when R+ is "True" and R- is "False". Reset mode (enabled) unlatches the internal L-channel latch; which allows the G-channel inputs to control the GO output (Pin 23). Latch mode must be disabled to operate in reset mode.
11	G-	Negative Comparator Input for G (Main) channel. The G-channel output (Pin 23) goes to a "P-MCT OFF" state (VGO = VP+) when G- is "True" and G+ is "False".
12	G+	Positive Comparator Input for G (Main) channel. The G-channel output (Pin 23) goes to a "P-MCT ON" state (VGO = VP-) when G+ is "True" and G- is "False".
13	MLT	Input for programmable Minimum Low Time timing capacitor (C_T). MLT is set by connecting a capacitor between P0 (Pin 22) and MLT (Pin 13). MLT is approximated by the equation: $(C_T)(5V)/(100uA)$.
14	MHT	Input for programmable Minimum High Time timing capacitor (C_T). MHT is set by connecting a capacitor between P0 (Pin 22) and MHT (Pin 14). MHT is approximated by the equation: $(C_T)(5V)/(100\mu A)$. MHT becomes Minimum Low Time function for turning on N-MCT's.
15	REG	5V regulator output. An opto-coupler or fiber-optic receiver may be power by connecting the positive voltage pin of the IC to P0 (Pin 22) and the IC common to REG (Pin 15). The internal regulator (REG) must sink 2mA of current minimum for the MLT and MHT functions to work properly.
16	P-	Chip negative supply. This pin is generally used as the DC bias power supply common. The regulator transistor, charge pump and logic are referenced to P- (Pin 16).
17	CPB	Output of the Charge Pump Oscillator Inverter stage. A 0.47µF capacitor is normally connected from this output to CPA (Pin 19).
18	NC	Unused pin.
19	CPA	Input of the charge pump steering diode. A 0.47µF capacitor is normally connected from this input to CPB (Pin 18).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
20	CLMP	An internal 12V clamp that can be used for additional regulation across P0 (Pin 22) and P- (Pin 16).
21	POS	Positive supply rail for the charge pump.
22	P0	Chip positive supply. This pin is generally used as the DC bias power supply positive input.
23	GO	Main channel output (Gate Output). The gate output controls the switching of power devices and is normally connected to the P-MCT gate. GO can sink or source greater than 6A peak at VP+ equal to 30V.
24	AO	A-Channel Output. AO has a CMOS output that switches from P0 (Pin 22) to P- (Pin 16). AO can source or sink 10mA of DC current.
25	BO	B-Channel Output. B-channel has a PMOS output that connects BO to P0 (Pin 22) when turned on. BO can source 10mA of DC current from P0.
26	LO	L-Channel Output. L-channel has a NMOS output that connects LO to P- (Pin 16) in latch mode. LO can sink 10mA of DC current.
27	NC	Unused pin.
28	P+	High side output. Connects to the output of a charge pump steering diode. A 10.0μF capacitor is normally connected from this output to P0 (Pin 22) to supply the high side of the gate voltage.

HIP2030 Application Information

The **Harris Photo-Coupled Isolated Gate Drive** (HPCIGD) circuit, illustrated in Figure 3, contains four subcircuits: a Single Supply DC bias, a Regulated voltage divider reference, a Local Energy Source Capacitance, and a Photo-Couple Receiver.

The **Single Supply DC Bias Circuit**, shown in Figure 3, consists of a single external dropping resistor (R1) connected between pins P+ (U1-28) and P0 (U1-22). When an input voltage of 30V is applied across pins P+ and P- (U1-16), R1 forms a resistive divider network with the input impedance located between pins P0 and P- (RVP0). This allows the circuit designer to adjust the value of R1 to obtain a desired bias voltage between pins P0 and P- (VP0.). The value of RVP0 can be calculated by evaluating the equivalent Quiescent Input Impedance (RQ) and the 5V reference impedance (RR) as parallel resistances. The values for R1, RQ, RR, and RVP0 can be determined by using Equations 1(A, B, C, D) as shown in Appendix A, Exercise 1.1.

The **Regulated Voltage Divider Reference** is comprised of two resistors (R3 and R4) connected in series and are located across pins P0 and REG. This voltage divider provides a stable voltage reference to all of the HIP2030 comparator inputs. Resistors R3 and R4 are selected equal in value to create a midpoint bias reference between the peak to peak input signal of U2. Also, the midpoint bias method ensures that input signals generated from U2 and midpoint bias reference voltages are within a safe common mode voltage range of the comparators.

The **Local Energy Source Capacitances**, C1 and C2, are needed to supply the charge required to drive large capacitance loads at high dv/dts. The HPCIGD circuit uses low cost "oversized" tantalum capacitors (C = 10μF) that are used for C1 and C2. If rise times and overshoot are critical, ceramic capacitors with low ESL and ESR should be used to improve gate drive signals. In a power circuit, where the gate driver is exposed to high dv/dts, the network of C1 and C2 directs noise current away from the HIP2030. This allows the HFOIGD circuit to operate well in half bridge power circuits that use a transformer coupled power source.

The **Photo-Coupled Receiver** subcircuit consists of U2, R5, C4, and R6. U2 is a photocoupler which combines an infrared emitter diode (IRED) and a high speed photo detector to translate light pulses to low voltage input signals. These signals are routed to the G channel and are used to control the output GO. Component R5 is used to limit the DC current through the IRED when the input signal voltage switches to its most positive level. A wide range of input voltages may be accommodated by varying R5 to limit the IRED current to 25mA. C4 is a speed up capacitor and is selected to match the forward bias capacitance of the IR diode. The last component, R6, is an optional part and is intended to be a termination resistor with the value set by the user.

The Harris HIP2030 Evaluation Board (HIP2030EVAL) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030DB circuit enables the user to conveniently populate the PCB for either Photo-Coupled or fiber-optic receivers. In addition, the PCB layout has provisions for "on board prototyping" and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030. The schematic of the HIP2030DB, illustrated in Figure 4, uses the basic HPCIGD circuitry and has provisions for "on board prototyping" and special function components.

TABLE 1. LOGIC

INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

1 = Input True
0 = Input False
U = Undefined
LS = Last State

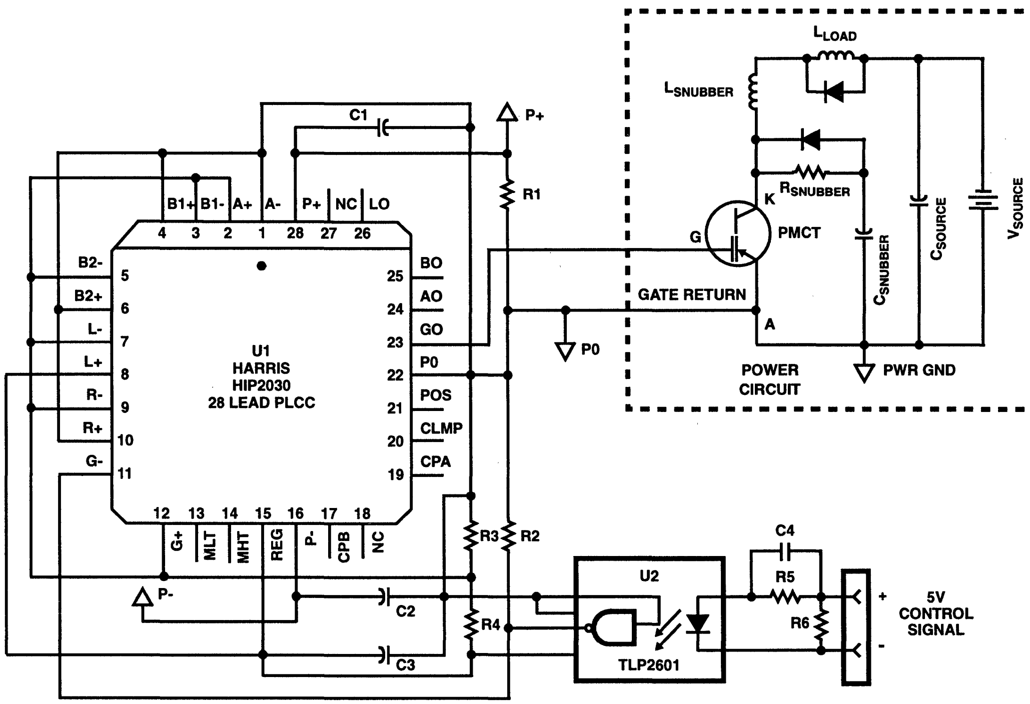


FIGURE 3. HARRIS PHOTO-COUPLED ISOLATED GATE DRIVE

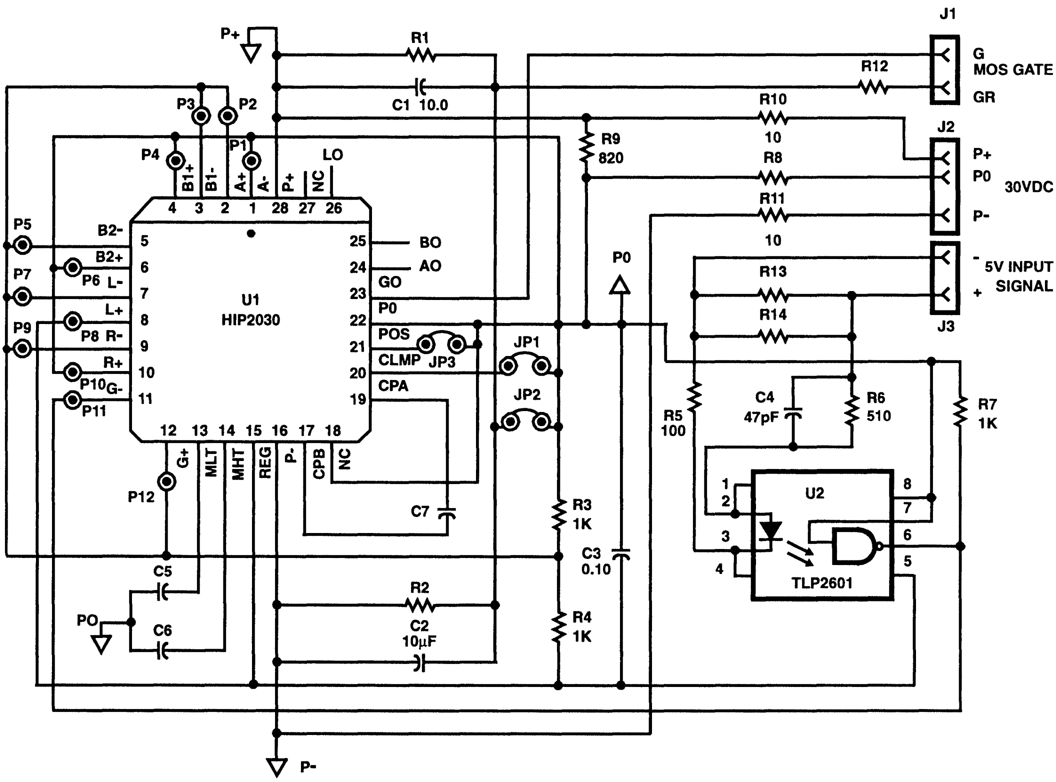


FIGURE 4. HARRIS HIP2030 EVALUATION BOARD (NOTE 9)

NOTES:

1. Capacitors C5 and C6 are special function components which control MLT and MHT.
2. Asymmetrical gate drive may be obtained by opening J2 and adjusting R1 and R2 for the desired voltage ratio.
3. Insert C7 for charge pump operation.
4. Open J3 to disable the charge pump oscillator.
5. Open J1 to disable the internal 12V regulator.
6. R5 is added for noise rejection at high Cdv/dts.
7. The internal 5V reference (REF) must be operational for MHT and MLT functions to work properly.
8. P1 - P12 are access pads for all comparator inputs.
9. Request Harris File #3918 for a full description of the HIP2030EVAL board.

Typical Performance Curves

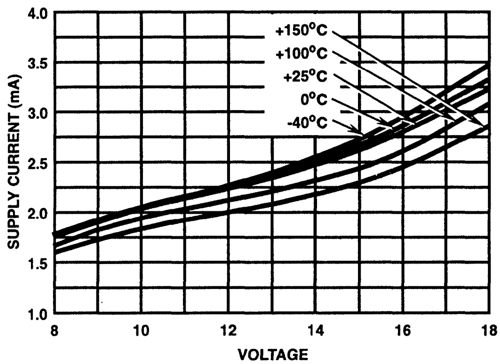


FIGURE 5. SUPPLY CURRENT (IP0) vs SUPPLY VOLTAGE (P0)

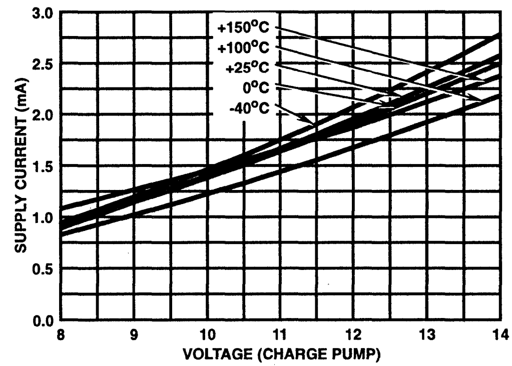


FIGURE 6. SUPPLY CURRENT (IPOS) vs SUPPLY VOLTAGE (POS)

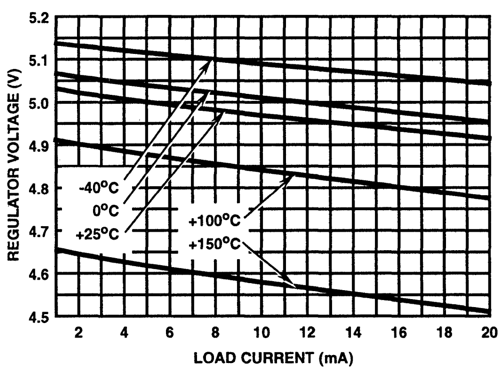


FIGURE 7. REGULATOR VOLTAGE vs LOAD CURRENT

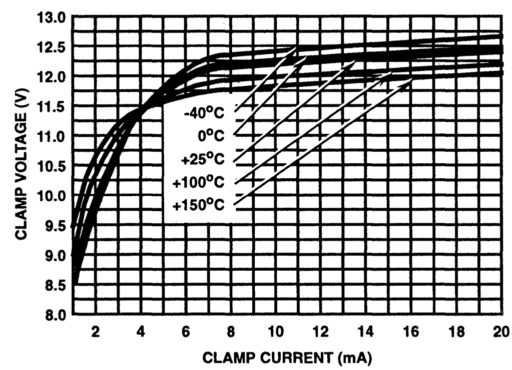


FIGURE 8. CLAMP VOLTAGE vs CLAMP CURRENT

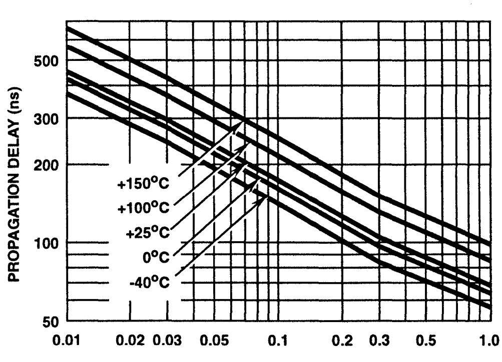


FIGURE 9. PROPAGATION DELAY vs VOLTAGE OVERDRIVE FOR A, B1, AND B2 CHANNELS

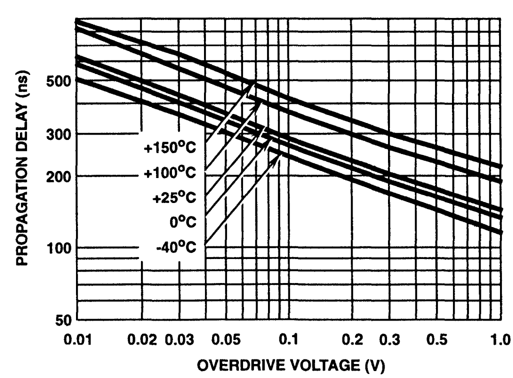


FIGURE 10. PROPAGATION DELAY vs VOLTAGE OVERDRIVE FOR G CHANNEL

Typical Performance Curves (Continued)

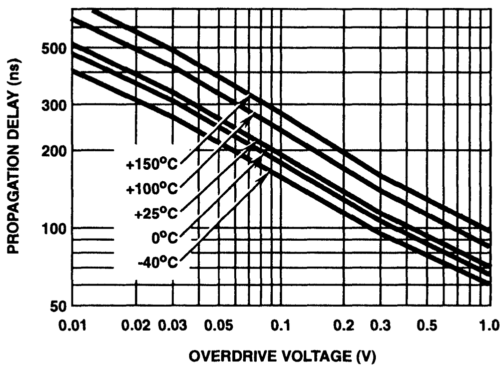


FIGURE 11. PROPAGATION DELAY vs VOLTAGE OVERDRIVE FOR R AND L CHANNELS

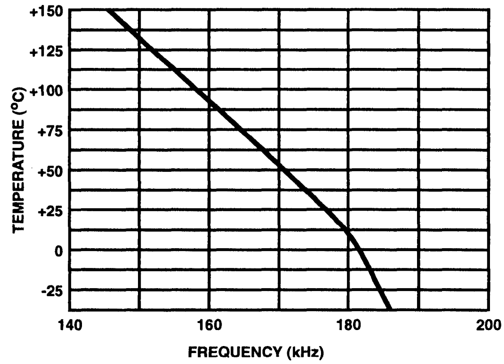


FIGURE 12. OSCILLATOR FREQUENCY OVER TEMPERATURE FOR CHARGE PUMP

Appendix A Exercises

Exercise 1.1

Q: How do I calculate the value of the series dropping resistor R1, shown in Figure 3?

A: The values for R1, R_Q, R_R and R_{VPO} can be determined by using Equations 1 (A, B, C, and D).

$$R_Q = \frac{V_{PO}}{I_{QPO}} \quad \text{(EQ. 1A)}$$

$$R_R = \frac{V_{PO}}{I_{OPTO} + I_{VDR} + I_{RP}} \quad \text{(EQ. 1B)}$$

$$R_{VPO} = \frac{1}{\frac{1}{R_Q} + \frac{1}{R_R}} \quad \text{(EQ. 1C)}$$

Where:
- V_{PO} = Voltage between pins P0 and P- (U1 - U22 and U1 - U16).
- I_{QPO} = Quiescent current flowing into pin P0.
- I_{QPTO} = Quiescent current of the HBR-2521 fiber-optic receiver.
- I_{VDR} = Current flowing through R3 and R4 (voltage divider reference).
- I_{RP} = Current flowing through pull up resistor R2 (in "ON" or "OFF" state)

The maximum value of R1 can easily be determined in four design steps:

1. Assume the following values:

   V_{IN} = 30V DC
   I_{QPO} = 2.75mA at V_{P0} = 15V
   I_{OPTO} = 5mA
   I_{VDR} = 2.5mA
   $I_{RP(ON)}$ = 5mA, R2 = 1K, VR2 = 5V

2. Select a usable value of V_{P0} between 7V and 15V DC.

   Use V_{P0} = 15V

3. Solve for R_{VP0} using Equations 1 (A, B, and C):

$$R_Q = \frac{15V}{2.75mA} = 5.45K$$

$$R_R = \frac{15V}{(5mA + 2.5mA + 5mA)} = 1.20K$$

$$R_{VP0} = \frac{1}{\frac{1}{5.45K} + \frac{1}{1.20K}} = 984$$

4. Solve for R1 using Equation 1(D):

$$R1 = \frac{R_{VP0}(V_{IN} - V_{P0})}{V_{P0}} \quad \text{(EQ. 1D)}$$

$$R1 = \frac{984\,(30V - 15V)}{15V} = 984$$

HARRIS SEMICONDUCTOR

HIP2030EVAL

August 1994

Isolated MCT/IGBT Gate Driver Evaluation Board

Features

- 3000VDC Isolation
- 10,000V/µS dv/dt Capability
- ± Polarity Gate Drive
- Standard Opto-Coupler LED Input
- Peak Output Current 6.0A
- Power CMOS Output Stage
- Fast Rise Time . . . . .200ns at 60,000pF
- Ability to Drive MCT or IGBT Modules
- Programmable Minimum ON/OFF (Times)
- On Board Prototyping Area
- 120kHz Gate Switching . . . . C_{LOAD} at 15,000pF

Applications

- Resonant Inverters
- Motor Controllers
- Uninterruptible Power Supplies
- Inverters
- Converters
- Arc Welders

Ordering Information

PART NUMBER	TEMPERATURE RANGE
HIP2030EVAL	-40°C to +85°C

Description

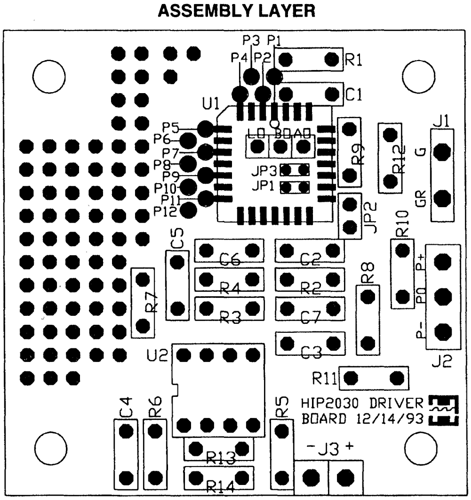
The HIP2030 is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dv/dts). This device is optimized for driving 60nF of MOS gate capacitance at 30V peak to peak in less than 200ns. The half bridge gate driver is ideal for driving MOS Controlled Thyristor (MCT) and IGBT modules.

The architecture of the HIP2030 includes four comparator input channels, a 5V reference, a 12V regulator, and a high side charge pump. The device provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (channels A and B) that can be used as monitors (temperature sensing), indicators (LEDs or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators.

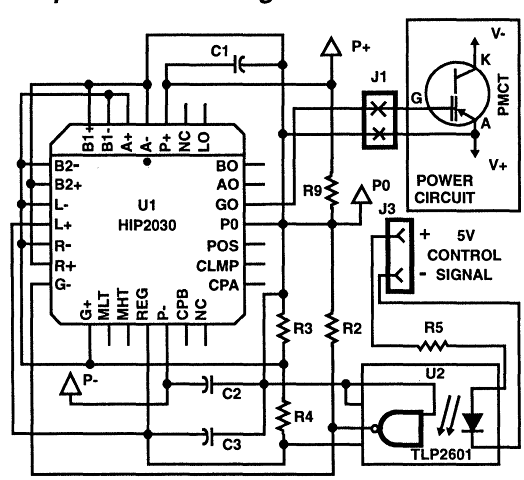
The Harris HIP2030 Evaluation Board (HIP2030EVAL) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030EVAL circuit enables the user to conveniently utilize either photo-coupled or fiber-optic receivers. In addition, the PCB layout has provisions for "on board prototyping" and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030.

Board Layout

ASSEMBLY LAYER



Simplified Board Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3918

HIP2030EVAL Application Information

Initial HIP2030EVAL Configuration

The HIP2030EVAL is populated with the Harris Photo-Coupled Isolated Gate Driver (HPCIGD) components and is configured as a dual polarity gate driver. To operate the driver board, the user must provide a damping resistor, an isolated DC bias voltage between 24V and 30V, and a control signal to the photo-coupler subcircuit. The schematic of the HIP2030EVAL shows the initial jumper and component configurations in the PCB Schematic. For more detailed information please refer to Applications Note AN9408.

DC Input Power

The HIP2030EVAL is configured for a 12V regulated single supply DC bias (SSDCB) operation. The SSDCB bias scheme allows the HIP2030EVAL to operate reliably with a single isolated DC supply and will accept input bias voltages ranging from 24V to 30V. Dropping resistor R9 and an internal clamp V_{CLMP} are used in combination to provide a regulated 12VDC bias voltage for the HIP2030 logic circuitry. The DC voltage input connections, for SSDCB operation, are applied to connector J2 between inputs P+ and P-.

Control Signal

HIP2030EVAL photo-coupler input can be driven with any signal generator that can supply a control signal with a pulse amplitude of 5V peak and provide 25mA of diode current. The input signal connections for the photo-coupled subcircuit, shown in the Simplified Board Diagram, are applied to connector J3 between inputs (+) and (-). The input signal requirements of the HIP2030EVAL are designed to be simple and allows the user to control the driver board with peripherals that contain either discrete logic or linear circuits.

Gate Output (GO)

The HIP2030EVAL is configured as a dual polarity gate driver with the gate return referenced to P0. In this mode of operation, the HIP2030 generates a -12V or a +18V output voltage when the SSDCB voltage equals 30V. The GO output connections, for -12V or +18V operation, are located at connector J1 between inputs G and GR.

Methods of DC Bias

The HIP2030EVAL can be biased in one of three configurations: a single supply (with a dropping resistor), a dual supply, and a single supply with a high side charge pump.

Single supply operation, using a dropping resistor (R9) and V_{CLMP}, uses one high side voltage supply and provides enough charging current to drive large capacitive loads at high frequencies. An example of this bias scheme is shown in the PCB Schematic.

Dual supply biasing (DSB) is configured by removing the droppigng resistor, adding a bias resistor and connecting two isolated power supplies. Follow steps 1 through 6 to use the DSB.

1. Apply voltage source #1 (V1) between P0 and P-.
2. Apply voltage source #2 (V2) between P+ and P0.
3. Install 10Ω resistor R8.
4. Remove dropping resistor R9.
5. Adjust V1 to provide the desired negative gate drive voltage.
6. Adjust V2 to provide the desired positive gate drive voltage.

Adjusting Gate Drive Output Polarity

The driver board is configured for driving a generic power switch and references the gate drive to P0; which is approximately half the voltage that is applied between P+ and P-. The HIP2030EVAL has provided the ability to adjust the gate drive output polarity to accommodate input voltage requirements for various power switches. Configurations for symmetric and asymmetric output polarities are given below.

Symmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference). Add R1 and R2 (select equal values of R1 and R2; typical values are between 1K and 10K).

Asymmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference), select R2 with this equation:

$$R2 = \left[\frac{(VPO)\,(R1)}{((VP+) - VPO)}\right] \qquad \text{(EQ. 1)}$$

Add R1 and R2 (typical values are between 1K and 10K).

Jumper Settings

Jumpers JP1, JP2, and JP3 are initially configured as shorts. Jumpers names and their functions are listed:

JP1 - Connect the internal 12V clamp, located inside the HIP2030, across P0 to P-.

JP2 - Use P0 for the gate return reference.

JP3 - Applies DC bias voltage to charge pump circuitry.

Minimum High and Low Time Functions

The HIP2030 provides two special functions that are unique to driving MCT power devices. These functions are called Minimum High Time (MHT) and Minimum Low Time (MLT). MLT and MHT are used to ensure that input control signals, with gate signals <1μs in duration, turn on and off the MCT devices reliability. The time settings for MHT and MLT are set as a function of MCT "ON" and "OFF" delay times. Both of these time settings can be independently programmed by installing a capacitor between its function pin (MHT and MLT) and pin P0. The value of either capacitor can be approximated by the equation:

$$C = \frac{(100\mu A)\,(DELAYTIME)}{5V} \qquad \text{(EQ. 2)}$$

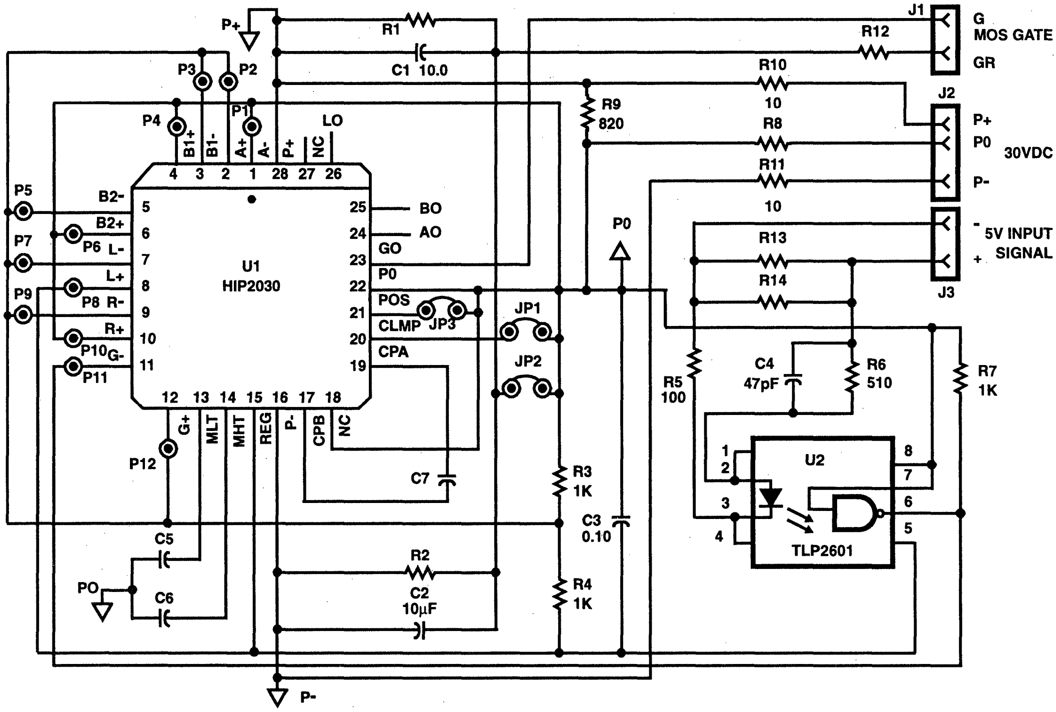
Monitor Channel Outputs

Channel outputs A, B, and L are accessed on the solder side of the HIP2030EVAL and are located above jumpers JP3 and JP4. The locations for AO, BO, LO, J1, and J3 are illustrated in the HIP2030EVAL PCB assembly layer drawing.

On Board Prototyping Suggestions

The HIP2030EVAL PCB furnishes the experimenter with a 1" x 0.6" prototyping area that provides a 62mil solder pad array at 100mil spacing. Pads P1 through P12, located at the inputs of the voltage comparators, are used as access points to the channel inputs and may be jumpered over to the prototype areas. These pads are currently connected to either the middle of the regulated voltage divider (between R3 and R4), P0 (U1-22), REG (U1-15) or control signal (U2-6). These traces are easily cut with the use of an "exacto-knife" and can be disconnected to prototype various circuits.

PCB Schematic



NOTES:

1. Capacitors C5 and C6 are special function components which control MLT and MHT.
2. Asymmetrical gate drive may be obtained by opening J2 and adjusting R1 and R2 for the desired voltage ratio.
3. Insert C7 for charge pump operation.
4. Open J3 to disable the charge pump oscillator.
5. Open J1 to disable the internal 12V regulator.
6. R5 is added for noise rejection at Cdv/dts.
7. The internal 5V regulator (REG) must be operational for MHT and MLT functions to work properly.
8. P1 - P12 are access pads for all comparitor inputs.

TABLE 1. EVALUATION BOARD PARTS LIST

REFERENCE DESIGNATOR	VALUE	TYPE
R1, R2, R8, R12, R13, R14	Unpopulated	1/3W Metal Film (1%)
R3, R4, R7	1K	1/3W Metal Film (1%)
R5	100Ω	1/3W Metal Film (1%)
R6	510Ω	1/3W Metal Film (1%)
R9	820Ω	1/3W Metal Film (1%)
R10, R11	10Ω	1/3W Metal Film (1%)
R12 (Damping Resistor)	Unpopulated	1/3W Metal Film (1%)
R13, R14	Unpopulated	1/3W Metal Film (1%)
C1, C2	10μF	Tantalum at 35V
C3	0.1μF	Ceramic at 35V
C4	47pF	Mica at 50V
C5, C6 (MLT/MHT)	Unpopulated (20pF - 100μF)	Varies Based on Capacitance Size
C7 (Charge Pump)	Unpopulated (0.01μF Typ)	Varies Based on Capacitance Size
U1	HIP2030	28 Pin PLCC
U2	TLP2601	8 Pin Plastic Dip

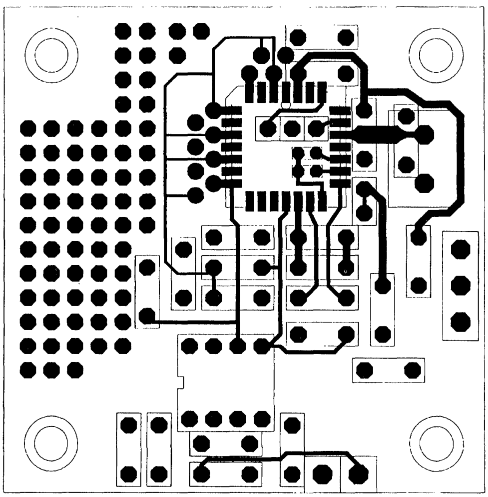
TABLE 2. LOGIC

INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

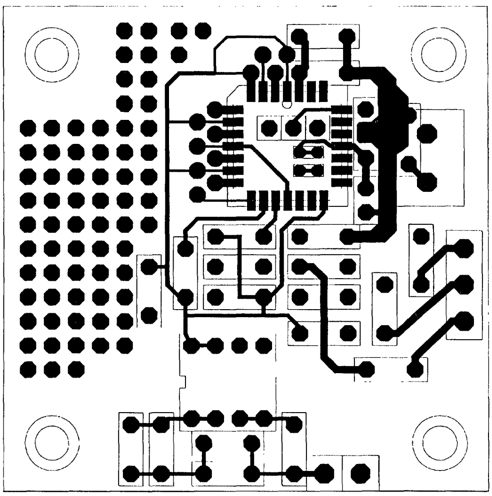
1 = Input True
0 = Input False
U = Undefined
LS = Last State

Board Layouts

TOP LAYER



BOTTOM LAYER

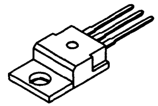
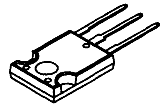
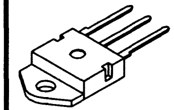
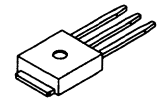
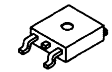
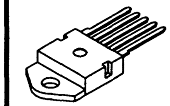


MCT/IGBT/DIODES 3

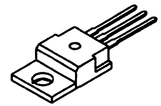
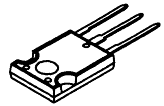
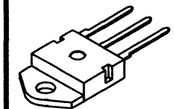
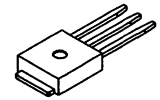
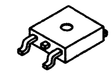
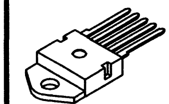
INSULATED GATE BIPOLAR TRANSISTORS

Insulated Gate Bipolar Transistors (Continued)

HARRIS IGBT PRODUCT LINE

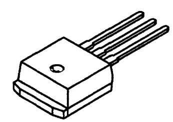
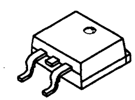
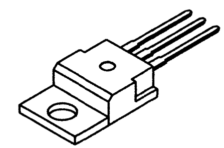
MAXIMUM RATINGS									
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_F (μs)	TO-220AB	TO-247	TO-218AC	TO-251AA	TO-252AA	MO-093AA
400	6	7.5	1.0				HGTD6N40E1	HGTD6N40E1S	
	10	12	1.2				HGTD10N40F1	HGTD10N40F1S	
	10	17.5	1.0	HGTP10N40E1					
			0.5	HGTP10N40C1					
	12	17.5	1.0			HGTH12N40E1			
			0.5			HGTH12N40C1			
	15	35	1.0	HGTP15N40E1					
			0.5	HGTP15N40C1					
	20	35	1.0			HGTH20N40E1			
			0.5			HGTH20N40C1			
500	5	10	1.0						
			0.5						
	6	7.5	1.0				HGTD6N50E1	HGTD6N50E1S	
	10	12	1.2				HGTD10N50F1	HGTD10N50F1S	
	10	17.5	1.0	HGTP10N50E1					
			0.5	HGTP10N50C1					
	12	17.5	1.0			HGTH12N50E1			
			0.5			HGTH12N50C1			
	15	35	1.0	HGTP15N50E1					
			0.5	HGTP15N50C1					
	20	35	1.0			HGTH20N50E1			
			0.5			HGTH20N50C1			

HARRIS IGBT PRODUCT LINE (Continued)

MAXIMUM RATINGS									
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_F (µs)	TO-220AB	TO-247	TO-218AC	TO-251AA	TO-252AA	MO-093AA
600	12	48	0.6	HGTP12N60D1					
	24	96	0.6		HGTG24N60D1				
	32	200	0.8		HGTG32N60E2				HGTA32N60E2
1000	20	100	0.68		HGTG20N100D2				
	34	200	0.87		HGTG34N100E2				
1200	20	100	1.00		HGTG20N120E2				
	30	200	0.75		HGTG30N120D2				

SHADING indicates DEVELOPMENTAL PRODUCTS
NOTES:
1. I_{C90} = maximum continuous current rating at $T_C = +90^oC$.
2. I_{CM} = maximum pulsed current rating.
3. t_F measured at $T_C = +150^oC$.

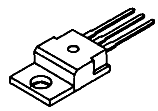
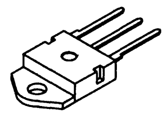
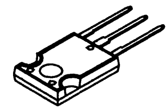
HARRIS IGBTs FEATURING LOGIC LEVEL DRIVE AND COLLECTOR-GATE VOLTAGE CLAMPING

MAXIMUM RATINGS AT $T_C = 25^oC$								
BV_{CLAMP} (V)	I_{C100} (A)	$V_{CE(SAT)}$ (A)	R_G (Ω)	R_{GE} (Ω)	INDUCTIVE USE TEST (A)	TO-262AA	TO-263AB	TO-220AB
350 - 420	14 at 90°C	2.0 at 10A, 4.5V	1k (Typ)	None	17 at L = 2.3mHy			HGTP14N40P3VL
320 - 390	20	1.6 at 10A, 4.5V	1k (Typ)	12k - 24k	26 at L = 2.3mHy	HGT1S20N35G3VL	HGT1S20N35G3VLS	HGTP20N35G3VL
330 - 390	14	1.45 at 7A, 4.5V	75 (Typ)	10k - 30k	17 at L = 2.3mHy	HGT1S14N36G3VL	HGT1S14N36G3VLS	HGTP14N36G3VL

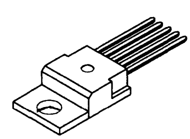
SHADING indicates DEVELOPMENTAL PRODUCTS
NOTES:
4. I_{C100} = maximum continuous current rating at $T_C = +100^oC$.

Selection Guide (Continued)

HARRIS IGBT'S WITH AN INTEGRAL REVERSE DIODE

MAXIMUM RATINGS						
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_F (μs)	TO-220AB	TO-218AC	TO-247
400	6	7.5	1.0	HGTP6N40E1D		
	10	12	1.2	HGTP10N40F1D		
	10	17.5	1.0	HGTP10N40E1D		
			0.5	HGTP10N40C1D		
	12	17.5	1.0		HGTH12N40E1D	
			0.5		HGTH12N40C1D	
	20	35	1.0		HGTH20N40E1D	
			0.5		HGTH20N40C1D	
500	6	7.5	1.0	HGTP6N50E1D		
	10	12	1.2	HGTP10N50F1D		
	10	17.5	1.0	HGTP10N50E1D		
			0.5	HGTP10N50C1D		
	12	17.5	1.0		HGTH12N50E1D	
			0.5		HGTH12N50C1D	
	20	35	1.0		HGTH20N50E1D	
			0.5		HGTH20N50C1D	HGTG20N50C1D
600	12	48	0.6			HGTG12N60D1D
	24	96	0.6			HGTG24N60D1D

HARRIS IGBT'S WITH INTEGRAL CURRENT SENSING

MAXIMUM RATINGS				
BV_{CES} (V)	I_{C90} (A)	I_{CM} (A)	t_F (μs)	TS-001AA (5 LEAD TO-220)
600	12	40	1.0	HGTB12N60D1C

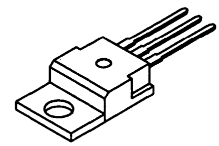
NOTES:

1. I_{C90} = maximum continuous current rating at T_C = +90°C.
2. I_{CM} = maximum pulsed current rating.
3. t_F measured at T_C = +150°C.

3

IGBTs

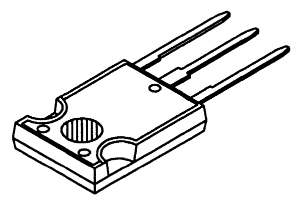
HARRIS "UFS" ULTRA FAST SWITCHING IGBT PRODUCT LINE

MAXIMUM RATINGS				
BV_{CES} (V)	I_{C110} (A)	SCWT (µs)	t_F (µs)	TO-220AB
600	20	4 at 15V 10 at 10V	0.2	HGTP20N60B3

NOTES:

1. I_{C110} = maximum continuous current rating at $T_C = +110^oC$.
2. SCWT = Short Circuit Withstand Time (minimum capability).
3. t_F measured at $T_C = +150^oC$.

HARRIS "UFS" ULTRA FAST SWITCHING IGBT PRODUCT LINE WITH AN INTEGRAL REVERSE DIODE

MAXIMUM RATINGS					
BV_{CES} (V)	I_{C110} (A)	SCWT (µs)	t_F (µs)	DIODE t_{RR} (ns)	TO-247
600	20	4 at 15V 10 at 10V	0.2	55	HGTP20N60B3D

NOTES:

1. I_{C110} = maximum continuous current rating at $T_C = +110^oC$.
2. SCWT = Short Circuit Withstand Time (minimum capability).
3. t_F measured at $T_C = +150^oC$.
4. Diode t_{RR} measured at $I_{EC} = 20A$, $dI_{EC}/dt = 100A/\mu s$, $T_C = 25^oC$.

HARRIS SEMICONDUCTOR

HGTD6N40E1, HGTD6N40E1S, HGTD6N50E1, HGTD6N50E1S

April 1995

6A, 400V and 500V N-Channel IGBTs

Features

- 6A, 400V and 500V
- $V_{CE(ON)}$: 2.5V Max.
- T_{FALL}: 1.0μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

The HGTD6N40E1, HGTD6N40E1S, HGTD6N50E1, and HGTD6N50E1S are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low power integrated circuits.

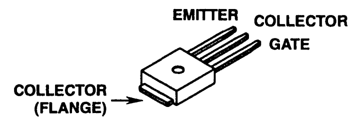
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTD6N40E1	TO-251AA	G6N40E
HGTD6N50E1	TO-251AA	G6N50E
HGTD6N40E1S	TO-252AA	G6N40E
HGTD6N50E1S	TO-252AA	G6N50E

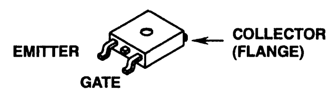
NOTE: When ordering, use the entire part number.

Packages

HGTD6N40E1, HGTD6N50E1
JEDEC TO-251AA

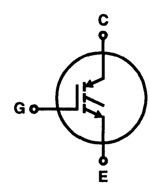


HGTD6N40E1S, HGTD6N50E1S
JEDEC TO-252AA



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTD6N40E1 HGTD6N40E1S	HGTD6N50E1 HGTD6N50E1S	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	7.5	7.5	A
at $T_C = +90^oC$	I_{C90}	6.0	6.0	A
Power Dissipation Total at $T_C = +25^oC$	P_D	60	60	W
Power Dissipation Derating $T_C > +25^oC$		0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2413.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS HGTD6N40E1 HGTD6N40E1S MIN	HGTD6N40E1 HGTD6N40E1S MAX	HGTD6N50E1 HGTD6N50E1S MIN	HGTD6N50E1 HGTD6N50E1S MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, I_C = 1mA	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	T_J = +150°C, V_{CE} = 400V	-	250	-	-	μA
		T_J = +150°C, V_{CE} = 500V	-	-	-	250	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0V	-	100	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(ON)}$	T_J = +150°C, I_C = 3A, V_{GE} = 10V	-	2.9	-	2.9	V
		T_J = +150°C, I_C = 3A, V_{GE} = 15V	-	2.5	-	2.5	V
		T_J = +25°C, I_C = 3A, V_{GE} = 10V	-	2.5	-	2.5	V
		T_J = +25°C, I_C = 3A, V_{GE} = 15V	-	2.4	-	2.4	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 3A, V_{CE} = 10V	6.5 (Typ)				V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 3A, V_{CE} = 10V	6.9 (Typ)				nC
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, I_C = 3A, V_{CE} = 400V, R_L = 133Ω, T_J = +150°C, V_{GE} = 10V, R_G = 25Ω	90 (Typ)				ns
Rise Time	t_R		32 (Typ)				ns
Turn-Off Delay Time	$t_{D(OFF)}$		24 (Typ)				ns
Fall Time	t_F		1100 (Typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		0.29 (Typ)				mJ
Turn-Off Delay Time	$t_{D(OFF)I}$	Inductive Load (See Figure 11), I_C = 3A, $V_{CE(CLP)}$ = 400V, R_L = 133Ω, L = 50μH, T_J = +150°C, V_{GE} = 10V, R_G = 25Ω	-	190	-	190	ns
Fall Time	t_{FI}		-	1	-	1	μs
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		-	0.43	-	0.43	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{θJC}$		-	2.08	-	2.08	°C/W

Typical Performance Curves

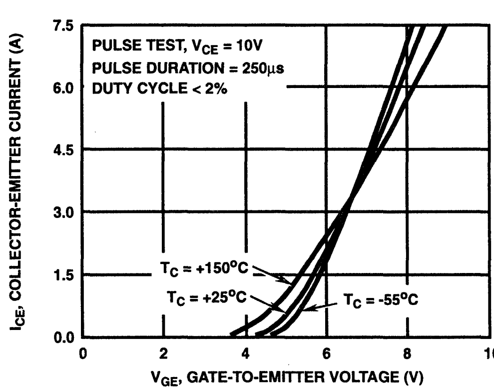


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

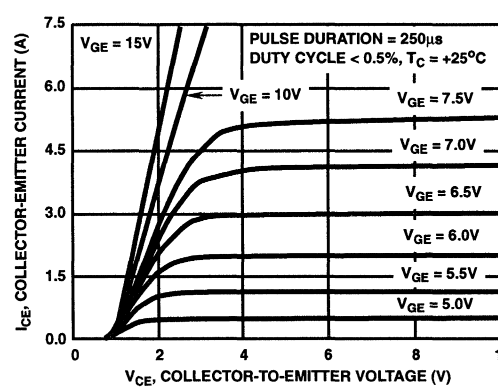


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

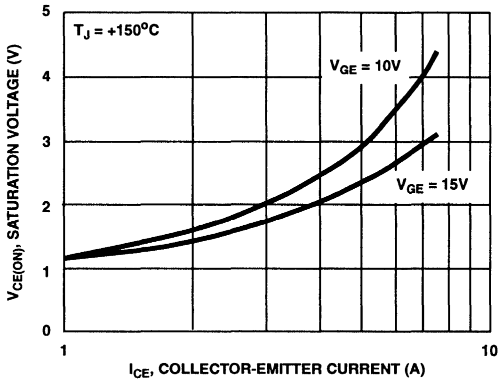


FIGURE 3. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT (TYPICAL)

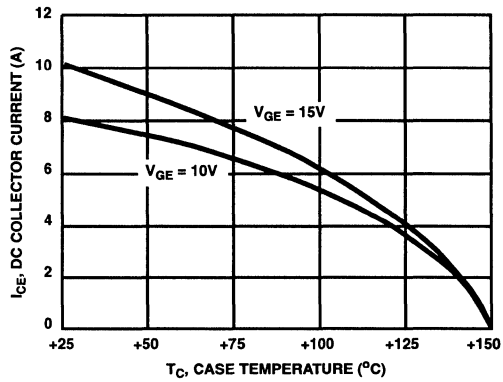


FIGURE 4. DC COLLECTOR CURRENT vs CASE TEMPERATURE

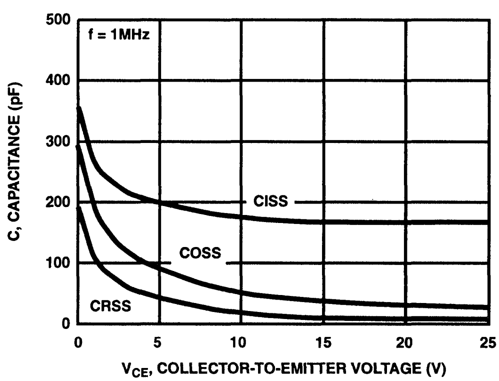


FIGURE 5. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

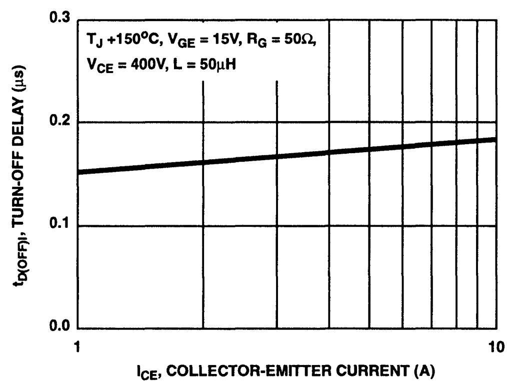


FIGURE 6. TURN-OFF DELAY vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

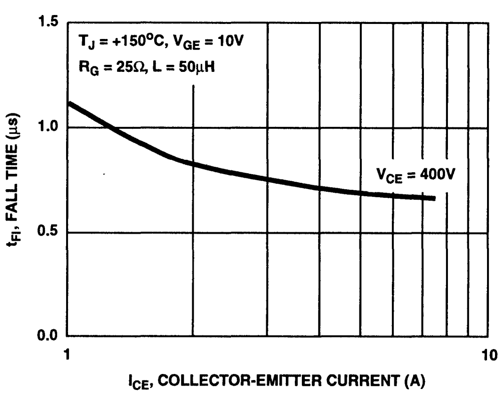


FIGURE 7. FALL TIME vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

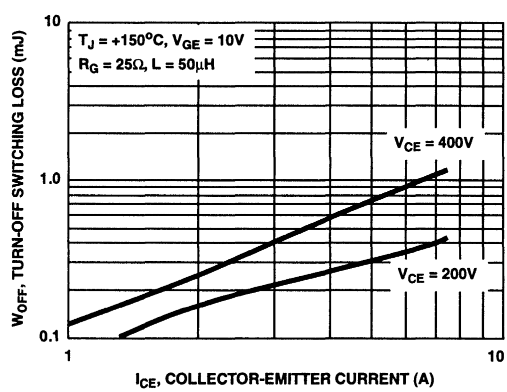


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT (TYPICAL)

Typical Performance Curves (Continued)

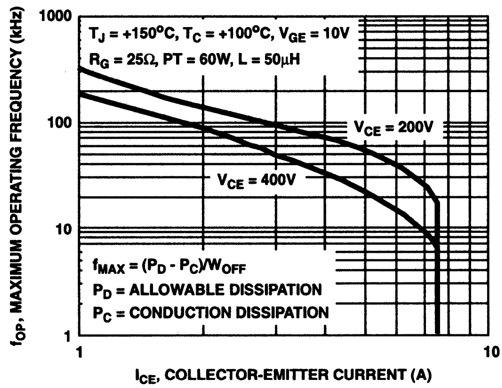


FIGURE 9. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

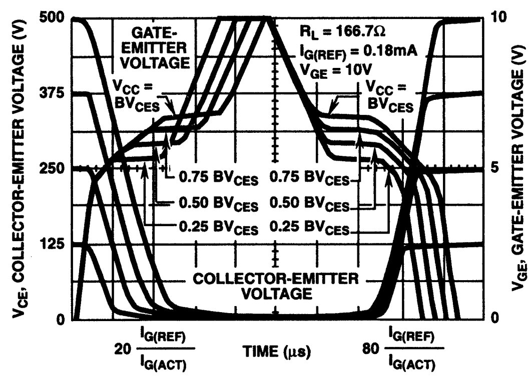


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

Test Circuit

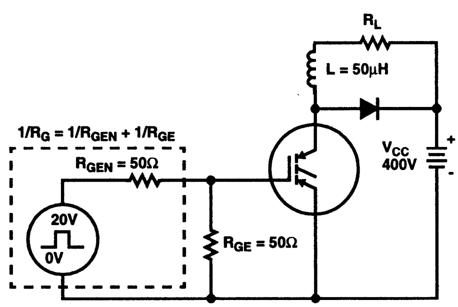


FIGURE 11. INDUCTIVE SWITCHING TEST CIRCUIT

HGTP6N40E1D, HGTP6N50E1D

HARRIS SEMICONDUCTOR

6A, 400V and 500V N-Channel IGBTs with Anti-Parallel Ultrafast Diodes

April 1995

Features

- 6A, 400V and 500V
- Latch Free Operation
- T_{FALL}: < 1.0μs
- High Input Impedance
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{RR} < 60ns

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{RR} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

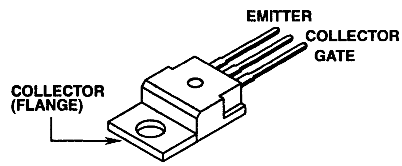
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP6N40E1D	TO-220AB	G6N40E1D
HGTP6N50E1D	TO-220AB	G6N50E1D

NOTE: When ordering, use the entire part number

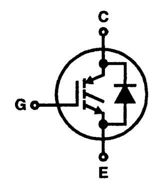
Package

JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

IGBTs

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTP6N40E1D	HGTP6N50E1D	UNITS
Collector-Emitter Voltage	BV_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	400	500	V
Collector Current Continuous at T_C = +25°C	I_{C25}	7.5	7.5	A
at T_C = +90°C	I_{C90}	6	6	A
Collector Current Pulsed (Note 1)	I_{CM}	7.5	7.5	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	±20	V
Diode Forward Current at T_C = +25°C	I_{F25}	10	10	A
at T_C = +90°C	I_{F90}	6	6	A
Power Dissipation Total at T_C = +25°C	P_D	75	75	W
Power Dissipation Derating T_C > +25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	260	°C

NOTE:
1. T_J = +150°C, Min. R_{GE} = 25Ω without latch.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2795.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

			LIMITS				
			HGTP6N40E1D		HGTP6N50E1D		
PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	MAX	MIN	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1.25mA$, $V_{GE} = 0V$	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, $I_C = 1mA$	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	$T_J = +150^oC$, $V_{CE} = 400V$	-	1.25	-	-	mA
		$T_J = +150^oC$, $V_{CE} = 500V$	-	-	-	1.25	mA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm20V$, $V_{CE} = 0V$	-	100	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(ON)}$	$T_J = +150^oC$, $I_C = 3A$, $V_{GE} = 10V$	-	2.9	-	2.9	V
		$T_J = +150^oC$, $I_C = 3A$, $V_{GE} = 15V$	-	2.5	-	2.5	V
		$T_J = +25^oC$, $I_C = 3A$, $V_{GE} = 10V$	-	2.5	-	2.5	V
		$T_J = +25^oC$, $I_C = 3A$, $V_{GE} = 15V$	-	2.4	-	2.4	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 3A$, $V_{CE} = 10V$	6.5 (Typ)				V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 3A$, $V_{CE} = 10V$	6.9 (Typ)				nC
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, $I_C = 3A$, $V_{CE} = 400V$, $R_L = 133\Omega$, $T_J = +150^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	90 (Typ)				ns
Rise Time	t_R		32 (Typ)				ns
Turn-Off Delay Time	$t_{D(OFF)}$		24 (Typ)				ns
Fall Time	t_F		1100 (Typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		0.29 (Typ)				mJ
Turn-Off Delay Time	$t_{D(OFF)I}$	Inductive Load (See Figure 13), $I_C = 3A$, $V_{CE(CLP)} = 400V$, $R_L = 133\Omega$, $L = 50\mu H$, $T_J = +150^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	-	190	-	190	ns
Fall Time	t_{FI}		-	1	-	1	µs
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		-	0.43	-	0.43	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		-	2.08	-	2.08	$^oC/W$
Thermal Resistance of Diode	$R_{\theta JC}$		-	2.00	-	2.00	$^oC/W$
Diode Forward Voltage	V_{EC}	$I_{EC} = 6A$	-	1.6	-	1.6	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 6A$, $dI_{EC}/dt = 100A/\mu s$	-	60	-	60	ns

Typical Performance Curves

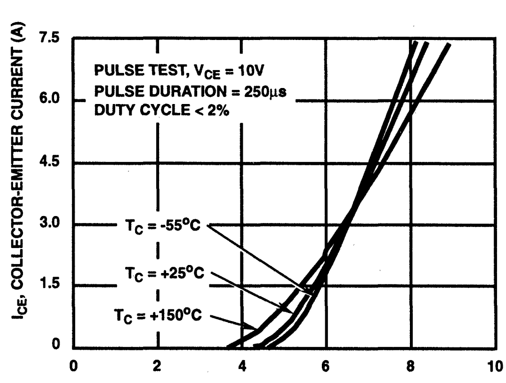


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

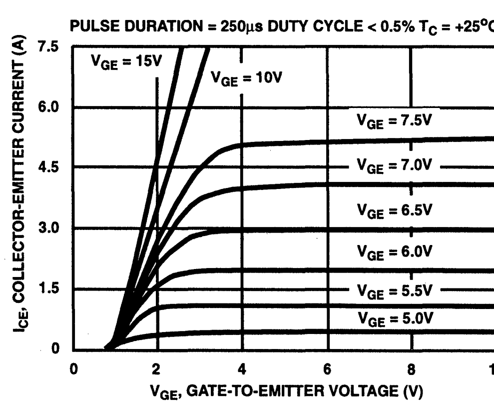


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

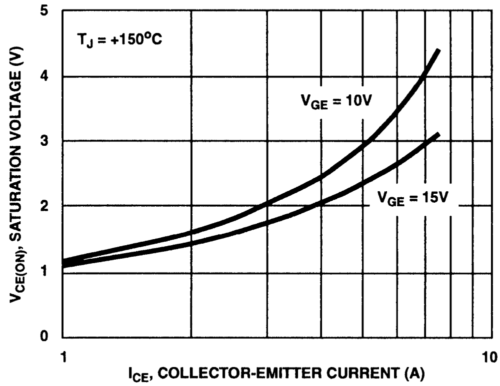


FIGURE 3. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT (TYPICAL)

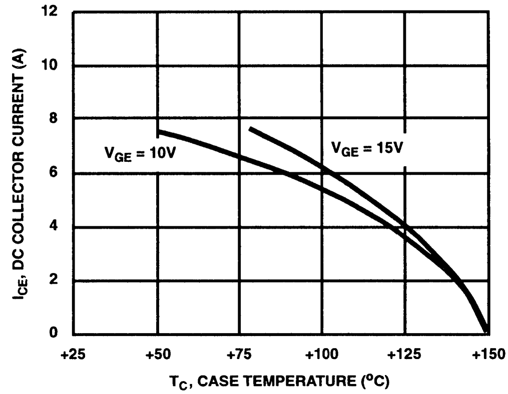


FIGURE 4. DC COLLECTOR CURRENT vs CASE TEMPERATURE

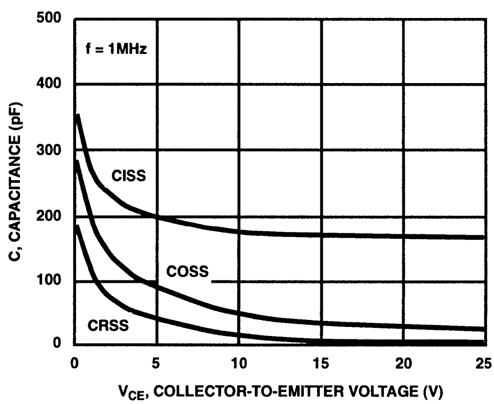


FIGURE 5. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

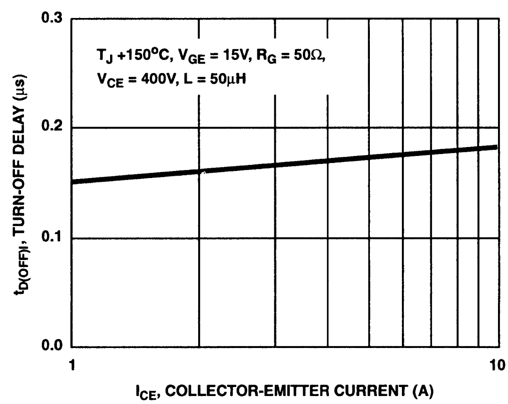


FIGURE 6. TURN-OFF DELAY vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

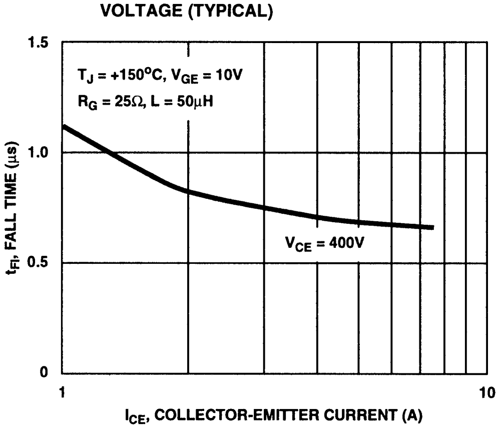


FIGURE 7. FALL TIME vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

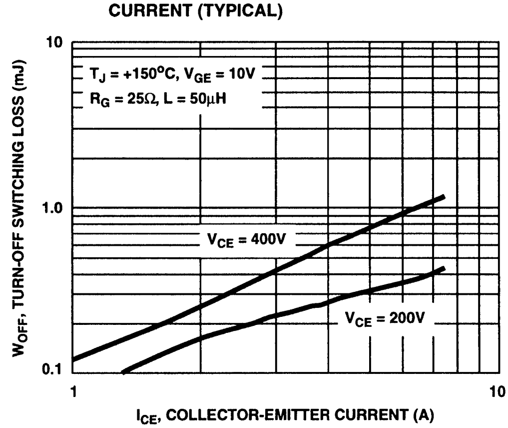


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT (TYPICAL)

3

IGBTs

Typical Performance Curves (Continued)

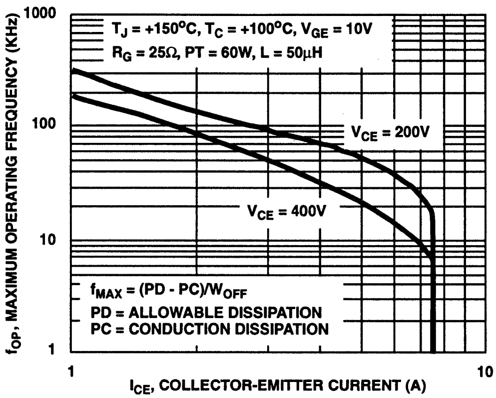


FIGURE 9. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

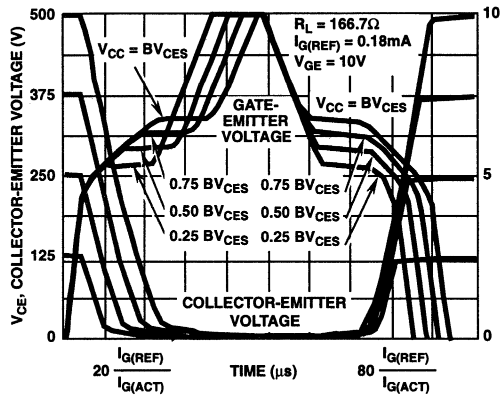


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

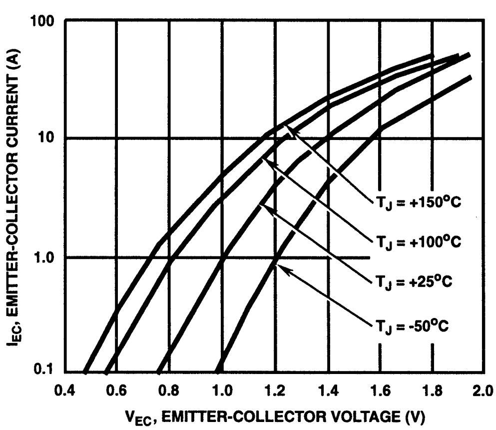


FIGURE 11. TYPICAL FORWARD VOLTAGE

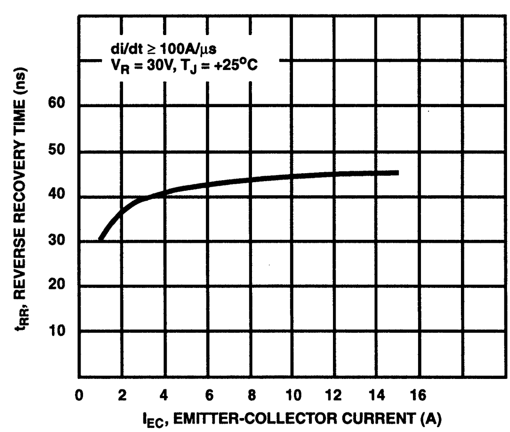


FIGURE 12. TYPICAL REVERSE RECOVERY TIME

Test Circuit

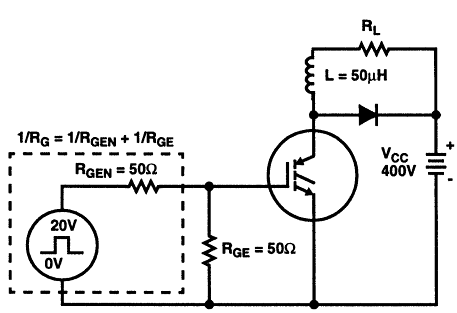


FIGURE 13. INDUCTIVE SWITCHING TEST CIRCUIT

HARRIS SEMICONDUCTOR

HGTP10N40C1, 40E1, 50C1, 50E1, HGTH12N40C1, 40E1, 50C1, 50E1

10A, 12A, 400V and 500V N-Channel IGBTs

April 1995

Features

- 10A and 12A, 400V and 500V
- $V_{CE(ON)}$: 2.5V Max.
- T_{FI}: 1µs, 0.5µs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- No Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protection Circuits

Description

The HGTH12N40C1, HGTH12N40E1, HGTH12N50C1, HGTH12N50E1, HGTP10N40C1, HGTP10N40E1, HGTP10N50C1 and HGTP10N50E1 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

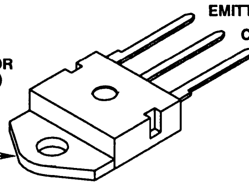
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTH12N40C1	TO-218AC	G12N40C1
HGTH12N40E1	TO-218AC	G12N40E1
HGTH12N50C1	TO-218AC	G12N50C1
HGTH12N50E1	TO-218AC	G12N50E1
HGTP10N40C1	TO-220AB	G10N40C1
HGTP10N40E1	TO-220AB	G10N40E1
HGTP10N50C1	TO-220AB	G10N50C1
HGTP10N50E1	TO-220AB	G10N50E1

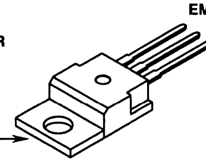
NOTE: When ordering, use the entire part number.

Packages

HGTH-TYPES JEDEC TO-218AC

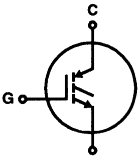


HGTP-TYPES JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

IGBTs

Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

	HGTH12N40C1 HGTH12N40E1	HGTH12N50C1 HGTH12N50E1	HGTP10N40C1 HGTP10N40E1	HGTP10N50C1 HGTP10N50E1	UNITS
Collector-Emitter Voltage . . . . . V_{CES}	400	500	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$ . . . . . V_{CGR}	400	500	400	500	V
Reverse Collector-Emitter Voltage . . . . . V_{ECS}(rev.)	15	15	-5	-5	V
Gate-Emitter Voltage . . . . . V_{GE}	±20	±20	±20	±20	V
Collector Current Continuous . . . . . I_C	12	12	10	10	A
Collector Current Pulsed . . . . . I_{CM}	17.5	17.5	17.5	17.5	A
Power Dissipation at $T_C = +25^oC$ . . . . . P_D	75	75	60	60	W
Power Dissipation Derating Above $T_C > +25^oC$	0.6	0.6	0.48	0.48	W/^{o}C
Operating and Storage Junction Temperature Range . . . T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1697.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS: HGTH12N40C1, E1, HGTP10N40C1, E1 MIN	MAX	LIMITS: HGTH12N50C1, E1, HGTP10N50C1, E1 MIN	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1mA, V_{GE} = 0	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	V_{GE} = V_{CE}, I_C = 1mA	2.0	4.5 3 (Typ)	2.0	4.5 3 (Typ)	V
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 400V, T_C = +25°C	-	250	-	-	μA
		V_{CE} = 500V, T_C = +25°C	-	-	-	250	μA
		V_{CE} = 400V, T_C = +125°C	-	1000	-	-	μA
		V_{CE} = 500V, T_C = +125°C	-	-	-	1000	μA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	-	100	-	100	nA
Collector-Emitter on Voltage	$V_{CE(ON)}$	I_C = 10A, V_{GE} = 10V	-	2.5	-	2.5	V
		I_C = 17.5A, V_{GE} = 20V	-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5A, V_{CE} = 10V	-	6 (Typ)	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 5A, V_{CE} = 10V	-	19 (Typ)	-	19 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	I_C = 10A, $V_{CE(CLP)}$ = 300V, L = 50μH, T_J = +100°C, V_{GE} = 10V, R_G = 50Ω	-	50	-	50	ns
Rise Time	t_{RI}		-	50	-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns
Fall Time	t_{FI}						
40E1, 50E1			680 (Typ)	1000	680 (Typ)	1000	ns
40C1, 50C1			400	500	400	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	I_C = 10A, $V_{CE(CLP)}$ = 300V, L = 50μH, T_J = +100°C, V_{GE} = 10V, R_G = 50Ω					
40E1, 50E1			680 (Typ)				μJ
40C1, 50C1			400 (Typ)				μJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	HGTH, HGTM	-	1.67	-	1.67	°C/W
		HGTP	-	2.083	-	2.083	°C/W

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
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4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Typical Performance Curves

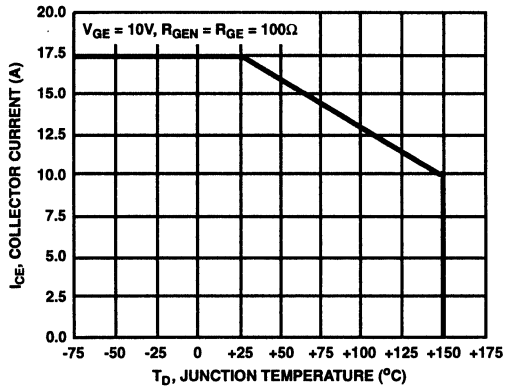


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. R_G = 50Ω, V_{GE} = 0V ARE THE MIN. ALLOWABLE VALUES

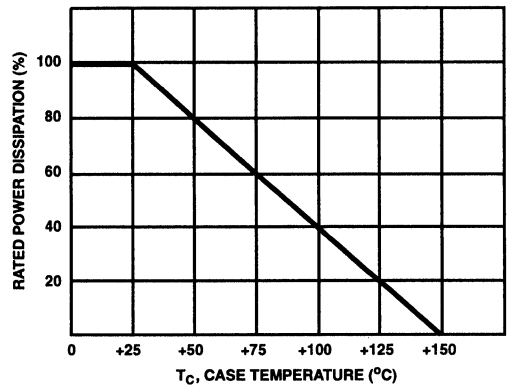


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

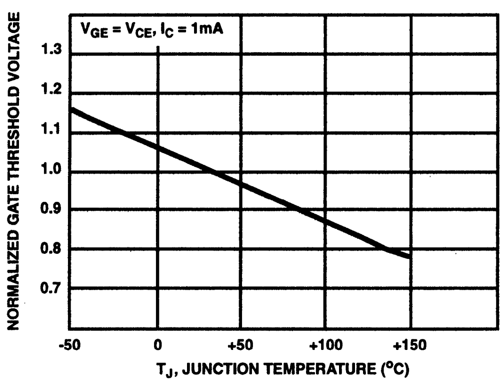


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

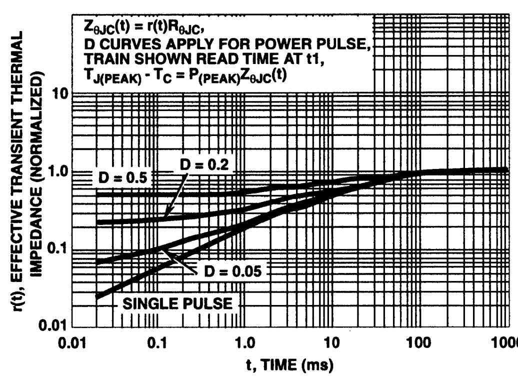


FIGURE 4. NORMALIZED THERMAL RESPONSE CHARACTERISTICS

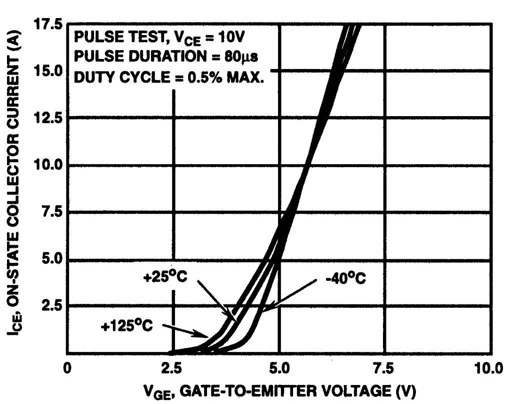


FIGURE 5. TYPICAL TRANSFER CHARACTERISTICS

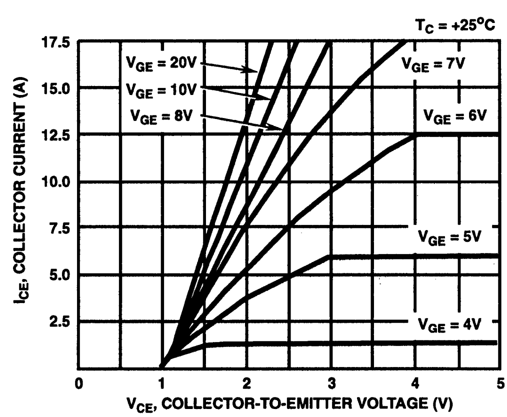


FIGURE 6. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

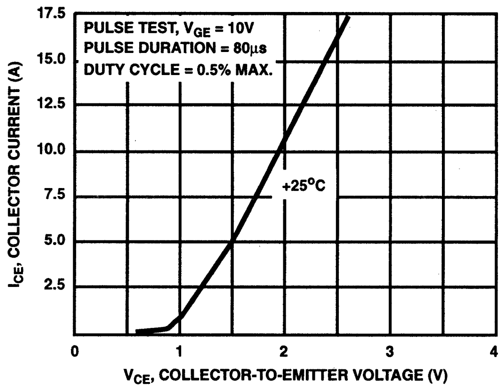


FIGURE 7. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

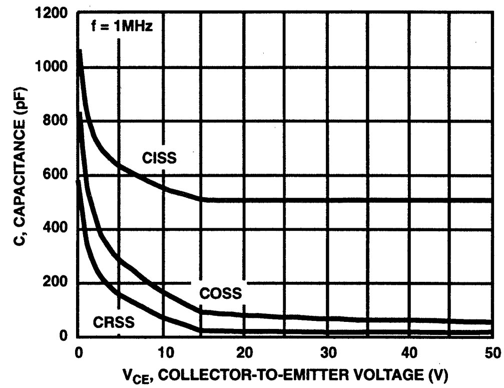


FIGURE 8. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

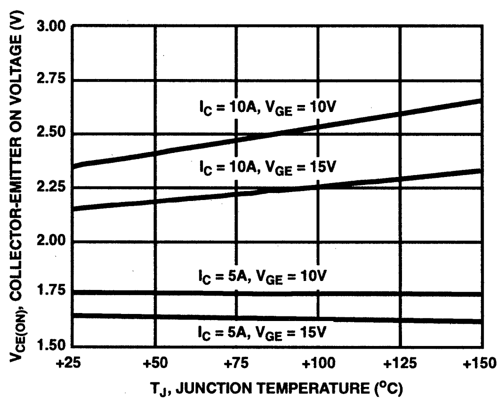


FIGURE 9. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

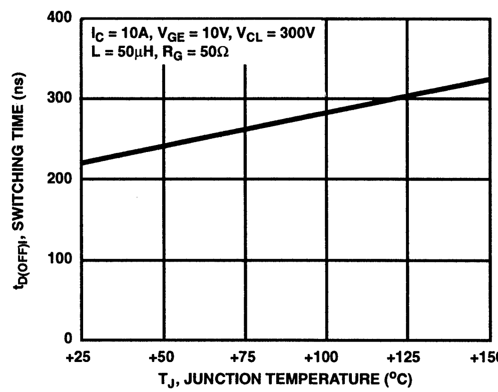


FIGURE 10. TYPICAL TURN-OFF DELAY TIME

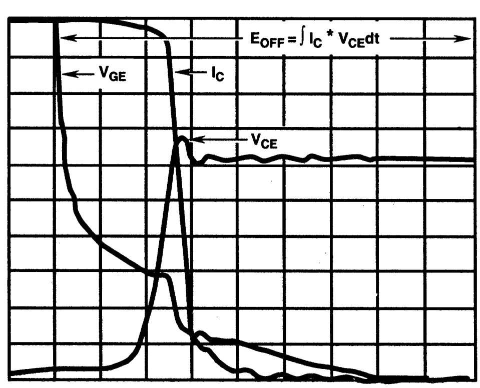


FIGURE 11. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

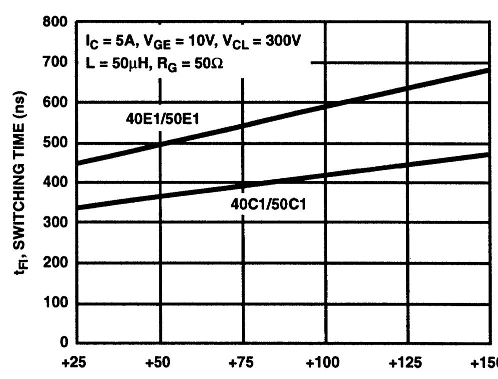


FIGURE 12. TYPICAL FALL TIME (I_C = 5A)

Typical Performance Curves (Continued)

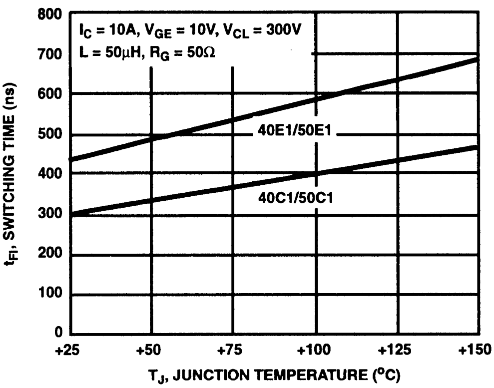


FIGURE 13. TYPICAL FALL TIME (I_C = 10A)

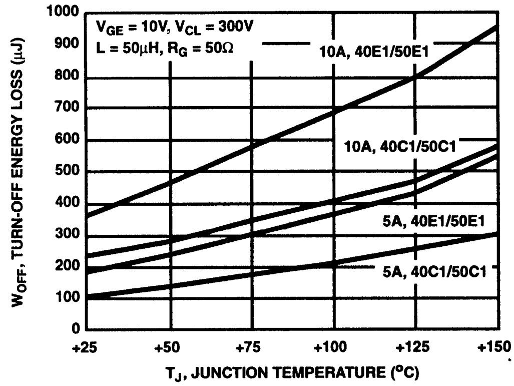


FIGURE 14. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE

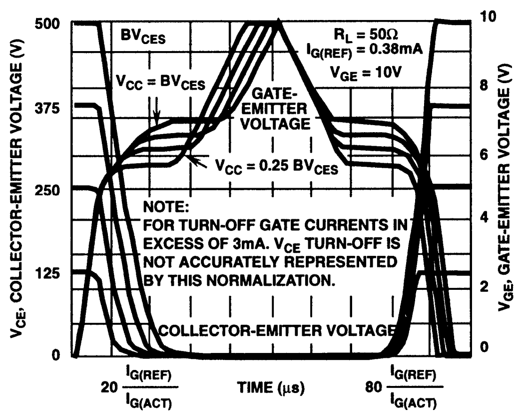


FIGURE 15. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

Test Circuit

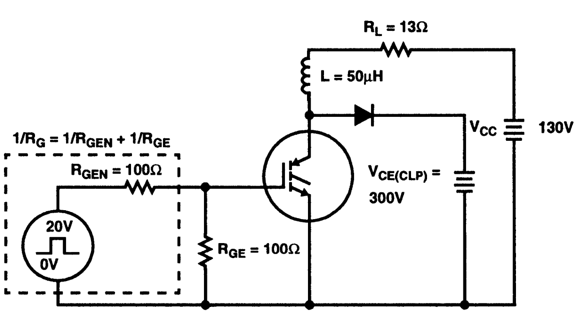


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

3

IGBTs

HARRIS SEMICONDUCTOR

HGTP10N40C1D, HGTP10N40E1D, HGTP10N50C1D, HGTP10N50E1D

10A, 400V and 500V N-Channel IGBTs with Anti-Parallel Ultrafast Diodes

April 1995

Features

- 10A, 400V and 500V
- $V_{CE(ON)}$: 2.5V Max.
- T_{FALL}: 1µs, 0.5µs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

The HGTP10N40C1D, HGTP10N40E1D, HGTP10N50C1D, and HGTP10N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

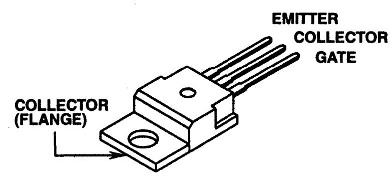
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP10N40C1D	TO-220AB	10N40C1D
HGTP10N40E1D	TO-220AB	10N40E1D
HGTP10N50C1D	TO-220AB	10N50C1D
HGTP10N50E1D	TO-220AB	10N50E1D

NOTE: When ordering, use the entire part number.

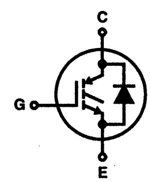
Package

JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP10N40C1D HGTP10N40E1D	HGTP10N50C1D HGTP10N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	17.5	17.5	A
at $T_C = +90^oC$	I_{C90}	10	10	
Power Dissipation Total at $T_C = +25^oC$	P_D	75	75	W
Power Dissipation Derating $T_C > +25^oC$		0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2405.5**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS HGTP10N40C1D, HGTP10N40E1D MIN	MAX	HGTP10N50C1D, HGTP10N50E1D MIN	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1mA$, $V_{GE} = 0$	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, $I_C = 1mA$	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = 400V$, $T_C = +25^oC$	-	250	-	-	µA
		$V_{CE} = 500V$, $T_C = +25^oC$	-	-	-	250	µA
		$V_{CE} = 400V$, $T_C = +125^oC$	-	1000	-	-	µA
		$V_{CE} = 500V$, $T_C = +125^oC$	-	-	-	1000	µA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$, $V_{CE} = 0$	-	100	-	100	nA
Collector-Emitter On Voltage	$V_{CE(ON)}$	$I_C = 10A$, $V_{GE} = 10V$	-	2.5	-	2.5	V
		$I_C = 17.5A$, $V_{GE} = 20V$	-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 5A$, $V_{CE} = 10V$	-	6 (Typ)	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 5A$, $V_{CE} = 10V$	-	19 (Typ)	-	19 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	$I_C = 10A$, $V_{CE(CLP)} = 300V$, $L = 50\mu H$, $T_J = +100^oC$, $V_{GE} = 10V$, $R_G = 50\Omega$	-	50	-	50	ns
Rise Time	t_{RI}		-	50	-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns
Fall Time	t_{FI}						
40E1D, 50E1D			680 (Typ)	1000	680 (Typ)	1000	ns
40C1D, 50C1D			400 (Typ)	500	400 (Typ)	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	$I_C = 10A$, $V_{CE(CLP)} = 300V$, $L = 50\mu H$, $T_J = +100^oC$, $V_{GE} = 10V$, $R_G = 50\Omega$					
40E1D, 50E1D			1810 (Typ)				µJ
40C1D, 50C1D			1070 (Typ)				µJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	1.67	-	1.67	°C/W
Diode Forward Voltage	V_{EC}	$I_{EC} = 10A$	-	2	-	2	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 10A$, di/dt = 100A/µs	-	100	-	100	ns

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Typical Performance Curves

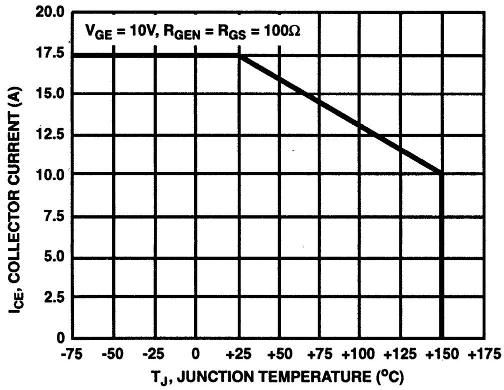


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. $R_G = 50\Omega$, $V_{GE} = 0V$ ARE THE MIN. ALLOWABLE VALUES

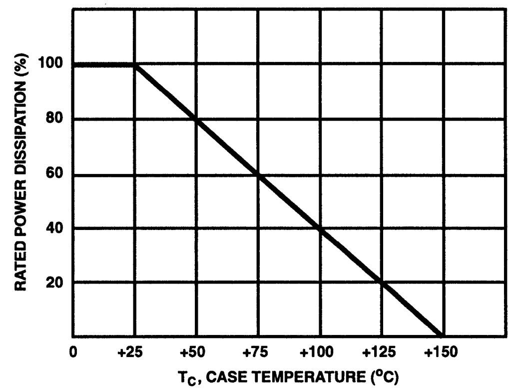


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

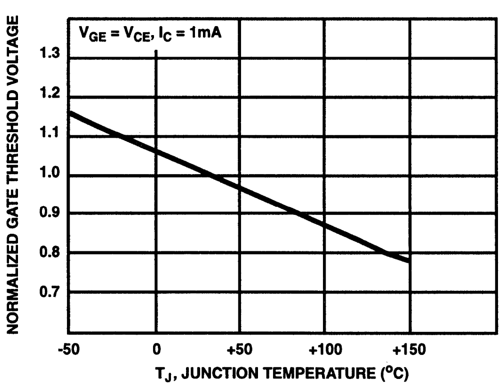


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

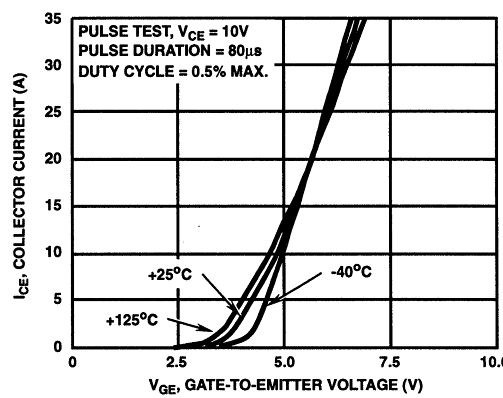


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

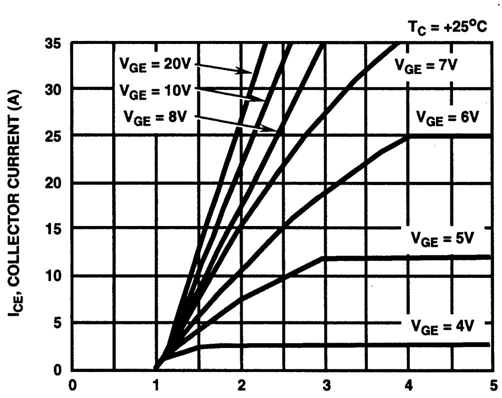


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

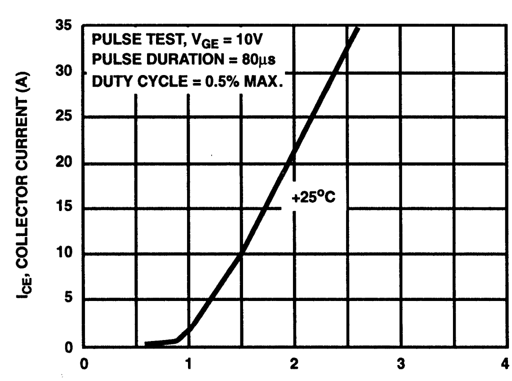


FIGURE 6. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

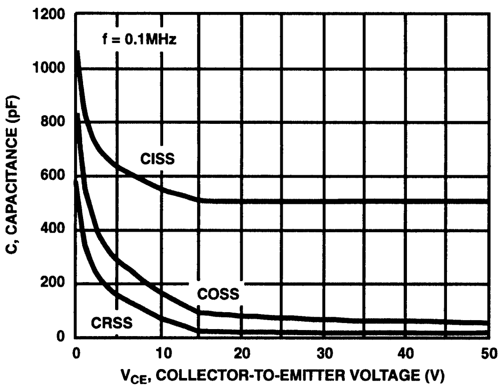


FIGURE 7. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

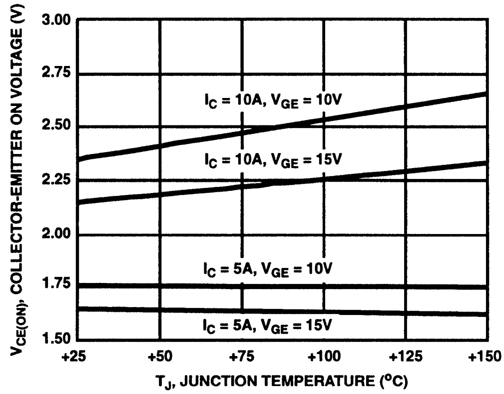


FIGURE 8. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

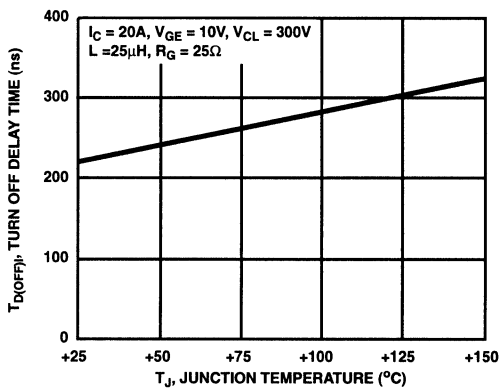


FIGURE 9. TYPICAL TURN-OFF DELAY TIME

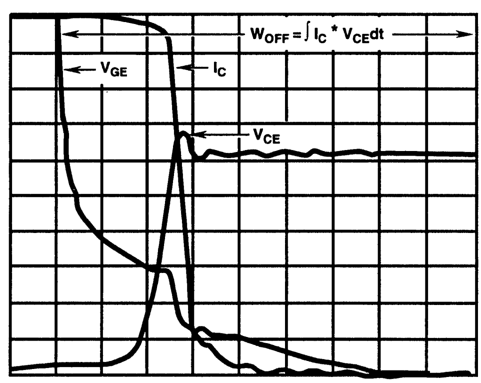


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

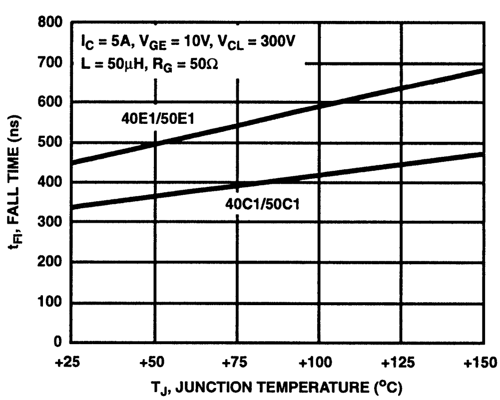


FIGURE 11. TYPICAL FALL TIME (I_C = 5A)

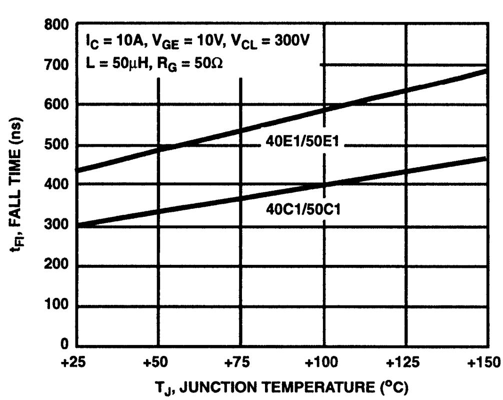


FIGURE 12. TYPICAL FALL TIME (I_C = 10A)

3

IGBTs

Typical Performance Curves (Continued)

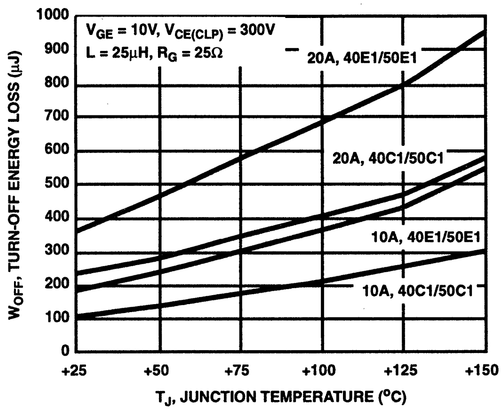


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE

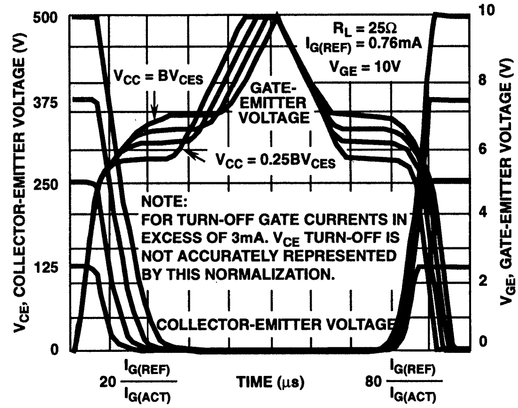


FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

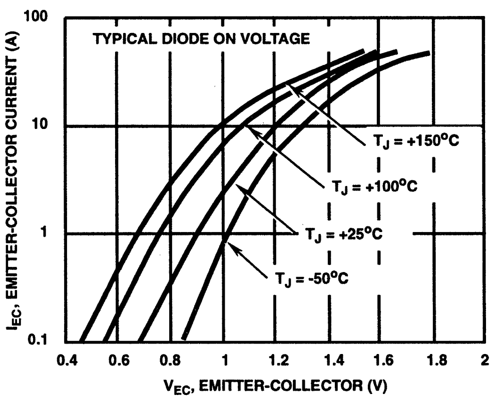


FIGURE 15. TYPICAL DIODE EMITTER-TO-COLLECTOR VOLTAGE vs CURRENT FOR ALL TYPES

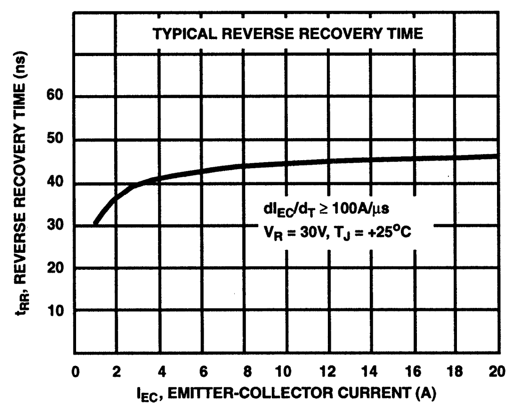


FIGURE 16. TYPICAL DIODE REVERSE-RECOVERY TIME FOR ALL TYPES

Test Circuit

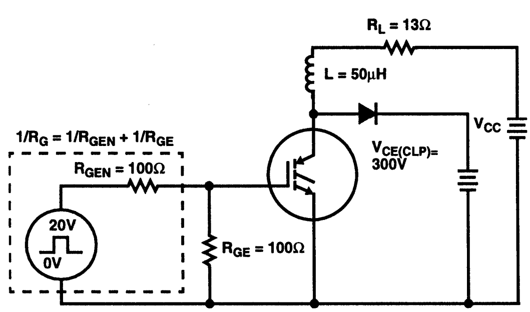


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

HGTP10N40F1D, HGTP10N50F1D

10A, 400V and 500V N-Channel IGBTs with Anti-Parallel Ultrafast Diodes

April 1995

Features

- **10A, 400V and 500V**
- **Latch Free Operation**
- **Typical Fall Time < 1.4μs**
- **High Input Impedance**
- **Low Conduction Loss**
- **Anti-Parallel Diode**
- **t_{RR} < 60ns**

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{RR} < 60ns) with soft recovery characteristic.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

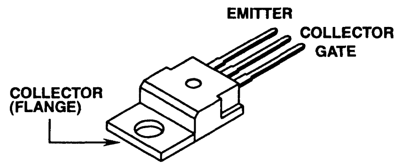
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP10N40F1D	TO-220AB	10N40F1D
HGTP10N50F1D	TO-220AB	10N50F1D

NOTE: When ordering, use the entire part number

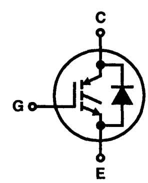
Package

JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTP10N40F1D	HGTP10N50F1D	UNITS
Collector-Emitter Voltage	BV_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	400	500	V
Collector Current Continuous at T_C = +25°C	I_{C25}	12	12	A
at T_C = +90°C	I_{C90}	10	10	A
Collector Current Pulsed (Note 1)	I_{CM}	12	12	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	±20	V
Diode Forward Current at T_C = +25°C	I_{F25}	16	16	A
at T_C = +90°C	I_{F90}	10	10	A
Power Dissipation Total at T_C = +25°C	P_D	75	75	W
Power Dissipation Derating T_C > +25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	260	°C

NOTE:

1. T_J = +150°C, Min. R_{GE} = 25Ω without latch.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			HGTP10N40F1D		HGTP10N50F1D		
			MIN	MAX	MIN	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1.25mA, V_{GE} = 0V	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, I_C = 1mA	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	T_J = +150°C, V_{CE} = 400V	-	1.25	-	-	mA
		T_J = +150°C, V_{CE} = 500V	-	-	-	1.25	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0V	-	100	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(ON)}$	T_J = +150°C, I_C = 5A, V_{GE} = 10V	-	2.5	-	2.5	V
		T_J = +150°C, I_C = 5A, V_{GE} = 15V	-	2.2	-	2.2	V
		T_J = +25°C, I_C = 5A, V_{GE} = 10V	-	2.5	-	2.5	V
		T_J = +25°C, I_C = 5A, V_{GE} = 15V	-	2.2	-	2.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 5A, V_{CE} = 10V	5.3 (Typ)				V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 5A, V_{CE} = 10V	13.4 (Typ)				nC
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, I_C = 5A, V_{CE} = 400V, R_L = 80Ω, T_J = +150°C, V_{GE} = 10V, R_G = 25Ω	45 (Typ)				ns
Rise Time	t_{RI}		35 (Typ)				ns
Turn-Off Delay Time	$t_{D(OFF)}$		130 (Typ)				ns
Fall Time	t_{FI}		1400 (Typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		0.64 (Typ)				mJ
Turn-Off Delay Time	$t_{D(OFF)I}$	Inductive Load (See Figure 13), I_C = 5A, $V_{CE(CLP)}$ = 400V, R_L = 80Ω, L = 50µH, T_J = +150°C, V_{GE} = 10V, R_G = 25Ω	-	375	-	375	ns
Fall Time	t_{FI}		-	1200	-	1200	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		-	1.2	-	1.2	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		-	1.67	-	1.67	°C/W
Thermal Resistance of Diode	$R_{\theta JC}$		-	2.0	-	2.0	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 10A	-	1.7	-	1.7	V
Diode Reverse Recovery Time	t_{RR}	I_{EC} = 10A, dI_{EC}/dt = 100A/µs	-	60	-	60	ns

Typical Performance Curves

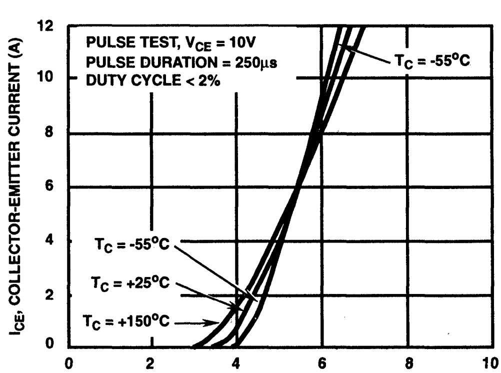


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

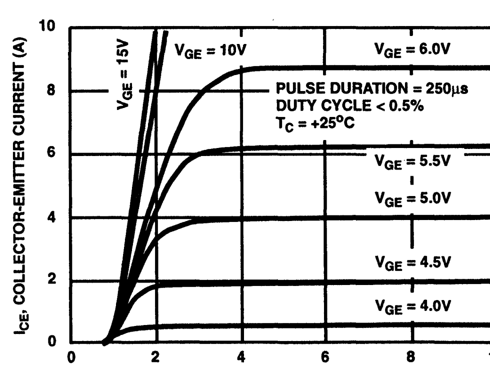


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

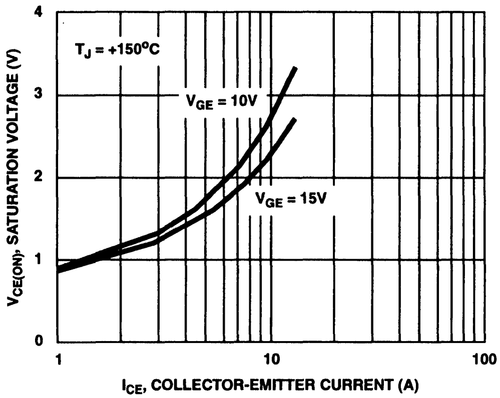


FIGURE 3. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT (TYPICAL)

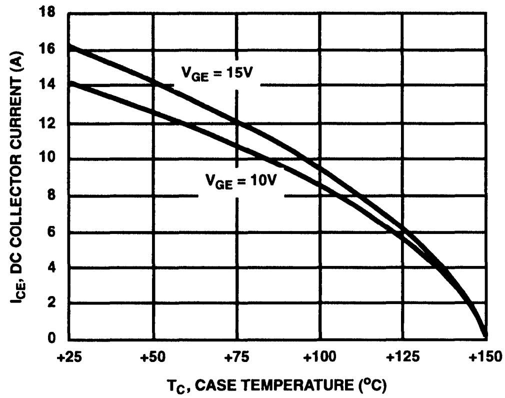


FIGURE 4. DC COLLECTOR CURRENT vs CASE TEMPERATURE

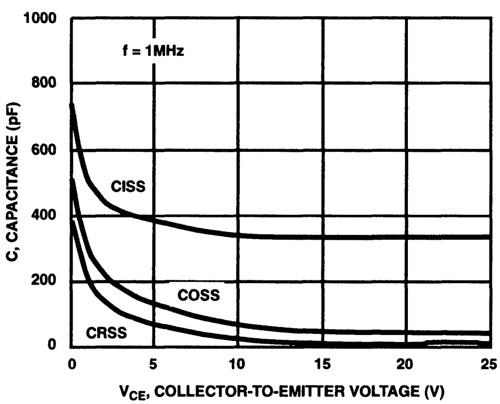


FIGURE 5. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

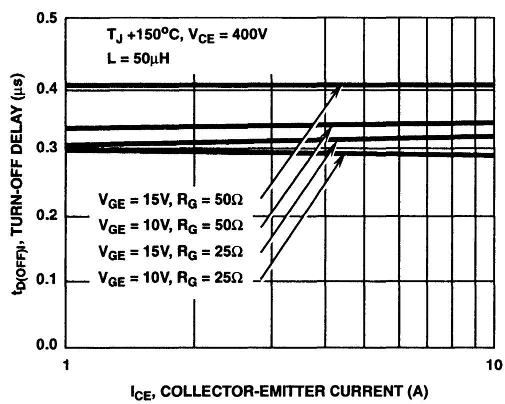


FIGURE 6. TURN-OFF DELAY vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

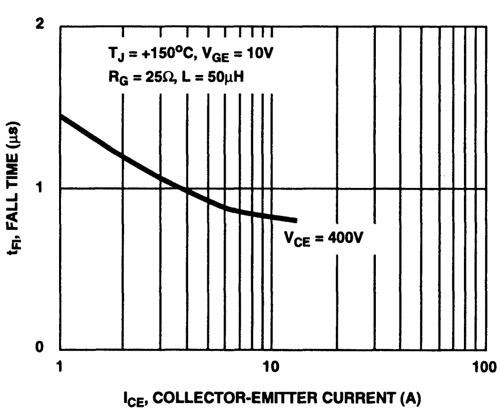


FIGURE 7. FALL TIME vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

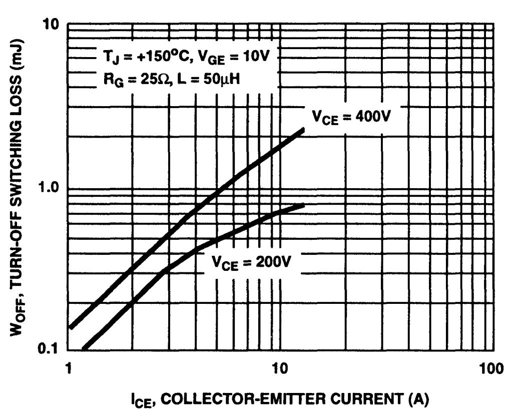


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT (TYPICAL)

Typical Performance Curves (Continued)

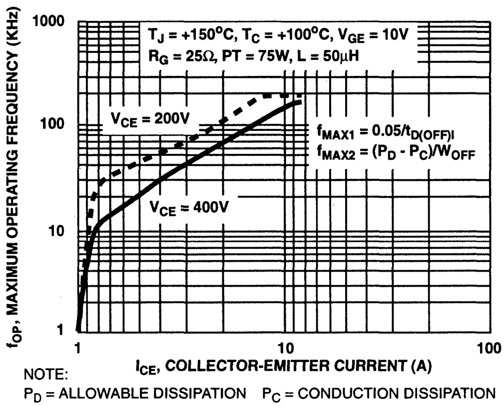


FIGURE 9. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

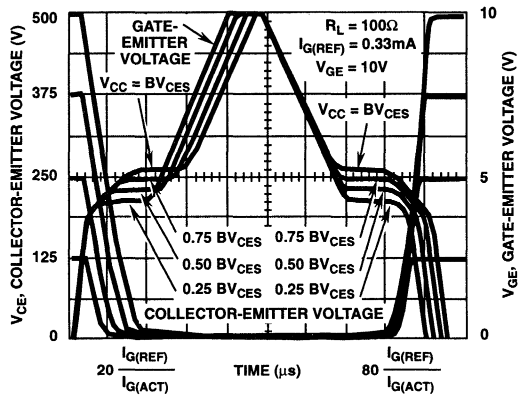


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

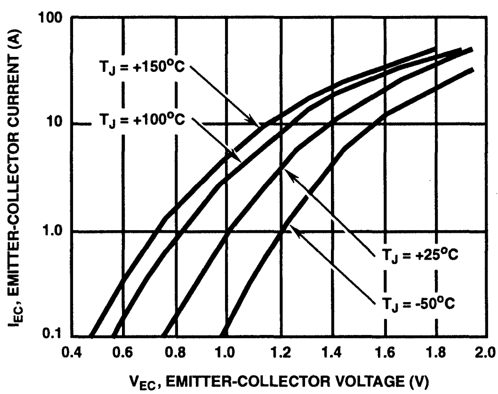


FIGURE 11. TYPICAL FORWARD VOLTAGE

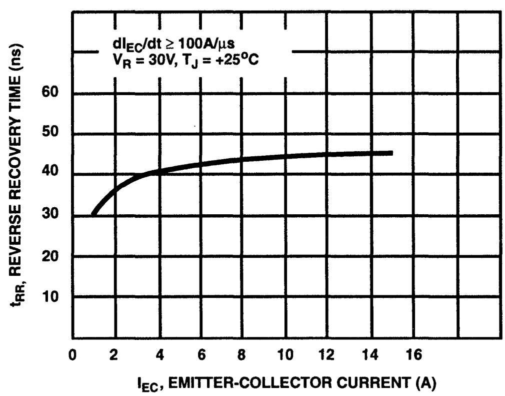


FIGURE 12. TYPICAL REVERSE RECOVERY TIME

Test Circuit

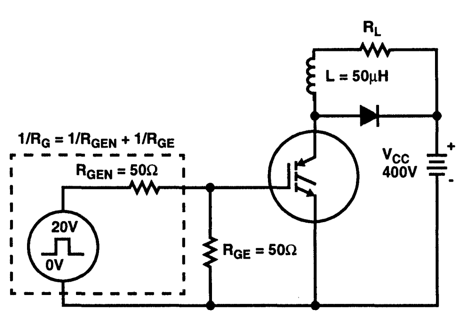


FIGURE 13. INDUCTIVE SWITCHING TEST CIRCUIT

HARRIS SEMICONDUCTOR

HGTD10N40F1, HGTD10N40F1S, HGTD10N50F1, HGTD10N50F1S

April 1995

10A, 400V and 500V N-Channel IGBTs

Features

- 10A, 400V and 500V
- $V_{CE(ON)}$ 2.5V Max.
- T_{FALL} ≤1.4μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

The HGTD10N40F1, HGTD10N40F1S, HGTD10N50F1, and HGTD10N50F1S are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low power integrated circuits.

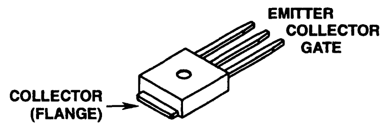
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTD10N40F1	TO-251AA	G10N40
HGTD10N50F1	TO-251AA	G10N50
HGTD10N40F1S	TO-252AA	G10N40
HGTD10N50F1S	TO-252AA	G10N50

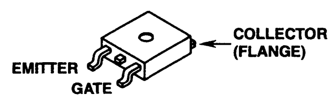
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., HGTD10N40F19A.

Packages

HGTD10N40F1, HGTD10N50F1
JEDEC TO-251AA

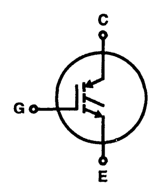


HGTD10N40F1S, HGTD10N50F1S
JEDEC TO-252AA



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTD10N40F1 HGTD10N40F1S	HGTD10N50F1 HGTD10N50F1S	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous at T_C = +25°C	I_{C25}	12	12	A
at T_C = +90°C	I_{C90}	10	10	A
Power Dissipation Total at T_C = +25°C	P_D	75	75	W
Power Dissipation Derating T_C > +25°C		0.6	0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2425.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			HGTD10N40F1 HGTD10N40F1S		HGTD10N50F1 HGTD10N50F1S		
			MIN	MAX	MIN	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, $I_C = 1mA$	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	$T_J = +150^oC$, $V_{CE} = 400V$	-	250	-	-	µA
		$T_J = +150^oC$, $V_{CE} = 500V$	-	-	-	250	µA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm20V$, $V_{CE} = 0V$	-	100	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(ON)}$	$T_J = +150^oC$, $I_C = 5A$, $V_{GE} = 10V$	-	2.5	-	2.5	V
		$T_J = +150^oC$, $I_C = 5A$, $V_{GE} = 15V$	-	2.2	-	2.2	V
		$T_J = +25^oC$, $I_C = 5A$, $V_{GE} = 10V$	-	2.5	-	2.5	V
		$T_J = +25^oC$, $I_C = 5A$, $V_{GE} = 15V$	-	2.2	-	2.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 5A$, $V_{CE} = 10V$	5.3 (Typ)				V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 5A$, $V_{CE} = 10V$	13.4 (Typ)				nC
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, $I_C = 5A$, $V_{CE} = 400V$, $R_L = 80\Omega$, $T_J = +150^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	45 (Typ)				ns
Rise Time	t_{RI}		35 (Typ)				ns
Turn-Off Delay Time	$t_{D(OFF)}$		130 (Typ)				ns
Fall Time	t_{FI}		1400 (Typ)				ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		0.64 (Typ)				mJ
Turn-Off Delay Time	$t_{D(OFF)}$	Inductive Load (See Figure 11), $I_C = 5A$, $V_{CE(CLP)} = 400V$, $R_L = 80\Omega$, $L = 50\mu H$, $T_J = +150^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	-	375	-	375	ns
Fall Time	t_{FI}		-	1200	-	1200	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}		-	1.2	-	1.2	mJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		-	1.67	-	1.67	°C/W

Typical Performance Curves

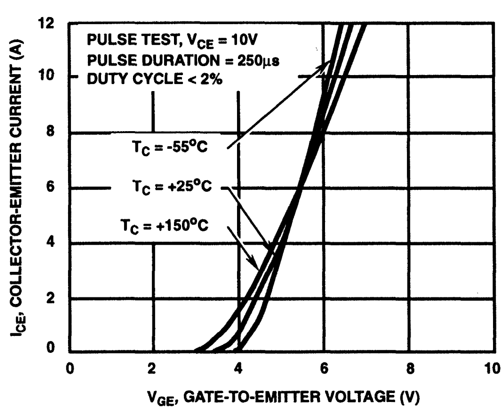


FIGURE 1. TYPICAL TRANSFER CHARACTERISTICS

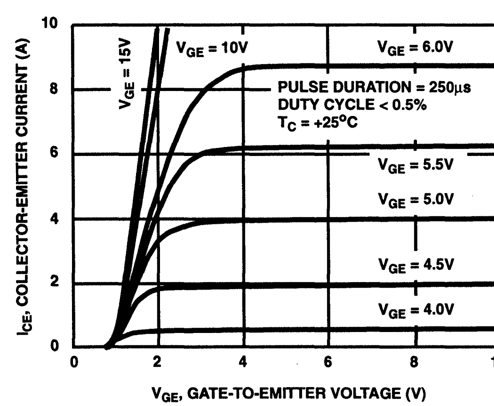


FIGURE 2. TYPICAL SATURATION CHARACTERISTICS

Typical Performance Curves (Continued)

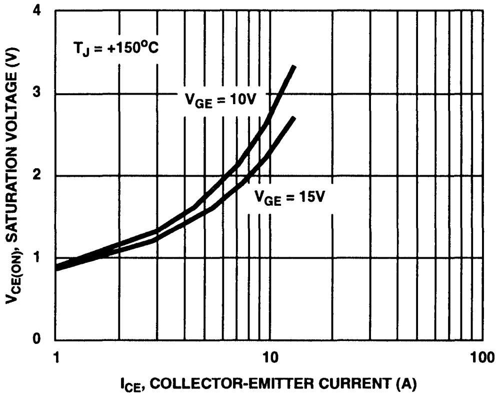


FIGURE 3. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT (TYPICAL)

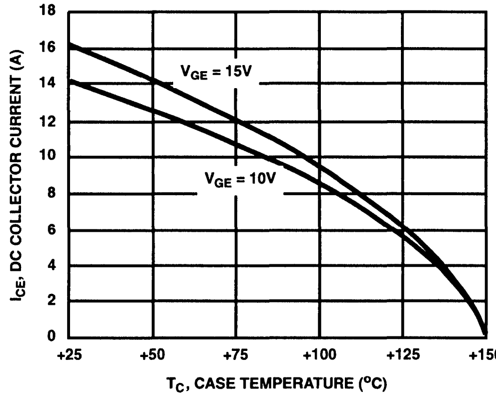


FIGURE 4. DC COLLECTOR CURRENT vs CASE TEMPERATURE

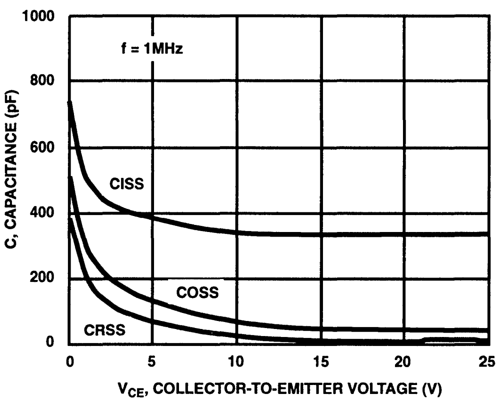


FIGURE 5. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE (TYPICAL)

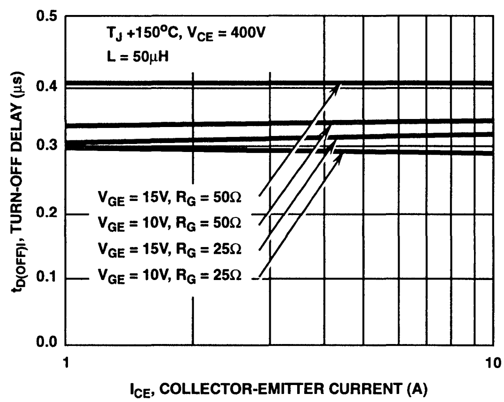


FIGURE 6. TURN-OFF DELAY vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

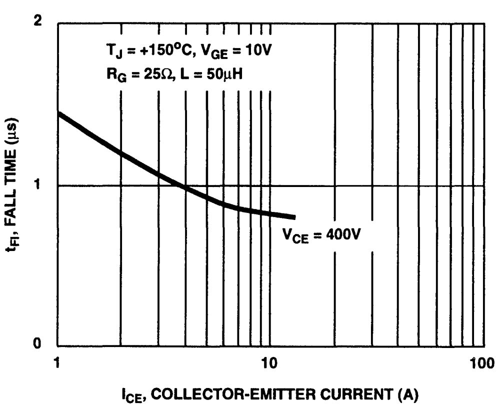


FIGURE 7. FALL TIME vs COLLECTOR-TO-EMITTER CURRENT (TYPICAL)

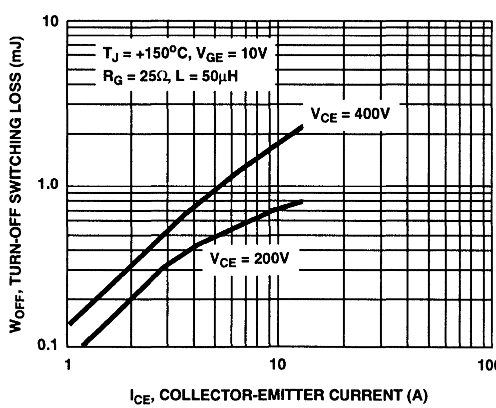
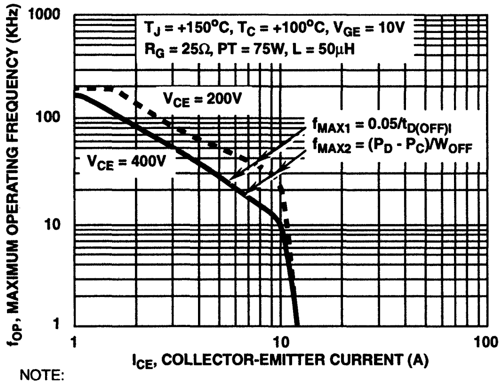


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT (TYPICAL)

3

IGBTs

Typical Performance Curves (Continued)



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 9. MAXIMUM OPERATING FREQUENCY vs COLLECTOR CURRENT AND VOLTAGE (TYPICAL)

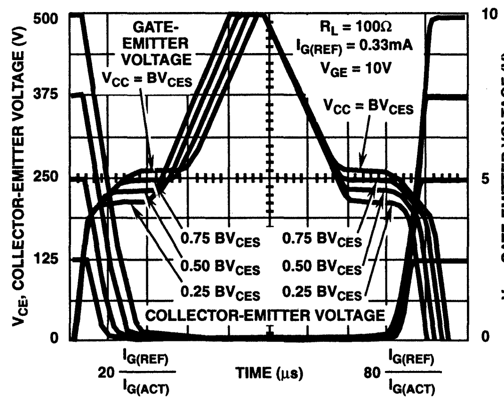


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT

Test Circuit

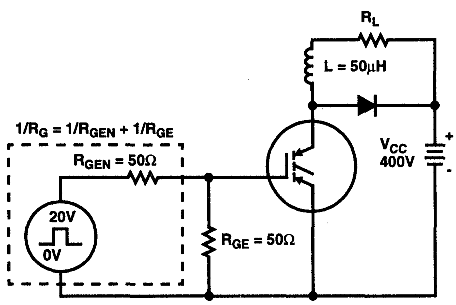


FIGURE 11. INDUCTIVE SWITCHING TEST CIRCUIT

HARRIS SEMICONDUCTOR

HGTH12N40C1D, HGTH12N40E1D, HGTH12N50C1D, HGTH12N50E1D

12A, 400V and 500V N-Channel IGBTs with Anti-Parallel Ultrafast Diodes

April 1995

Features

- 12A, 400V and 500V
- $V_{CE(ON)}$: 2.5V Max.
- T_{FALL}: 1μs, 0.5μs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protective Circuits

Description

The HGTH12N40C1D, HGTH12N40E1D, HGTH12N50C1D, and HGTH12N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

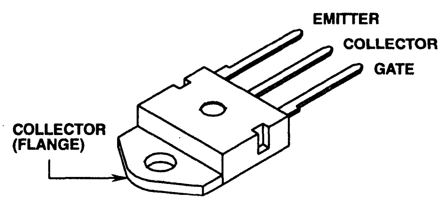
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTH12N40C1D	TO-218AC	G12N40C1D
HGTH12N40E1D	TO-218AC	G12N40E1D
HGTH12N50C1D	TO-218AC	G12N50C1D
HGTH12N50E1D	TO-218AC	G12N50E1D

NOTE: When ordering, use the entire part number

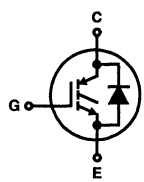
Package

JEDEC TO-218AC



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTH12N40C1D HGTH12N40E1D	HGTH12N50C1D HGTH12N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous	I_C	12	12	A
Collector Current Pulsed	I_{CM}	17.5	17.5	A
Power Dissipation Total at $T_C = +25^oC$	P_D	75	75	W
Power Dissipation Derating $T_C > +25^oC$		0.6	0.6	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	^{o}C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2273.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS HGTH12N40C1D, HGTH12N40E1D MIN	MAX	HGTH12N50C1D, HGTH12N50E1D MIN	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1mA, V_{GE} = 0$	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}, I_C = 1mA$	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = 400V, T_C = +25^oC$	-	250	-	-	μA
		$V_{CE} = 500V, T_C = +25^oC$	-	-	-	250	μA
		$V_{CE} = 400V, T_C = +125^oC$	-	1000	-	-	μA
		$V_{CE} = 500V, T_C = +125^oC$	-	-	-	1000	μA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm20V, V_{CE} = 0$	-	100	-	100	nA
Collector-Emitter On Voltage	$V_{CE(ON)}$	$I_C = 10A, V_{GE} = 10V$	-	2.5	-	2.5	V
		$I_C = 17.5A, V_{GE} = 20V$	-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 5A, V_{CE} = 10V$	-	6 (Typ)	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 5A, V_{CE} = 10V$	-	19 (Typ)	-	19 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	$I_C = 10A, V_{CE(CLP)} = 300V$, $L = 50\mu H, T_J = +100^oC$, $V_{GE} = 10V, R_G = 50\Omega$ (Note 9)	-	50	-	50	ns
Rise Time	t_{RI}		-	50	-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns
Fall Time	t_{FI}						
40E1D, 50E1D			680 (Typ)	1000	680 (Typ)	1000	ns
40C1D, 50C1D			400 (Typ)	500	400 (Typ)	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	$I_C = 10A, V_{CE(CLP)} = 300V$, $L = 50\mu H, T_J = +100^oC$, $V_{GE} = 10V, R_G = 50\Omega$					
40E1D, 50E1D			1810 (Typ)				μJ
40C1D, 50C1D			1070 (Typ)				μJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	1.67	-	1.67	$^oC/W$
Diode Forward Voltage	V_{EC}	$I_{EC} = 10A$	-	2	-	2	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 10A, dI_{EC}/dt = 100A/\mu s$	-	100	-	100	ns

Typical Performance Curves

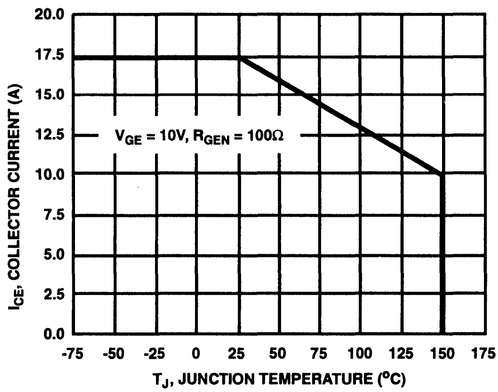


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. R_G = 50Ω, V_{GE} = 0V ARE THE MIN. ALLOWABLE VALUES

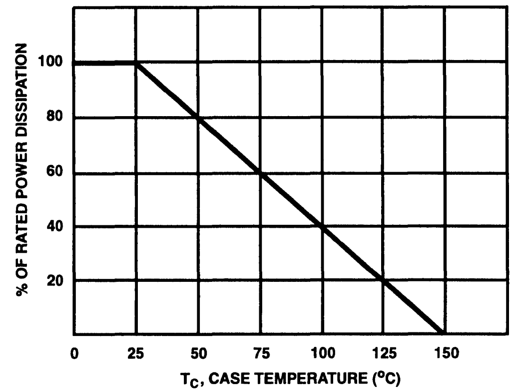


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

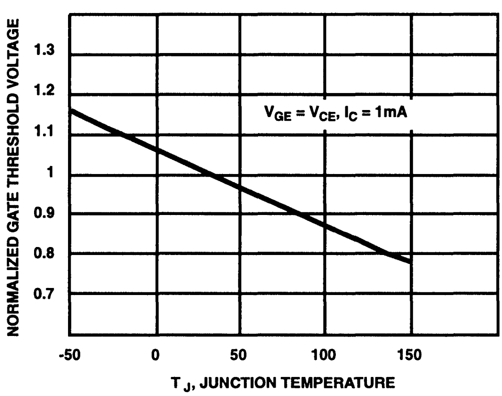


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

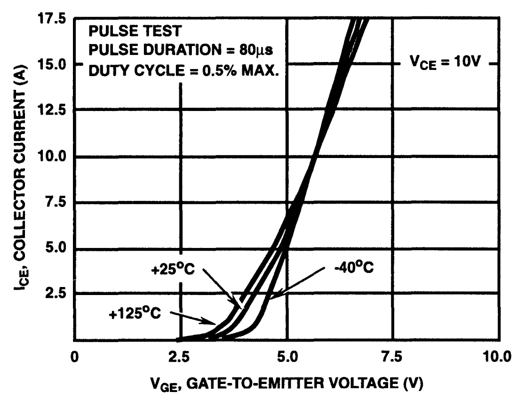


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

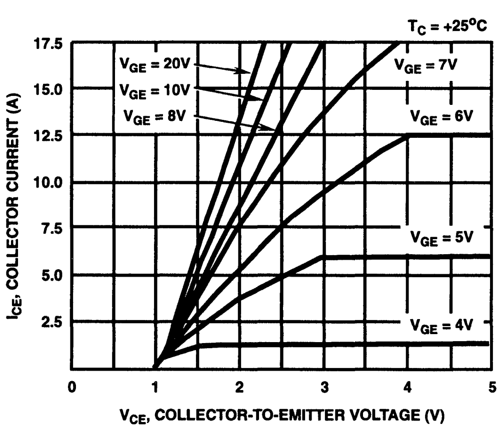


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

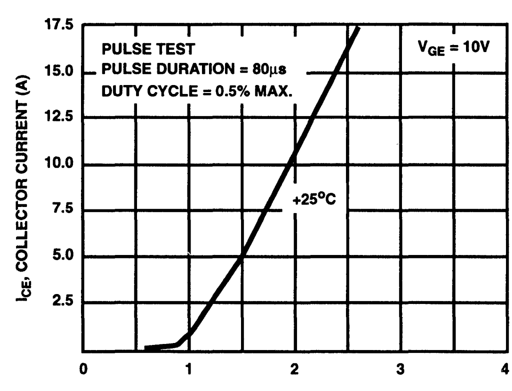


FIGURE 6. TYPICAL COLLECTOR-TO-EMITTER ON VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

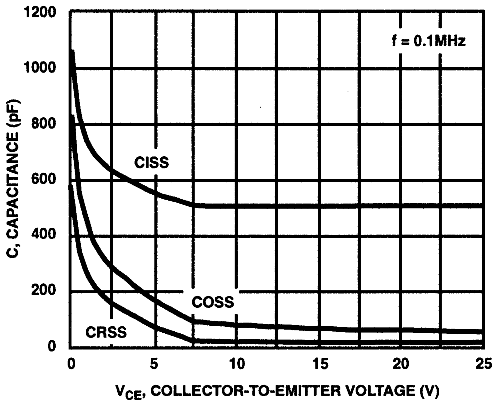


FIGURE 7. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

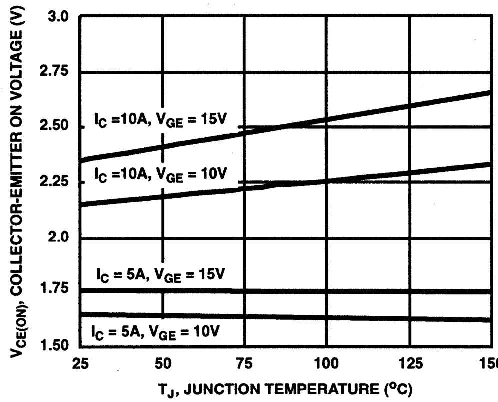


FIGURE 8. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

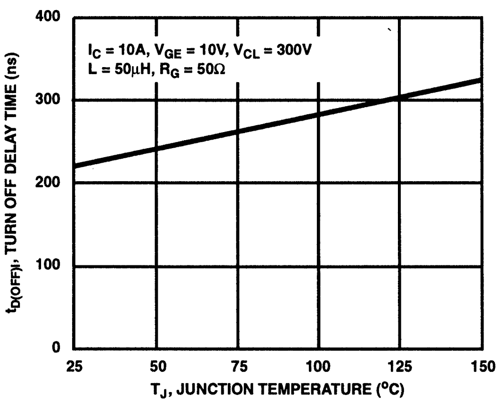


FIGURE 9. TYPICAL TURN-OFF DELAY TIME

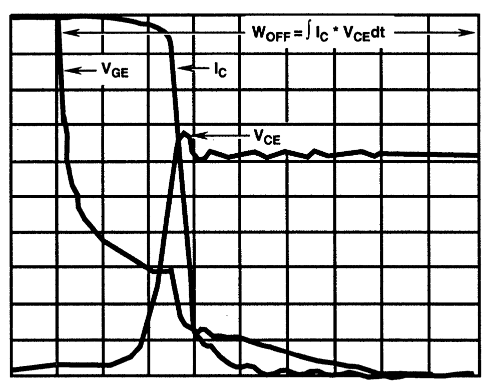


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

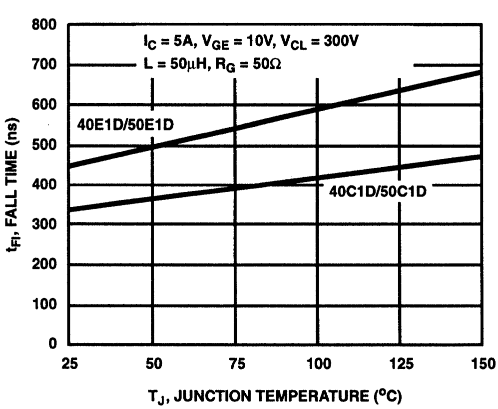


FIGURE 11. TYPICAL FALL TIME (I_C = 5A)

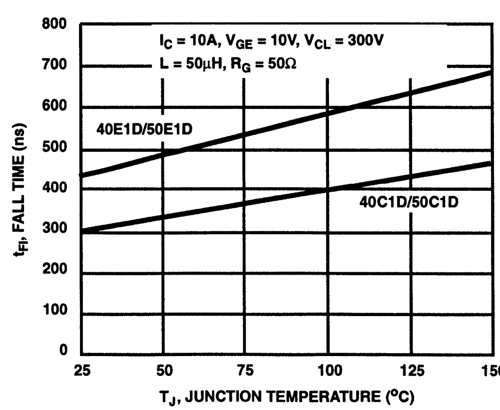


FIGURE 12. TYPICAL FALL TIME (I_C = 10A)

Typical Performance Curves (Continued)

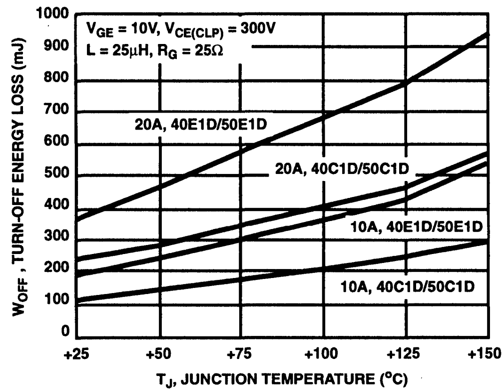


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE

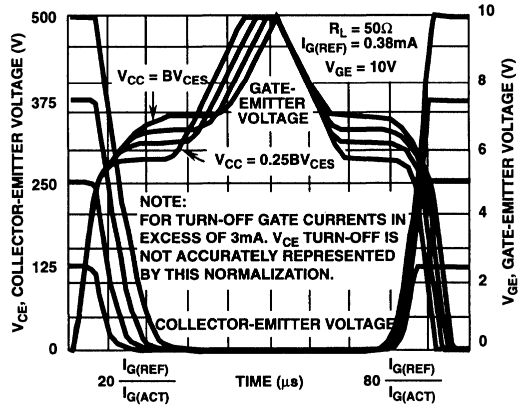


FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

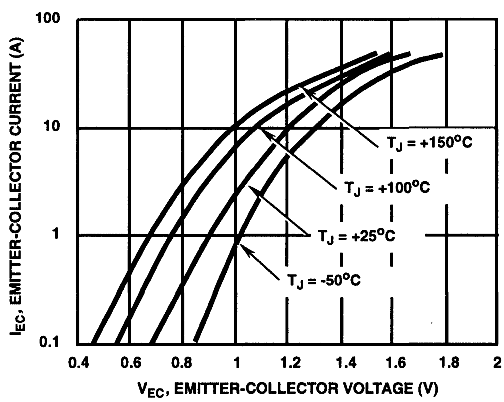


FIGURE 15. TYPICAL DIODE EMITTER-TO-COLLECTOR VOLTAGE vs CURRENT

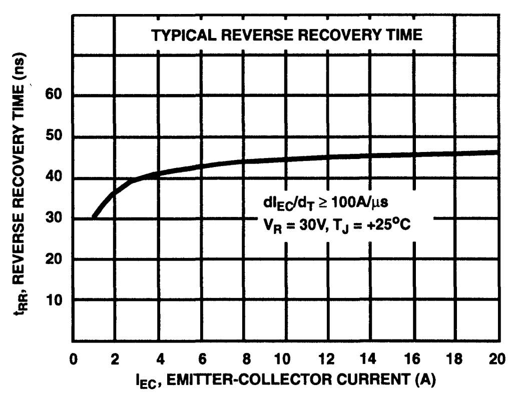


FIGURE 16. TYPICAL DIODE REVERSE RECOVERY TIME

Test Circuit

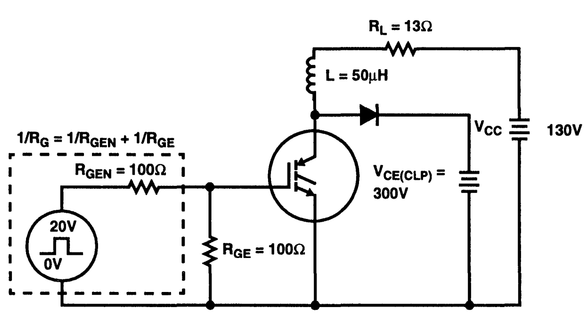


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

3

IGBTs

HARRIS SEMICONDUCTOR

HGTP12N60D1

April 1995

12A, 600V N-Channel IGBT

Features

- 12A, 600V
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

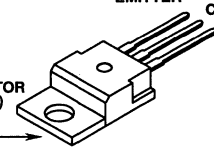
The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP12N60D1	TO-220AB	G12N60D1

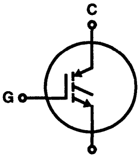
Package

JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP12N60D1	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	21	A
at $V_{GE} = 15V$ at $T_C = +90^oC$	I_{C90}	12	A
Collector Current Pulsed (Note 1)	I_{CM}	48	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at $T_J = +150^oC$	SSOA	30A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25^oC$	P_D	75	W
Power Dissipation Derating $T_C > +25^oC$		0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2830.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	T_C = +25°C	-	-	1.0	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, V_{GE} = 15V	T_C = +25°C	-	1.9	2.5	V
			T_C = +125°C	-	2.1	2.7	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, $V_{CE} = V_{GE}$, T_C = +25°C		3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, V_{CE} = 0.5 BV_{CES}		-	7.2	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	45	60	nC
			V_{GE} = 20V	-	70	90	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 500μH, $I_C = I_{C90}$, R_G = 25Ω, V_{GE} = 15V, T_J = +150°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off	$t_{D(OFF)I}$			-	430	600	ns
Current Fall Time	t_{FI}			-	430	600	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	1.8	-	mJ
Thermal Resistance IGBT	$R_{\theta JC}$			-	-	1.67	°C/W

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). The HGTP12N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

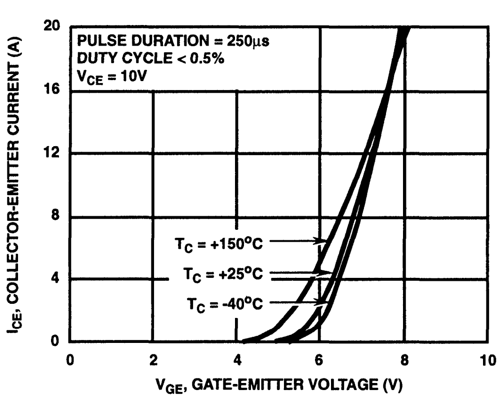


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

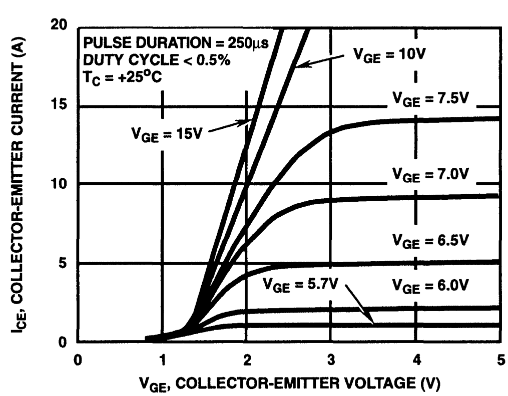


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

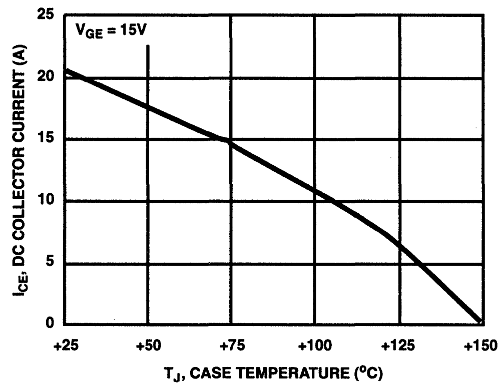


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

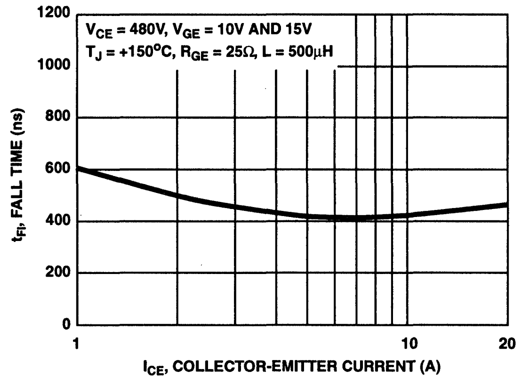


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

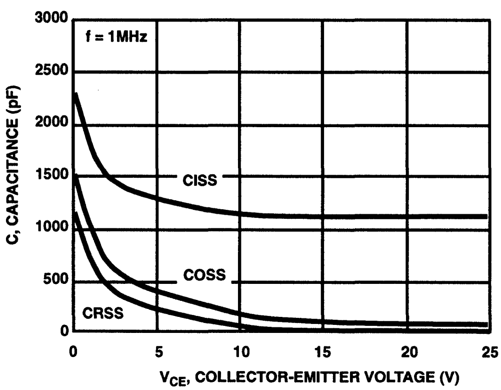


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

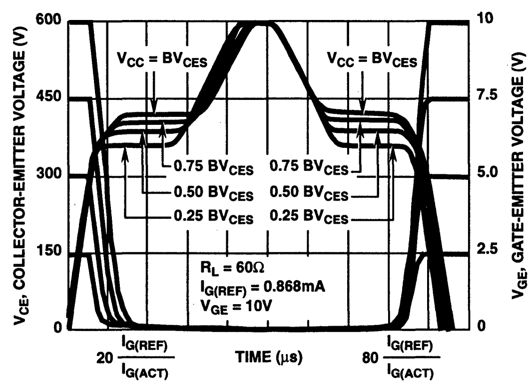


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

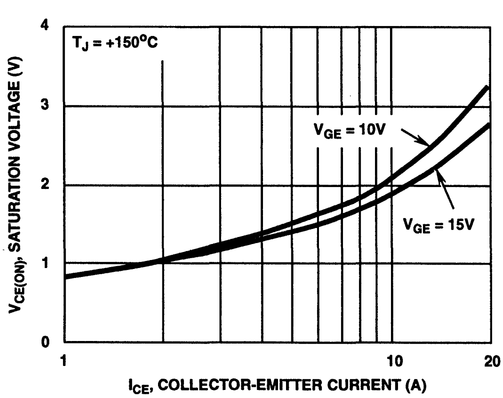


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

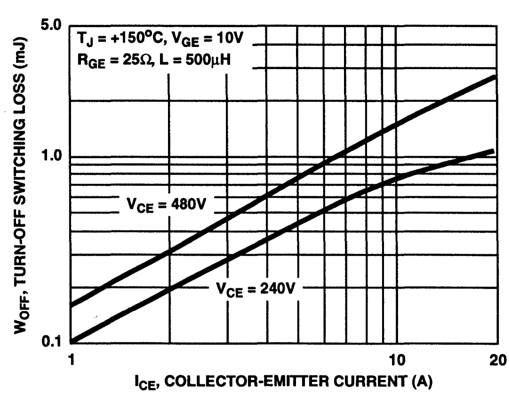


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

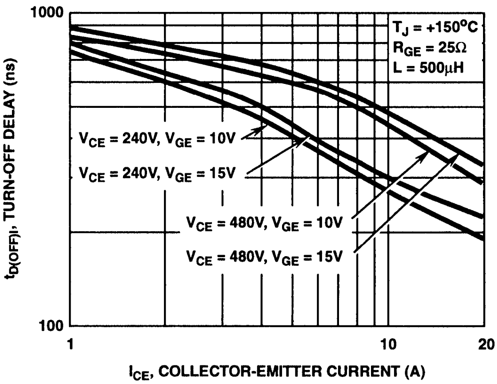
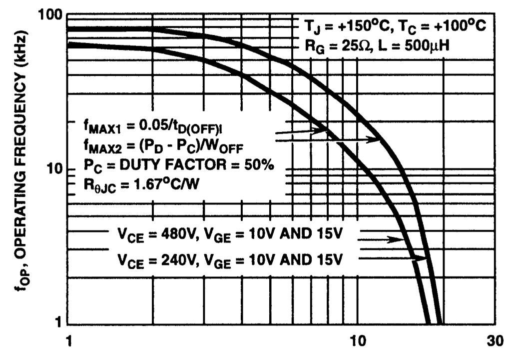


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR HGTB12N60D1C

April 1995

12A, 600V Current Sensing N-Channel IGBT

Features

- 12A, 600V
- $r_{DS(ON)}$ 0.27Ω
- Low $V_{CE(SAT)}$ at 25A .... 2.5V (Typ)
- Ultra-Fast Turn-On .... 100ns (Typ)
- Polysilicon MOS Gate - Voltage Controlled Turn On/Off
- High Current Handling at +100°C........................... 10A
- Current Sensing Pilot

Description

The HGTB12N60D1C Insulated-Gate Bipolar Transistor is a MOS-gate turn on/off power switching device combining the best advantages of power MOSFETs and bipolar transistors, and current sensing pilots. The result is a device that has the high input impedance of MOSFETs and the low on-state conduction losses similar to bipolar transistors. The device design and gate characteristics of the IGBT are also similar to power MOSFETs. An important difference is the equivalent $r_{DS(ON)}$ drain resistance which is modulated to a low value (ten times lower) when the gate is turned on. The much lower on-state voltage drop also varies only moderately between +25°C and +150°C, offering extended power handling capability.

The IGBT is ideal for many high-voltage switching applications operating at low frequencies and where low conduction losses are essential, such as AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

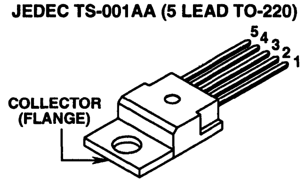
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTB12N60D1C	TS-001AA	12N60D1C

NOTE: When ordering, use the entire part number.

Package

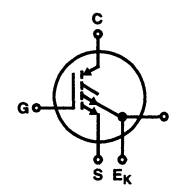
JEDEC TS-001AA (5 LEAD TO-220)



1 - GATE
2 - SENSE
3 - COLLECTOR
4 - (KELVIN) EMITTER
5 - EMITTER

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTB12N60D1C	UNITS
Collector-Emitter Voltage (V_{GE} = 0V)	V_{CES}	600	V
Collector-Gate Voltage (R_{GE} = 1MΩ)	V_{CGR}	600	V
Collector Current Continuous at T_C = +100°C	I_C	12	A
at T_C = +25°C	I_C	18	A
Collector Current Pulsed (Note 1)	I_{CM}	40	A
Gate-Emitter Voltage	V_{GE}	±25	V
Power Dissipation Total at T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering (1/8 inch from case for 5s)	T_L	260	°C

NOTE: 1. Repetitive Rating: Pulse width limited by maximum junction temperature. Gate control turn-off not allowed above 50A.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2326.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
OFF CHARACTERISTICS							
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 25μA, V_{GE} = 0V		600	-	-	V
Collector Cut-Off Current	I_{CES}	T_C = +25°C, V_{GE} = 0V, V_{CE} = Maximum Rating		-	-	250	μA
		T_C = +150°C, V_{GE} = 0V, V_{CE} = Maximum Rating x 0.8 (Note 1)		-	-	4	mA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(TH)}$	V_{CE} = V_{GE}, I_C = 250μA	T_C = +25°C	2	4	5	V
			T_C = +150°C	-	2.5	-	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	V_{GE} = 15V, I_C = 10A, T_C = +25°C		-	2.5	2.7	V
		V_{GE} = 15V, I_C = 10A, T_C = +150°C		-	2.8	-	V
		V_{GE} = 10V, I_C = 10A, T_C = +25°C		-	2.9	-	V
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{IES}	V_{GE} = 0V, V_{CE} = 25V, f = 1MHz		-	1050	-	pF
Output Capacitance	C_{OES}			-	340	-	pF
Reverse Transfer Capacitance	C_{RES}			-	10	-	pF
SWITCHING CHARACTERISTICS (See Figures 8 and 9) (Note 2)							
Turn-On Delay Time	$t_{D(ON)}$	Resistive Load, T_J = +125°C, I_C = 10A, V_{CE} = 500V, V_{GE} = 15V, $R_{G(ON)}$ = 50Ω, $R_{G(OFF)}$ = 100Ω		-	100	-	ns
Rise Time	t_R			-	100	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	0.4	-	μs
Fall Time	t_F			-	2.5	-	μs
Turn-Off Delay Time	$t_{D(OFF)I}$	Inductive Load, T_J = +125°C, L=45μH, I_C=10A, $V_{CE(CLAMP)}$=500V, V_{GE} = 15V, $R_{G(ON)}$ = 50Ω, $R_{G(OFF)}$ = 100Ω		-	0.8	1.2	μs
Fall Time	t_{FI}			-	0.8	1.0	μs
Equivalent Fall Time	$t_{F(EQ)}$			-	0.6	0.8	μs
Turn-Off Switching Losses	W_{OFF}			-	1.6	2.0	mJ
PILOT CHARACTERISTICS (Notes 2, 3 and 4)							
Pilot-Emitter Kelvin Voltage	V_{PEK}	V_{GE} = 15V_{DC}, R_P = 2kΩ					
I_C = 5A				-	1.25	-	V
I_C = 10A				1.4	1.67	1.8	V
I_C = 20A				-	2.06	-	V

NOTES:

1. Applies for 3.3°C per watt maximum thermal resistance, case-to-ambient.
2. Pulse test: Pulse widths ≤ 300μs, duty cycle ≤ 2%.
3. Refer to Figure 10.
4. When not in use connect S to emitter.

Typical Performance Curves

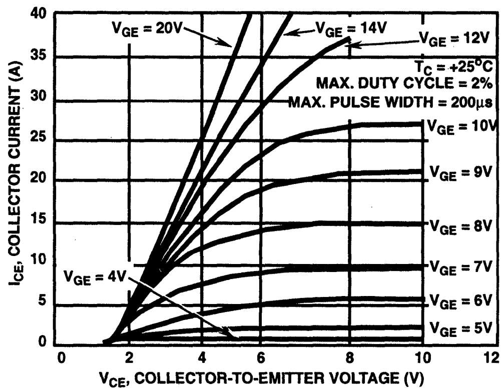


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

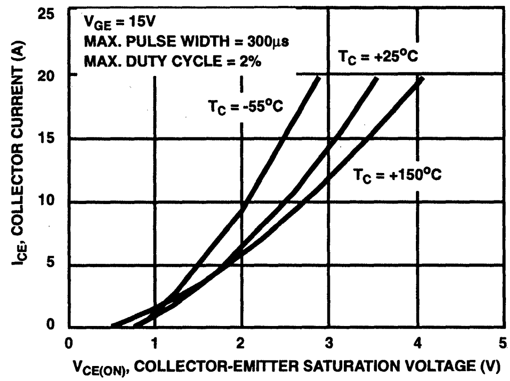


FIGURE 2. TYPICAL COLLECTOR-EMITTER SATURATION VOLTAGE

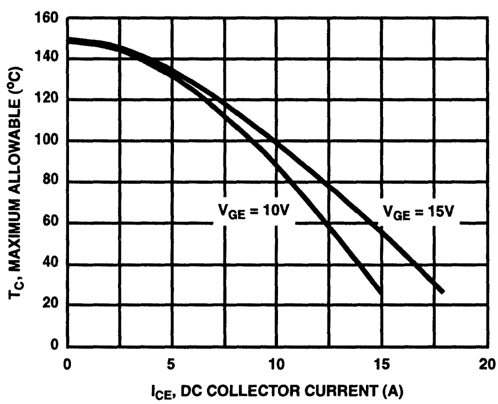
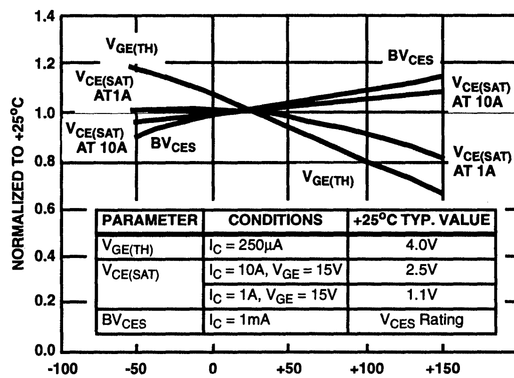


FIGURE 3. MAXIMUM ALLOWABLE CASE TEMPERATURE vs DC COLLECTOR CURRENT



PARAMETER	CONDITIONS	+25°C TYP. VALUE
$V_{GE(TH)}$	I_C = 250μA	4.0V
$V_{CE(SAT)}$	I_C = 10A, V_{GE} = 15V	2.5V
	I_C = 1A, V_{GE} = 15V	1.1V
BV_{CES}	I_C = 1mA	V_{CES} Rating

FIGURE 4. TYPICAL TEMPERATURE DEPENDENCE OF PARAMETERS

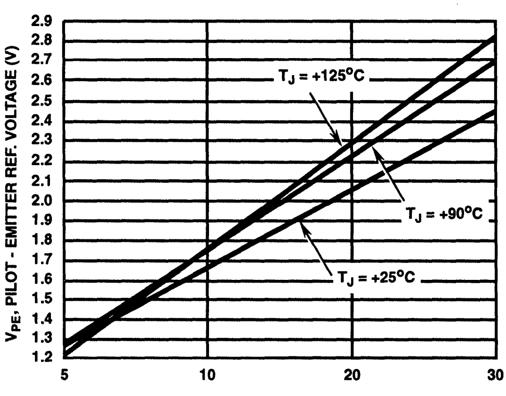


FIGURE 5. TYPICAL EMITTER PILOT CHARACTERISTICS 2kΩ PILOT RESISTOR

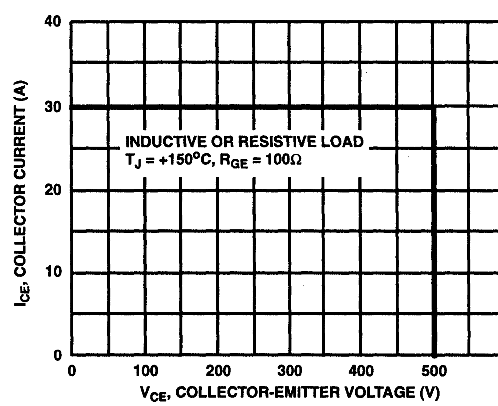


FIGURE 6. TURN-OFF SAFE OPERATING AREA

Typical Performance Curves (Continued)

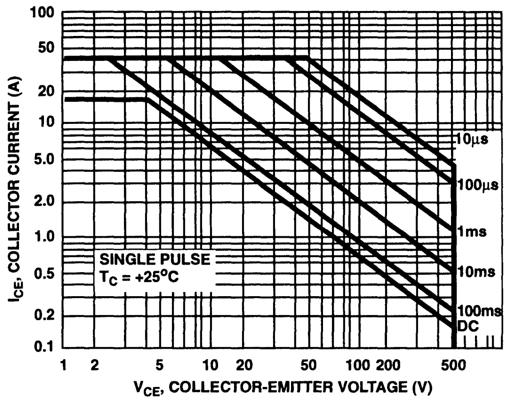


FIGURE 7. TURN-ON SAFE OPERATING AREA

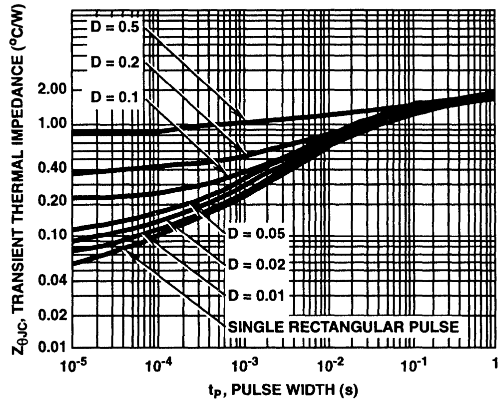
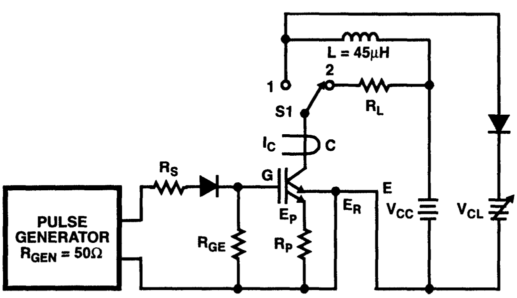


FIGURE 8. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

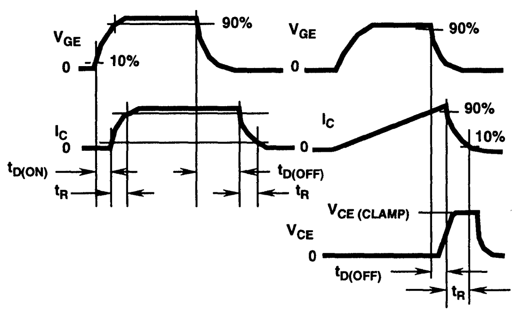


S1 SWITCH POSITION 1 CLAMPED INDUCTIVE LOAD
2 RESISTIVE LOAD

$R_{G(ON)} = \frac{(R_{GEN} + R_S)(R_{GE})}{R_{GEN} + R_S + R_{GE}}$ PULSE WIDTH 60µs V_{CC}

L-$I_{C\ MAXIMUM}$, PULSE WIDTH

FIGURE 9. BASIC SWITCHING TEST CIRCUIT



RESISTIVE LOAD INDUCTIVE LOAD

(WAVEFORMS NOT TO SCALE)

FIGURE 10. SWITCHING WAVEFORMS

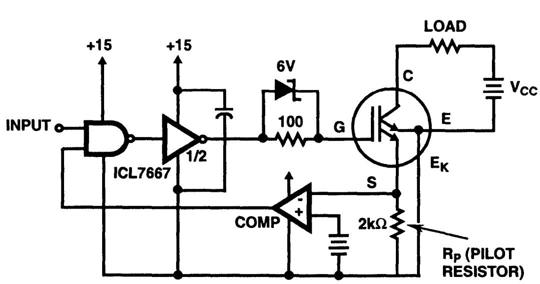


FIGURE 11. TYPICAL CIRCUIT UTILIZING THE EMITTER PILOT FOR OVERCURRENT PROTECTION

HARRIS SEMICONDUCTOR

HGTG12N60D1D

12A, 600V N-Channel IGBT with Anti-Parallel Ultrafast Diode

April 1995

Features

- 12A, 600V
- Latch Free Operation
- Typical Fall Time <500ns
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{RR} < 60ns

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{RR} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

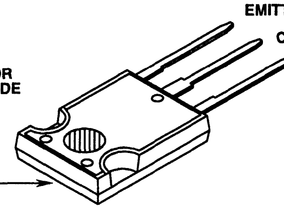
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG12N60D1D	TO-220AB	G12N60D1D

NOTE: When ordering, use the entire part number

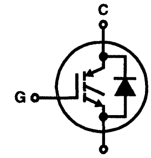
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTG12N60D1D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous at T_C = +25°C	I_{C25}	21	A
at T_C = +90°C	I_{C90}	12	A
Collector Current Pulsed (Note 1)	I_{CM}	48	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Switching Safe Operating Area at T_J = +150°C	SSOA	30A at 0.8 BV_{CES}	-
Diode Forward Current at T_C = +25°C	I_{F25}	21	A
at T_C = +90°C	I_{F90}	12	A
Power Dissipation Total at T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.6	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125 inches from case for 5s)	T_L	260	°C

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2800.4**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 280\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	280	µA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	5.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.9	2.5	V
			$T_C = +125^oC$	-	2.1	2.7	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$, $T_C = +25^oC$		3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.2	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	45	60	nC
			$V_{GE} = 20V$	-	70	90	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 500\mu H$, $I_C = I_{C90}$, $R_G = 25V$, $V_{GE} = 15V$, $T_J = +150^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off	$t_{D(OFF)I}$			-	430	600	ns
Current Fall Time	t_{FI}			-	430	600	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	1.8	-	mJ
Thermal Resistance IGBT	$R_{\theta JC}$			-	-	1.67	°C/W
Thermal Resistance Diode	$R_{\theta JC}$			-	-	1.5	°C/W
Diode Forward Voltage	V_{EC}	$I_{EC} = 12A$		-	-	1.50	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 12A$, $dI_{EC}/dt = 100A/\mu s$		-	-	60	ns

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG12N60D1D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

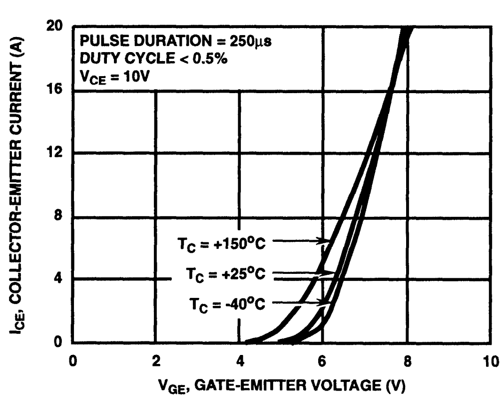


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

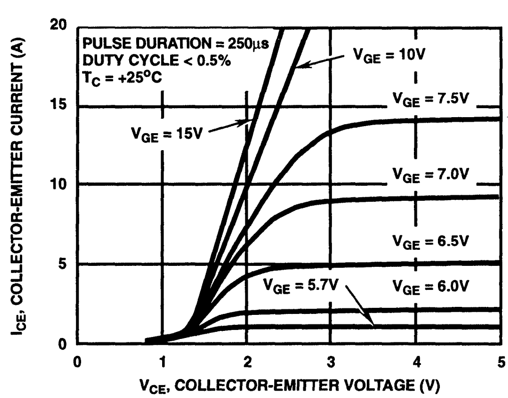


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

3

IGBTs

Typical Performance Curves (Continued)

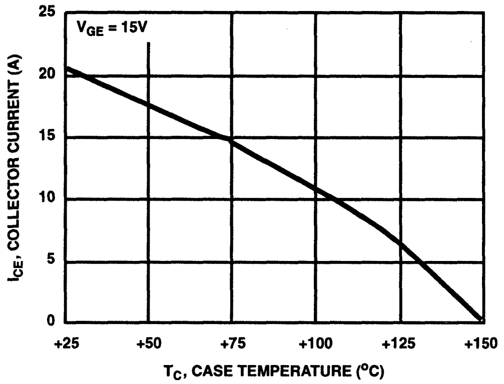


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

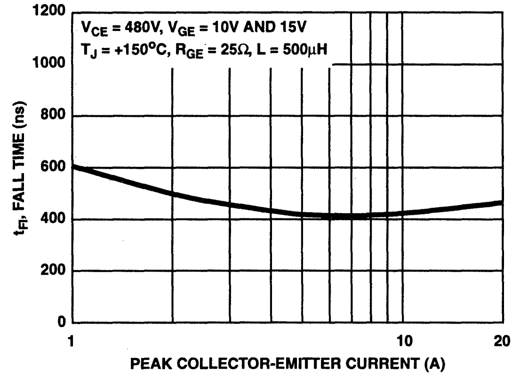


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

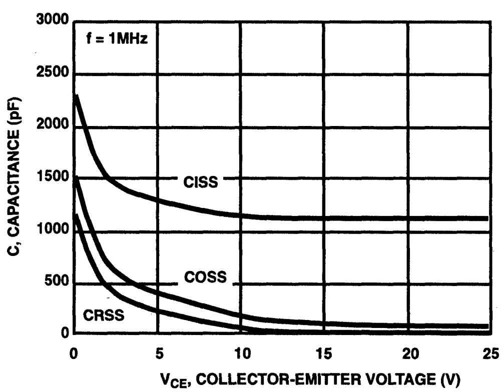


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

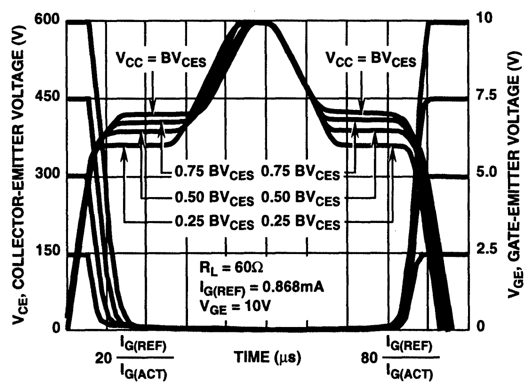


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

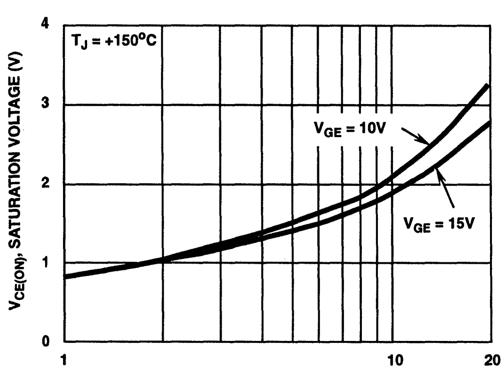


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

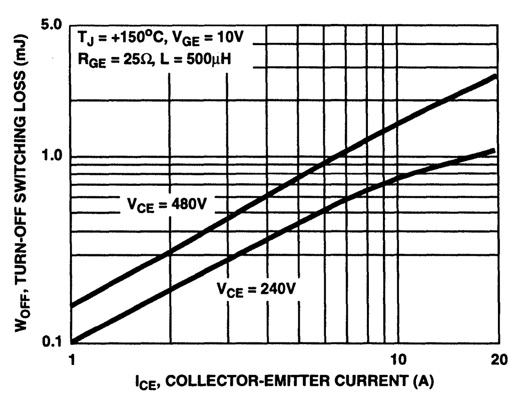


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

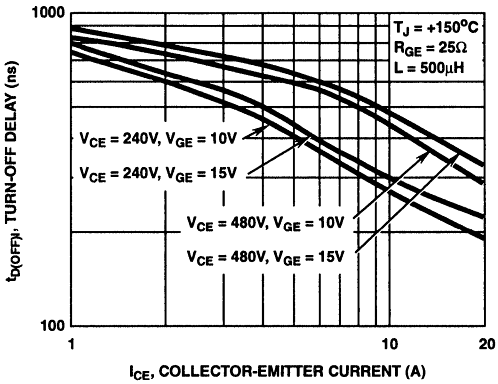
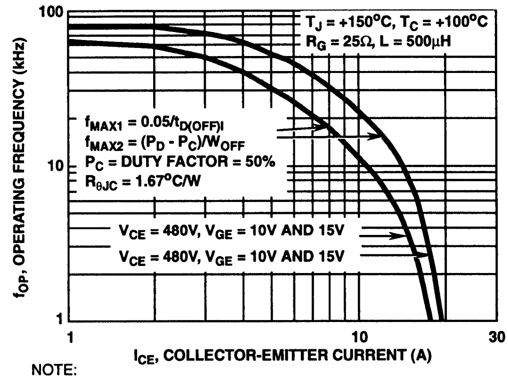


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

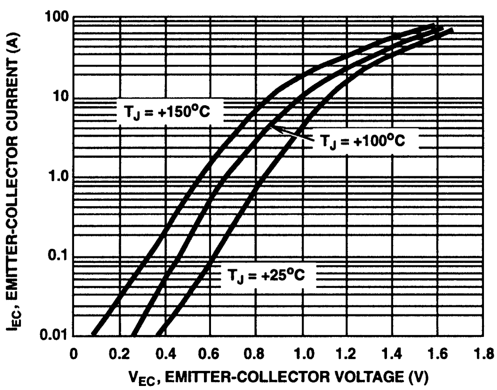


FIGURE 11. TYPICAL DIODE EMITTER-TO-COLLECTOR VOLTAGE

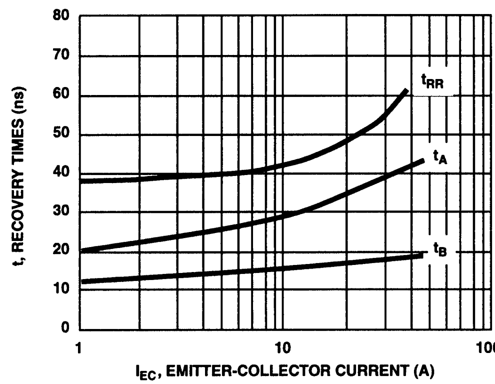


FIGURE 12. TYPICAL t_{RR}, t_A, t_B vs FORWARD CURRENT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{MAX1} \times W_{OFF}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR HGTP14N40F3VL

14A, 400V N-Channel, Logic Level Voltage Clamping IGBT

April 1995

Features

- Logic Level Gate Drive
- Internal Voltage Clamp
- ESD Gate Protection
- $T_J = +150^oC$
- Ignition Energy Capable

Applications

- Automotive Ignition
- Small Engine Ignition
- Fuel Ignitor

Description

This N-Channel IGBT is a MOS gated, logic level device which is intended to be used as an ignition coil driver in automotive ignition circuits. Unique features include an active voltage clamp between the drain and the gate and ESD protection for the logic level gate. Some specifications are unique to this automotive application and are intended to assure device survival in this harsh environment. The development type number for this device is TA49023.

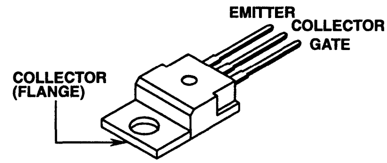
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTP14N40F3VL	TO-220AB	14N40FVL

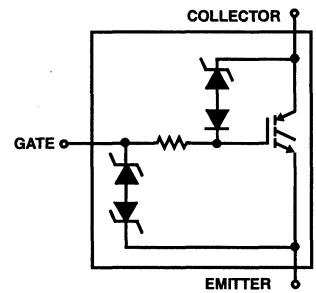
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP14N40F3VL	UNITS
Collector-Emitter Breakdown Voltage at 10mA	BV_{CES}	420	V
Collector-Gate Breakdown Voltage R_{GE} = 10kΩ	BV_{CGR}	420	V
Collector Current Continuous			
V_{GE} = 4.5V at $T_C = +25^oC$	I_{C25}	19	A
V_{GE} = 4.5V at $T_C = +90^oC$	I_{C90}	14	A
Gate-Emitter Voltage Continuous	V_{GES}	±10	V
Gate-Emitter Voltage Pulsed or	V_{GEM}	±12	V
Gate-Emitter Current Pulsed	I_{GEM}	±10	mA
Open Secondary Turn-Off Current			
L = 2.3mH at $+25^oC$	I_{CO}	17	A
L = 2.3mH at $+150^oC$	I_{CO}	12	A
Drain to Source Avalanche Energy at L = 2.3mH, $T_C = +25^oC$	EAS	330	mJ
Power Dissipation Total at $T_C = +25^oC$	P_T	83	W
Power Dissipation Derating $T_C > +25^oC$		0.67	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +150	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Electrostatic Voltage at 100pF, 1500Ω	ESD	6	KV

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3407.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 10mA, V_{GE} = 0V	T_C = +150°C	345	370	415	V
			T_C = +25°C	350	375	420	V
			T_C = -40°C	355	380	425	V
Collector-Emitter Clamp Bkdn. Voltage	$BV_{CE(CL)}$	I_C = 10A	T_C = +150°C	350	385	430	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	I_C = 1.0mA	T_C = +25°C	24	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 250V	T_C = +25°C	-	-	50	µA
		V_{CE} = 250V	T_C = +150°C	-	-	250	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A V_{GE} = 4.5V	T_C = +25°C	-	-	2.0	V
			T_C = +150°C	-	-	2.3	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1.0mA V_{CE} = V_{GE}	T_C = +25°C	1.0	1.5	2.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±10V		-	-	±10	µA
Gate-Emitter Breakdown Voltage	BV_{GES}	I_{GES} = ±1.0mA		±12	-	-	V
Current Turn-off Time-Inductive Load	$t_{D(OFF)I}$ + $t_{F(OFF)I}$	R_L = 32Ω, I_C = 10A, R_G = 25Ω, L = 550µH, V_{CL} = 320V, V_{GE} = 5V, T_C = +125°C		-	12	16	µs
Inductive Use Test	UIS	L = 2.3mH, V_G = 5V, Figure 13	T_C = +150°C	12	-	-	A
			T_C = +25°C	17	-	-	A
Thermal Resistance	$R_{\theta JC}$			-	1.5	-	°C/W

Typical Performance Curves

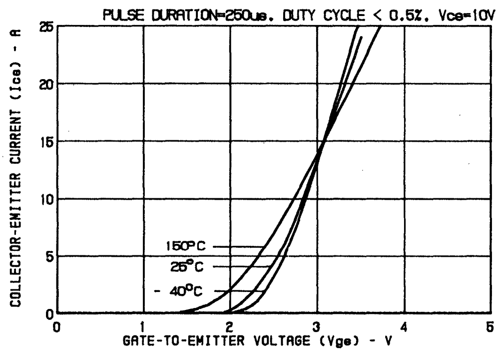


FIGURE 1. TRANSFER CHARACTERISTICS (TYP.)

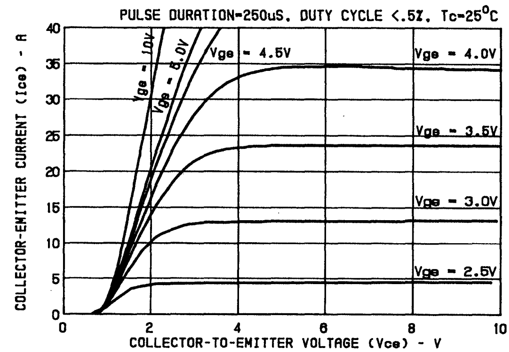


FIGURE 2. SATURATION CHARACTERISTIC (TYP.)

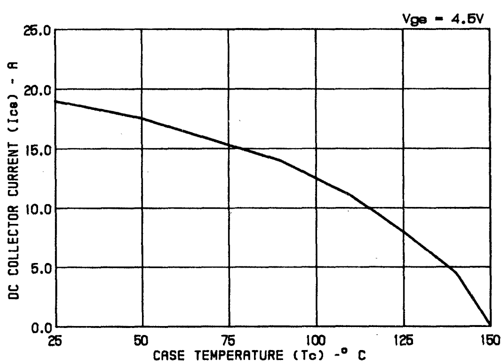


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

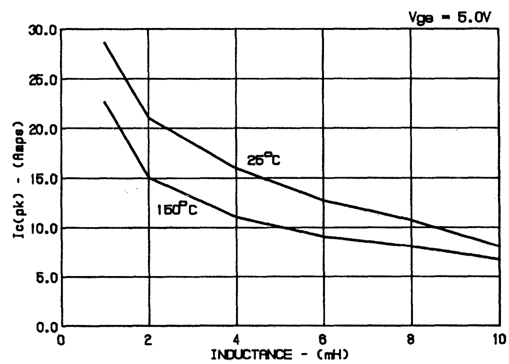


FIGURE 4. OPEN SECONDARY CURRENT AS A FUNCTION OF INDUCTANCE (TYP.)

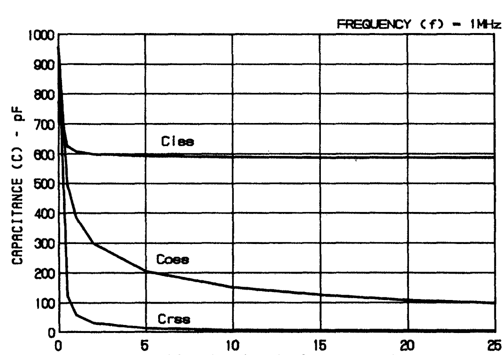


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR - EMITTER VOLTAGE (TYP.)

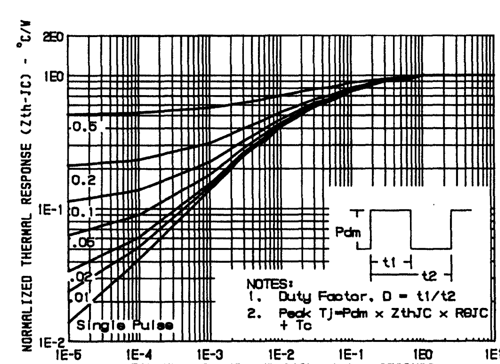


FIGURE 6. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE, vs PULSE DURATION

Typical Performance Curves (Continued)

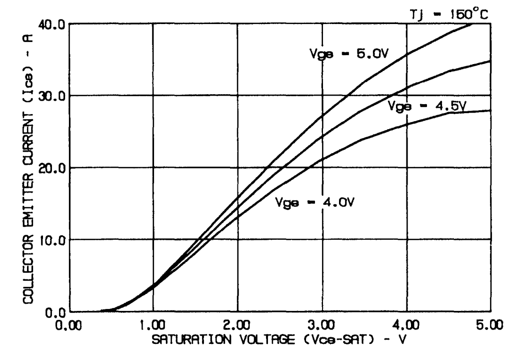


FIGURE 7. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE; T_J = +150°C (TYP.)

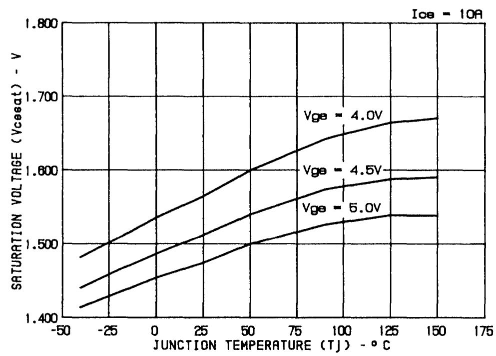


FIGURE 8. SATURATION VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (TYP.)

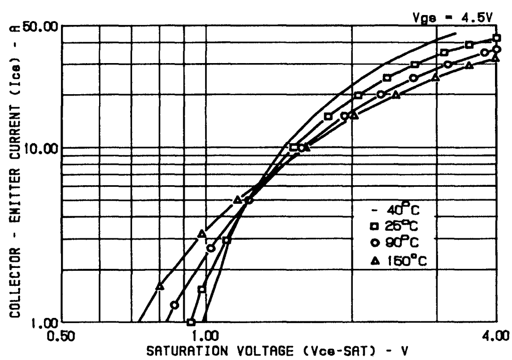


FIGURE 9. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE (TYP.)

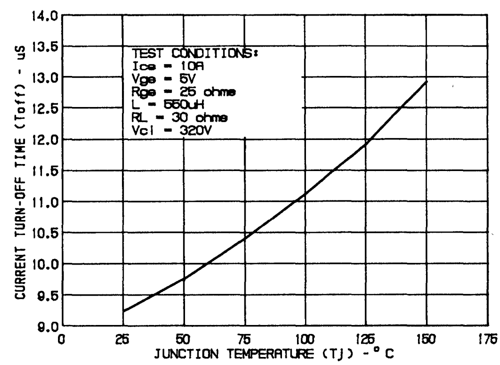


FIGURE 10. INDUCTIVE CURRENT TURN-OFF TIME AS A FUNCTION OF JUNCTION TEMPERATURE (TYP.)

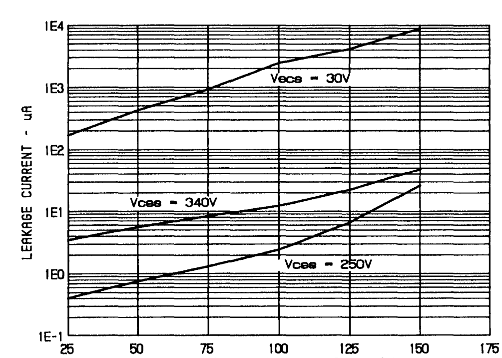


FIGURE 11. LEAKAGE CURRENTS AS A FUNCTION OF JUNCTION TEMPERATURE (TYP.)

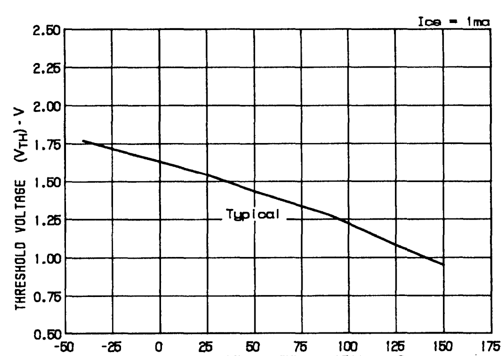


FIGURE 12. THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE (TYP.)

3

IGBTs

Test Circuits

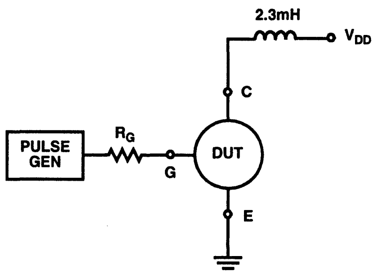


FIGURE 13. USE TEST CIRCUIT

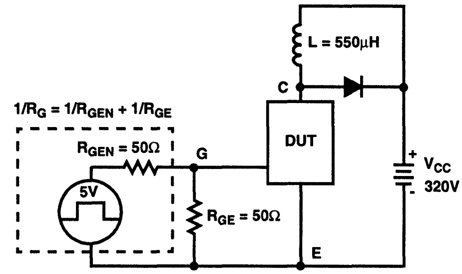


FIGURE 14. INDUCTIVE SWITCHING TEST CIRCUIT

Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "†ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR

HGTP14N36G3VL, HGT1S14N36G3VL, HGT1S14N36G3VLS

14A, 360V N-Channel, Logic Level, Voltage Clamping IGBTs

June 1995

Features

- Logic Level Gate Drive
- Internal Voltage Clamp
- ESD Gate Protection
- $T_J = 175^oC$
- Ignition Energy Capable

Description

This N-Channel IGBT is a MOS gated, logic level device which is intended to be used as an ignition coil driver in automotive ignition circuits. Unique features include an active voltage clamp between the collector and the gate which provides Self Clamped Inductive Switching (SCIS) capability in ignition circuits. Internal diodes provide ESD protection for the logic level gate. Both a series resistor and a shunt resister are provided in the gate circuit.

PACKAGING AVAILABILITY

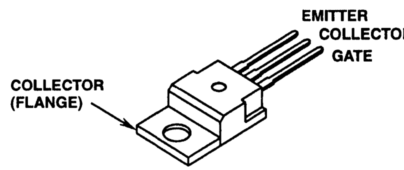
PART NUMBER	PACKAGE	BRAND
HGTP14N36G3VL	TO-220AB	14N36GVL
HGT1S14N36G3VL	TO-262AA	14N36GVL
HGT1S14N36G3VLS	TO-263AB	14N36GVL

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., HGT1S14N36G3VLS9A.

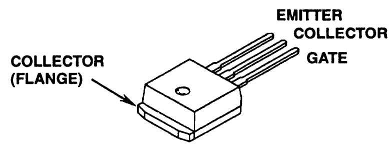
The development type number for this device is TA49021.

Packages

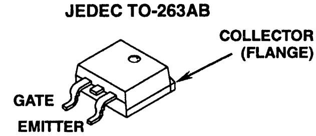
JEDEC TO-220AB



JEDEC TO-262AA

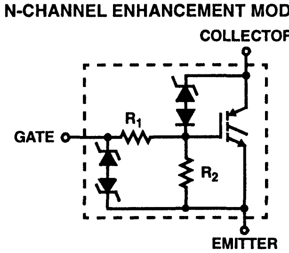


JEDEC TO-263AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP14N36G3VL, HGT1S14N36G3VL, HGT1S14N36G3VLS	UNITS
Collector-Emitter Bkdn Voltage at 10mA	BV_{CER}	390	V
Emitter-Collector Bkdn Voltage at 10mA	BV_{ECS}	24	V
Collector Current Continuous at $V_{GE} = 5V$, $T_C = +25^oC$	I_{C25}	18	A
at $V_{GE} = 5V$, $T_C = +100^oC$	I_{C100}	14	A
Gate-Emitter Voltage (Note)	V_{GEM}	±10	V
Inductive Switching Current at L = 2.3mH, $T_C = +25^oC$	I_{SCIS}	17	A
at L = 2.3mH, $T_C = +175^oC$	I_{SCIS}	12	A
Collector to Emitter Avalanche Energy at L = 2.3mH, $T_C = +25^oC$	E_{AS}	332	mJ
Power Dissipation Total at $T_C = +25^oC$	P_D	100	W
Power Dissipation Derating $T_C > +25^oC$		0.67	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +175	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Electrostatic Voltage at 100pF, 1500Ω	ESD	6	KV

NOTE: May be exceeded if I_{GEM} is limited to 10mA.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4008**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CER}	$I_C = 10mA$, $V_{GE} = 0V$ $R_{GE} = 1k\Omega$	$T_C = +175^oC$	320	355	400	V
			$T_C = +25^oC$	330	360	390	V
			$T_C = -40^oC$	320	350	385	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 7A$, $V_{CE} = 12V$	$T_C = +25^oC$	-	2.7	-	V
Gate Charge	$Q_{G(ON)}$	$I_C = 7A$, $V_{CE} = 12V$	$T_C = +25^oC$	-	24	-	nC
Collector-Emitter Clamp Breakdown Voltage	$BV_{CE(CL)}$	$I_C = 7A$ $R_G = 1000\Omega$	$T_C = +175^oC$	350	380	410	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_C = 10mA$	$T_C = +25^oC$	24	28	-	V
Collector-Emitter Leakage Current	I_{CER}	$V_{CE} = 250V$ $R_{GE} = 1k\Omega$	$T_C = +25^oC$	-	-	25	μA
			$T_C = +175^oC$	-	-	250	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 7A$ $V_{GE} = 4.5V$	$T_C = +25^oC$	-	1.25	1.45	V
			$T_C = +175^oC$	-	1.15	1.6	V
		$I_C = 14A$ $V_{GE} = 5V$	$T_C = +25^oC$	-	1.6	2.2	V
			$T_C = +175^oC$	-	1.7	2.9	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$ $V_{CE} = V_{GE}$	$T_C = +25^oC$	1.3	1.8	2.2	V
Gate Series Resistance	R_1		$T_C = +25^oC$	-	75	-	Ω
Gate-Emitter Resistance	R_2		$T_C = +25^oC$	10	20	30	kΩ
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 10V$		±330	±500	±1000	μA
Gate-Emitter Breakdown Voltage	BV_{GES}	$I_{GES} = \pm 2mA$		±12	±14	-	V
Current Turn-Off Time-Inductive Load	$t_{D(OFF)I}$ + $t_{F(OFF)I}$	$I_C = 7A$, $R_L = 28\Omega$ $R_G = 25\Omega$, $L = 550\mu H$, $V_{CL} = 300V$, $V_{GE} = 5V$, $T_C = +175^oC$		-	7	-	μs
Inductive Use Test	I_{SCIS}	$L = 2.3mH$, $V_G = 5V$,	$T_C = +175^oC$	12	-	-	A
			$T_C = +25^oC$	17	-	-	A
Thermal Resistance	$R_{\theta JC}$			-	-	1.5	°C/W

Typical Performance Curves

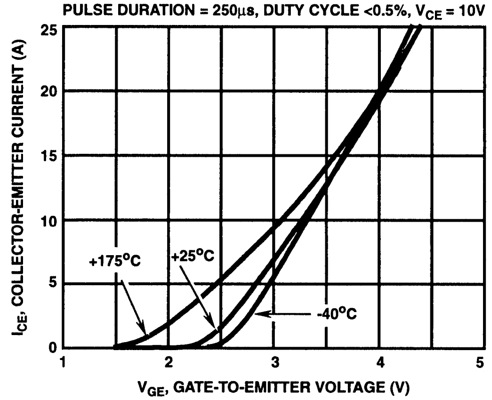


FIGURE 1. TRANSFER CHARACTERISTICS

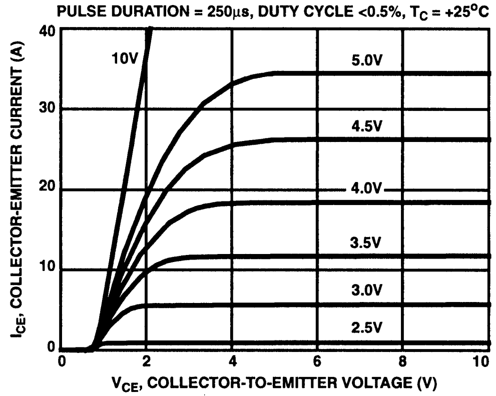


FIGURE 2. SATURATION CHARACTERISTICS

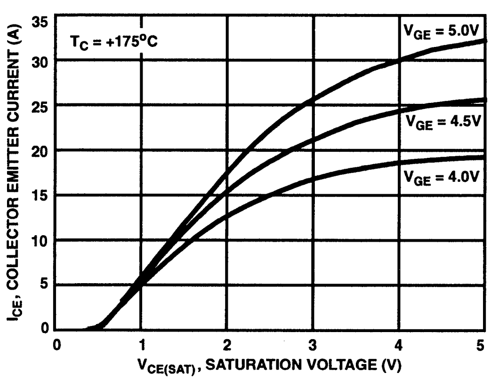


FIGURE 3. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE

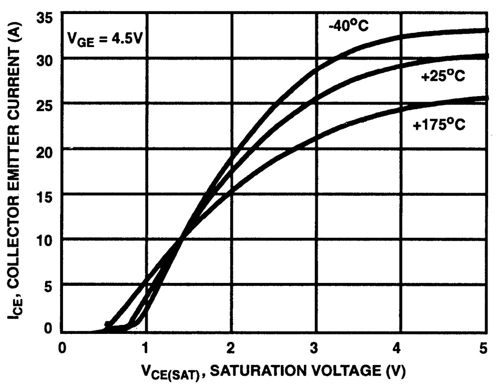


FIGURE 4. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE

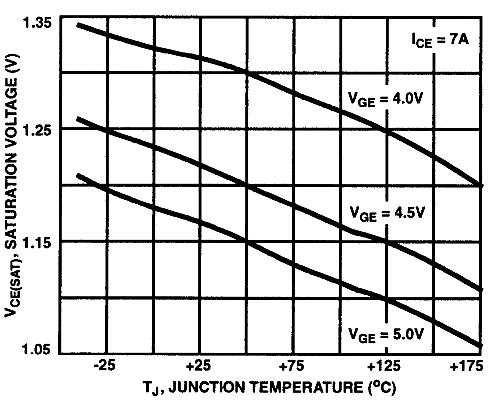


FIGURE 5. SATURATION VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

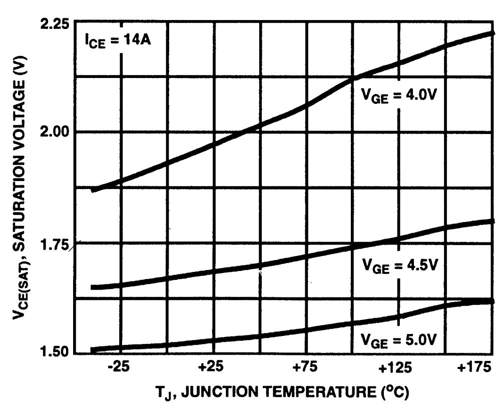


FIGURE 6. SATURATION VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

3

IGBTs

Typical Performance Curves (Continued)

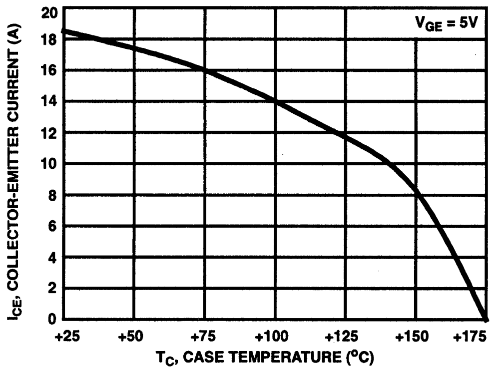


FIGURE 7. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF CASE TEMPERATURE

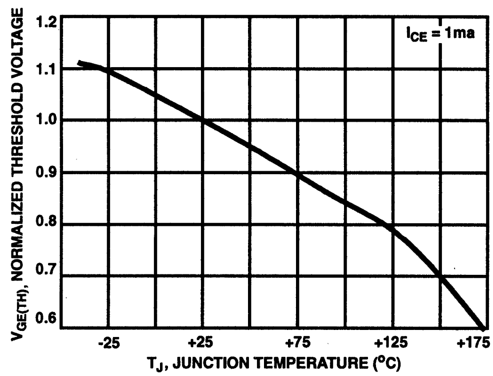


FIGURE 8. NORMALIZED THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

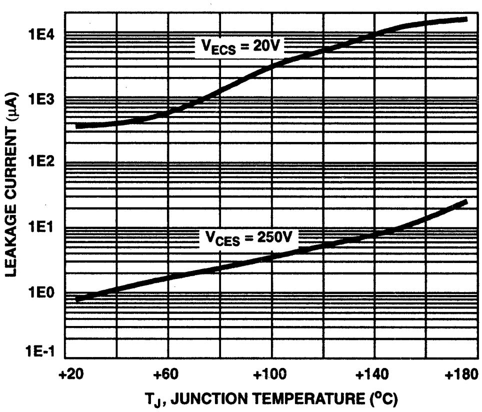


FIGURE 9. LEAKAGE CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

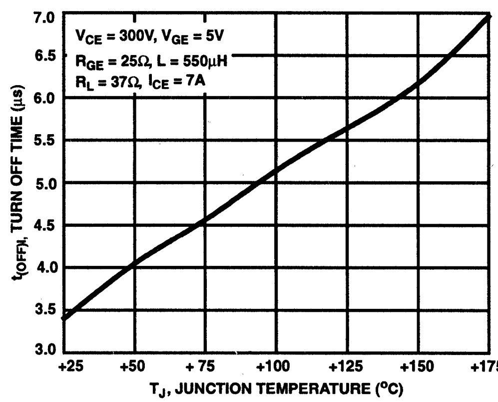


FIGURE 10. TURN-OFF TIME AS A FUNCTION OF JUNCTION TEMPERATURE

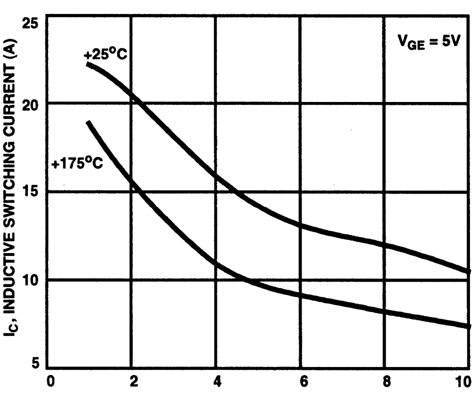


FIGURE 11. SELF CLAMPED INDUCTIVE SWITCHING CURRENT AS A FUNCTION OF INDUCTANCE

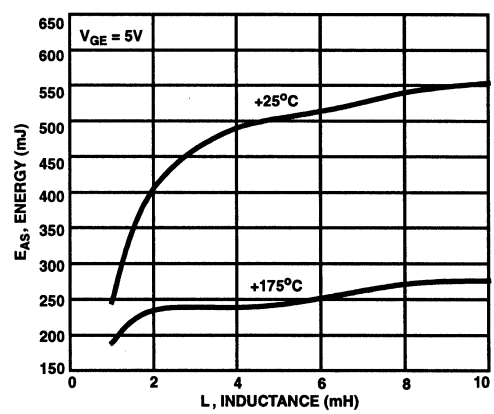


FIGURE 12. SELF CLAMPED INDUCTIVE SWITCHING ENERGY AS A FUNCTION OF INDUCTANCE

Typical Performance Curves (Continued)

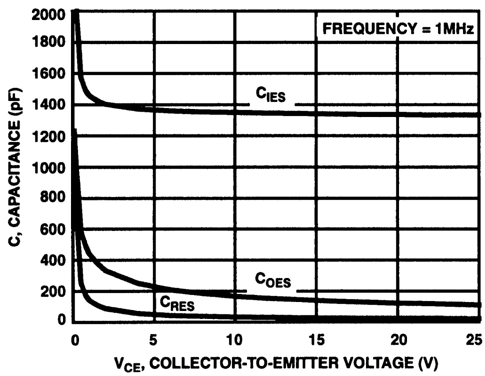


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

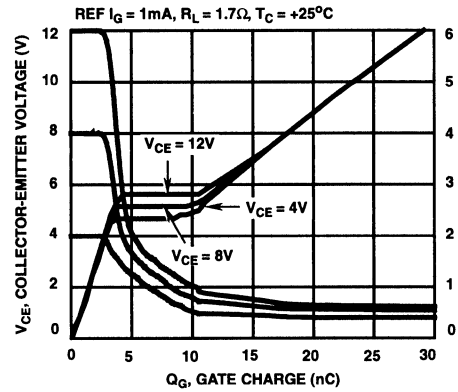


FIGURE 14. GATE CHARGE WAVEFORMS

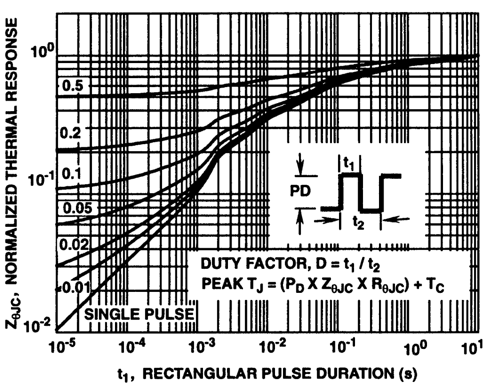


FIGURE 15. NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

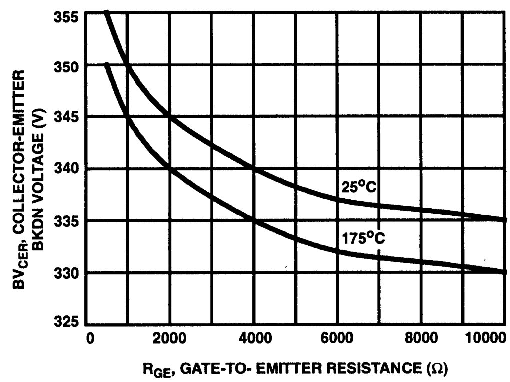


FIGURE 16. BREAKDOWN VOLTAGE AS A FUNCTION OF GATE-EMITTER RESISTANCE

Test Circuits

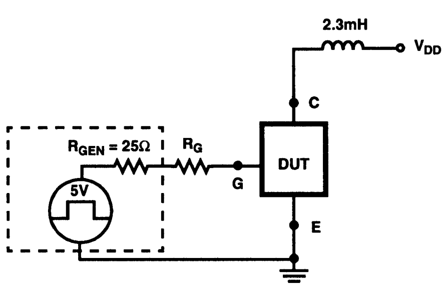


FIGURE 17. SELF CLAMPED INDUCTIVE SWITCHING CURRENT TEST CIRCUIT

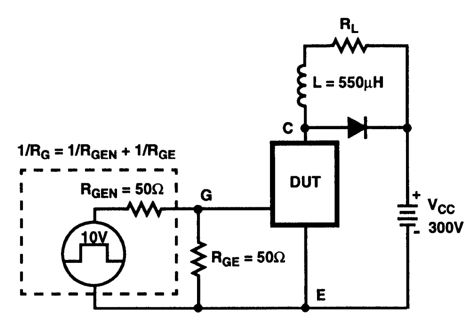


FIGURE 18. CLAMPED INDUCTIVE SWITCHING TIME TEST CIRCUIT

Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †"ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** -The gate-voltage rating of V_{GEM} may be exceeded if I_{GEM} is limited to 10mA.

† Trademark Emerson and Cumming, Inc

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

HARRIS SEMICONDUCTOR

HGTP15N40C1, 40E1, 50C1, 50E1, HGTH20N40C1, 40E1, 50C1, 50E1

15A, 20A, 400V and 500V N-Channel IGBTs

April 1995

Features

- 15A and 20A, 400V and 500V
- $V_{CE(ON)}$ 2.5V
- T_{FI} 1µs, 0.5µs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- No Anti-Parallel Diode

Applications

- Power Supplies
- Motor Drives
- Protection Circuits

Description

The HGTH20N40C1, HGTH20N40E1, HGTH20N50C1, HGTH20N50E1, HGTP15N40C1, HGTP15N40E1, HGTP15N50C1 and HGTP15N50E1 are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

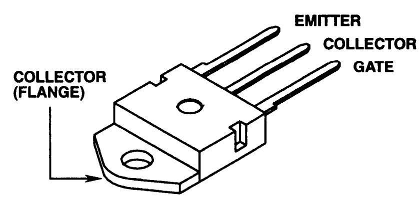
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTH20N40C1	TO-218AC	G20N40C1
HGTH20N40E1	TO-218AC	G20N40E1
HGTH20N50C1	TO-218AC	G20N50C1
HGTH20N50E1	TO-218AC	G20N50E1
HGTP15N40C1	TO-220AB	G15N40C1
HGTP15N40E1	TO-220AB	G15N40E1
HGTP15N50C1	TO-220AB	G15N50C1
HGTP15N50E1	TO-220AB	G15N50E1

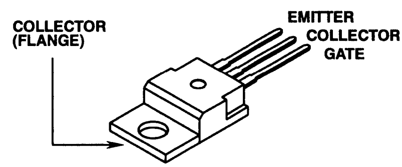
NOTE: When ordering, use the entire part number.

Packages

HGTH-TYPES JEDEC TO-218AC

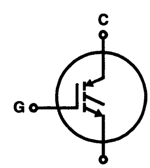


HGTP-TYPES JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

IGBTs

Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

	HGTH20N40C1 HGTH20N40E1	HGTH20N50C1 HGTH20N50E1	HGTP15N40C1 HGTP15N40E1	HGTP15N50C1 HGTP15N50E1	UNITS
Collector-Emitter Voltage . . . . . V_{CES}	400	500	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$ . . . . . V_{CGR}	400	500	400	500	V
Reverse Collector-Emitter Voltage . . . . . V_{CES}(rev.)	-5	-5	-5	-5	V
Gate-Emitter Voltage . . . . . V_{GE}	±20	±20	±20	±20	V
Collector Current Continuous . . . . . I_C	20	20	15	15	A
Collector Current Pulsed . . . . . I_{CM}	35	35	35	35	A
Power Dissipation at $T_C = +25^oC$ . . . . . P_D	100	100	75	75	W
Power Dissipation Derating $T_C > +25^oC$	0.8	0.8	0.6	0.6	W/°C
Operating and Storage Junction Temperature Range . . . T_J, T_{STG}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 2174.3

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS HGTH20N40C1, E1, HGTP15N40C1, E1 MIN	HGTH20N40C1, E1, HGTP15N40C1, E1 MAX	HGTH20N50C1, E1, HGTP15N50C1, E1 MIN	HGTH20N50C1, E1, HGTP15N50C1, E1 MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1mA, V_{GE} = 0	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, I_C = 1mA	2.0	4.5	2.0	4.5	V
Zero -Gate Voltage Collector Current	I_{CES}	V_{CE} = 400V, T_C = +25°C	-	250	-	-	µA
		V_{CE} = 500V, T_C = +25°C	-	-	-	250	µA
		V_{CE} = 400V, T_C = +125°C	-	1000	-	-	µA
		V_{CE} = 500V, T_C = +125°C	-	-	-	1000	µA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	-	100	-	100	nA
Reverse Collector-Emitter Leakage Current	I_{CE}	R_{GE} = 0Ω, V_{EC} = 5V	-	-5	-	-5	mA
Collector-Emitter on Voltage	$V_{CE(ON)}$	I_C = 20A, V_{GE} = 10V	-	2.5	-	2.5	V
		I_C = 35A, V_{GE} = 20V	-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10A, V_{CE} = 10V	-	6 (Typ)	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 10A, V_{CE} = 10V	-	33 (Typ)	-	33 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	I_C = 20A, $V_{CE(CLP)}$ = 300V, L = 25µH, T_J = +100°C, V_{GE} = 10V, R_G = 25Ω	-	50	-	50	ns
Rise Time	t_{RI}		-	50	-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns
Fall Time	t_{FI}						
40E1, 50E1			680 (Typ)	1000	680 (Typ)	1000	ns
40C1, 50C1			400	500	400	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	I_C = 10A, $V_{CE(CLP)}$ = 300V, L = 25µH, T_J = +100°C, V_{GE} = 10V, R_G = 25Ω					
40E1, 50E1			1810 (Typ)				µJ
40C1, 50C1			1070 (Typ)				µJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	HGTH, HGTM	-	1.25	-	1.25	°C/W
		HGTP	-	1.67	-	1.67	°C/W

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Typical Performance Curves

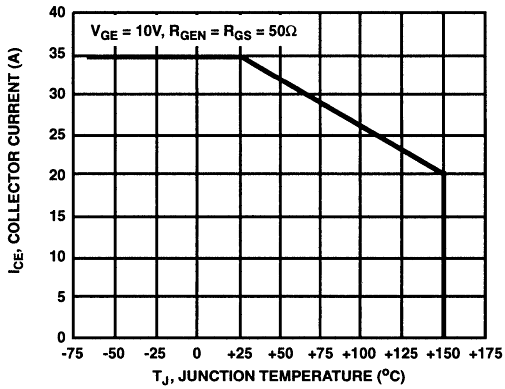


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. R_G = 25Ω, V_{GE} = 0V ARE THE MIN. ALLOWABLE VALUES

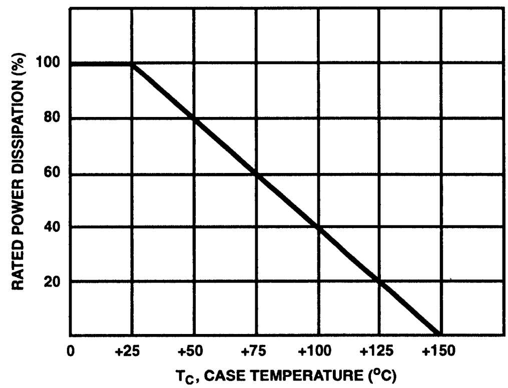


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

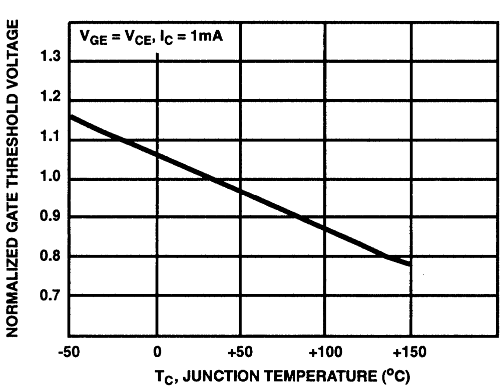


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

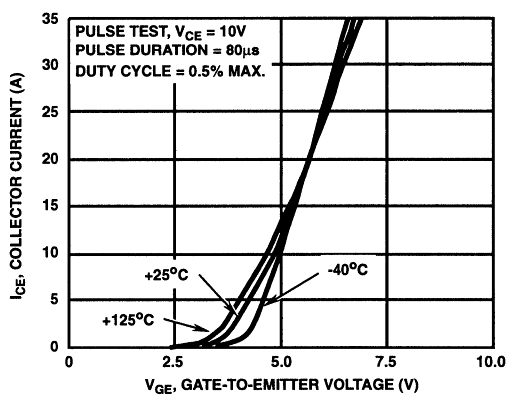


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

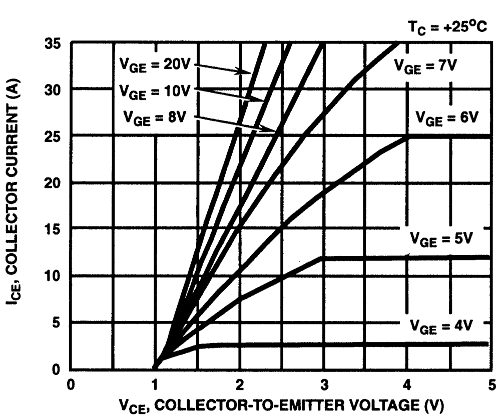


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

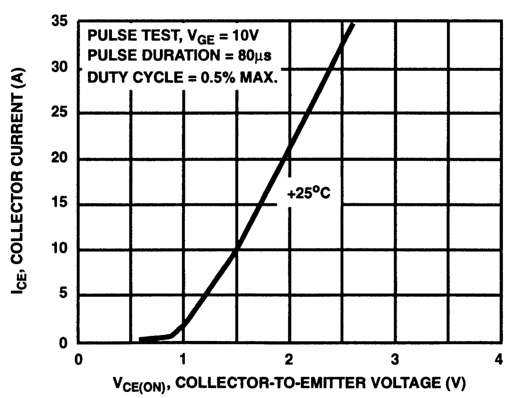


FIGURE 6. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

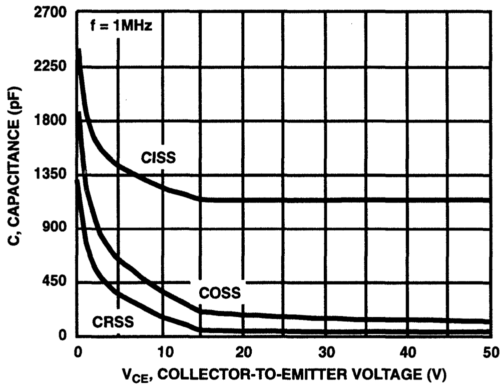


FIGURE 7. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

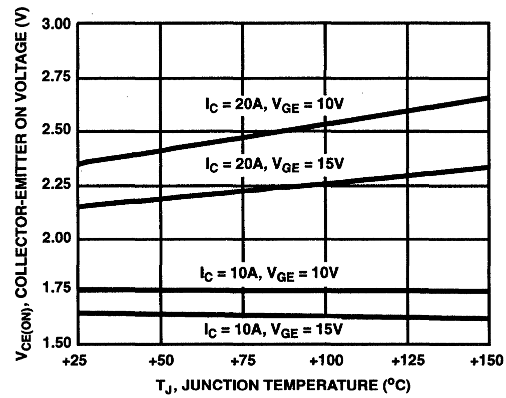


FIGURE 8. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

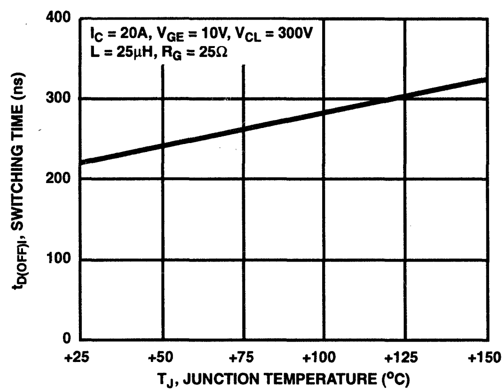


FIGURE 9. TYPICAL TURN-OFF DELAY TIME

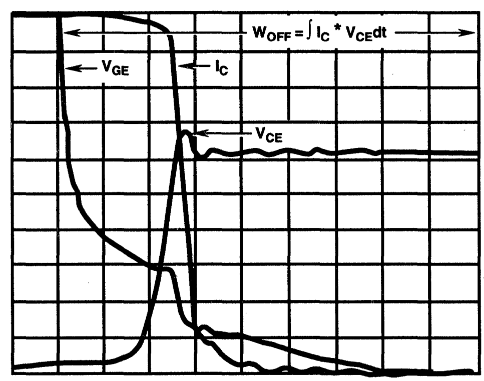


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

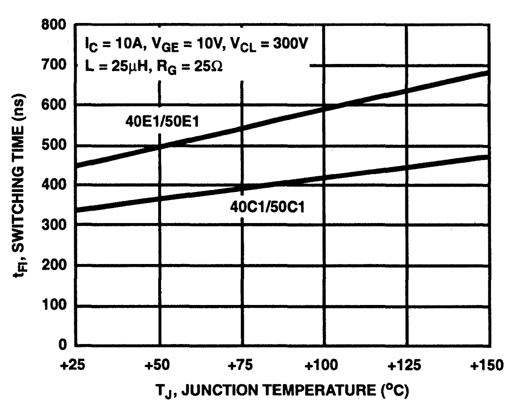


FIGURE 11. TYPICAL FALL TIME (I_C = 10A)

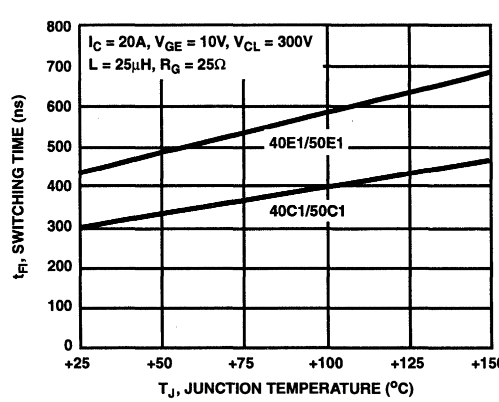


FIGURE 12. TYPICAL FALL TIME (I_C = 20A)

Typical Performance Curves (Continued)

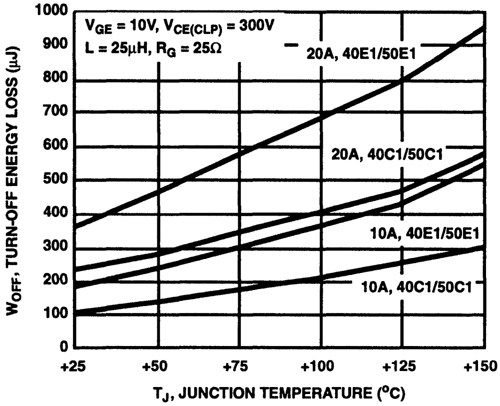


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE

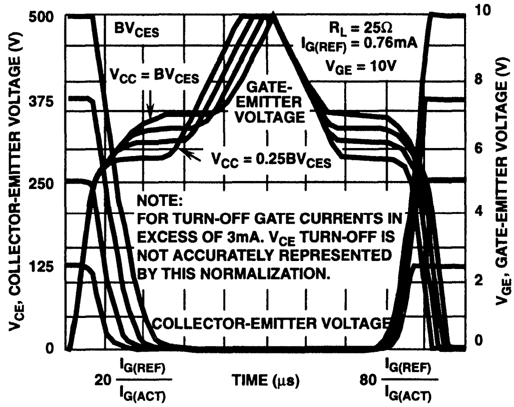


FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260 ON THE USE OF NORMALIZED SWITCHING WAVEFORMS)

Test Circuit

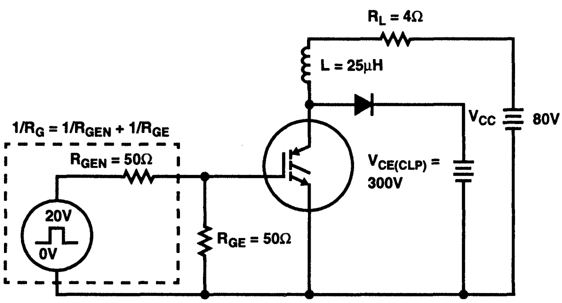


FIGURE 15. INDUCTIVE SWITCHING TEST CIRCUIT

3

IGBTs

HARRIS SEMICONDUCTOR

HGTP20N35G3VL, HGT1S20N35G3VL, HGT1S20N35G3VLS

20A, 350V N-Channel, Logic Level, Voltage Clamping IGBTs

April 1995

Features

- Logic Level Gate Drive
- Internal Voltage Clamp
- ESD Gate Protection
- $T_J = 175^oC$
- Ignition Energy Capable

Description

This N-Channel IGBT is a MOS gated, logic level device which is intended to be used as an ignition coil driver in automotive ignition circuits. Unique features include an active voltage clamp between the collector and the gate which provides Self Clamped Inductive Switching (SCIS) capability in ignition circuits. Internal diodes provide ESD protection for the logic level gate. Both a series resistor and a shunt resistor are provided in the gate circuit.

PACKAGING AVAILABILITY

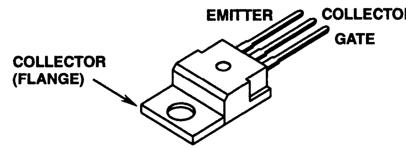
PART NUMBER	PACKAGE	BRAND
HGTP20N35G3VL	T0-220AB	20N35GVL
HGT1S20N35G3VL	T0-262AA	20N35GVL
HGT1S20N35G3VLS	T0-263AB	20N35GVL

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., HGT1S20N35G3VLS9A.

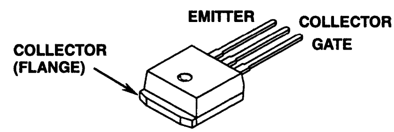
The development type number for this device is TA49076.

Packages

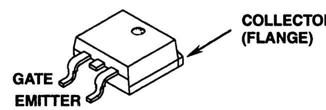
JEDEC TO-220AB



JEDEC TO-262AA

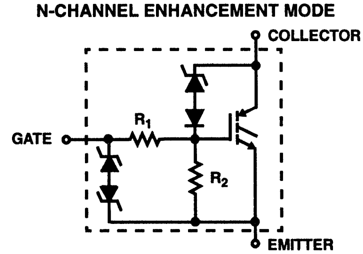


JEDEC TO-263AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP20N35G3VL HGT1S20N35G3VL HGT1S20N35G3VLS	UNITS
Collector-Emitter Bkdn Voltage At 10mA, $R_{GE} = 1k\Omega$	BV_{CER}	375	V
Emitter-Collector Bkdn Voltage At 10mA	BV_{ECS}	24	V
Collector Current Continuous At $V_{GE} = 5.0V$, $T_C = +25^oC$, Figure 7	I_{C25}	20	A
At $V_{GE} = 5.0V$, $T_C = +100^oC$	I_{C100}	20	A
Gate-Emitter-Voltage (Note)	V_{GES}	±10	V
Inductive Switching Current At L = 2.3mH, $T_C = +25^o$ C	I_{SCIS}	26	A
At L = 2.3mH, $T_C = +175^oC$	I_{SCIS}	18	A
Collector to Emitter Avalanche Energy At L = 2.3mH, $T_C = +25^oC$	E_{AS}	775	mJ
Power Dissipation Total At $T_C = +25^oC$	P_D	150	W
Power Dissipation Derating $T_C > +25^oC$		1.0	W/^{o}C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +175	^{o}C
Maximum Lead Temperature for Soldering	T_L	260	^{o}C
Electrostatic Voltage at 100pF, 1500Ω	ESD	6	KV

NOTE: May be exceeded if I_{GEM} is limited to 10mA.

File Number **4006**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 10mA, V_{GE} = 0V	T_C = +175°C	310	345	380	V
			T_C = +25°C	320	350	380	V
			T_C = -40°C	320	355	390	V
Collector-Emitter Breakdown Voltage	BV_{CER}	I_C = 10mA V_{GE} = 0V R_{GE} = 1kΩ	T_C = +175°C	300	340	375	V
			T_C = +25°C	315	345	375	V
			T_C = -40°C	315	350	390	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10A V_{CE} = 12V	T_C = +25°C	-	3.7	-	V
Gate Charge	$Q_{G(ON)}$	I_C = 10A V_{GE} = 5V V_{CE} = 12V	T_C = +25°C	-	28.7	-	nC
Collector-Emitter Clamp Bkdn. Voltage	$BV_{CE(CL)}$	I_C = 10A R_G = 0Ω	T_C = +175°C	325	360	395	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	I_C = 10mA	T_C = +25°C	20	32	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 250V	T_C = +25°C	-	-	5	µA
		V_{CE} = 250V	T_C = +175°C	-	-	250	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 10A V_{GE} = 4.5V	T_C = +25°C	-	1.3	1.6	V
			T_C = +175°C	-	1.25	1.5	V
		I_C = 20A V_{GE} = 5.0V	T_C = +25°C	-	1.6	2.8	V
			T_C = +175°C	-	1.9	3.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1mA V_{CE} = V_{GE}	T_C = +25°C	1.3	1.8	2.3	V
Gate Series Resistance	R_1		T_C = +25°C	-	1.0	-	kΩ
Gate-Emitter Resistance	R_2		T_C = +25°C	10	17	25	kΩ
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±10V		±400	±590	±1000	µA
Gate-Emitter Breakdown Voltage	BV_{GES}	I_{GES} = ±2mA		±12	±14	-	V
Current Turn-Off Time-Inductive Load	$t_{D(OFF)I}$ + $t_{F(OFF)I}$	I_C = 10A, R_G = 25Ω, L = 550 H, R_L = 26.4Ω, V_{GE} = 5V, V_{CL} = 300V, T_C = +175°C		-	15	30	µs
Inductive Use Test	I_{SCIS}	L = 2.3mH, V_G = 5V, R_G = 0Ω	T_C = +175°C	18	-	-	A
			T_C = +25°C	26	-	-	A
Thermal Resistance	$R_{\theta JC}$			-	-	1.0	°C/W

Typical Performance Curves

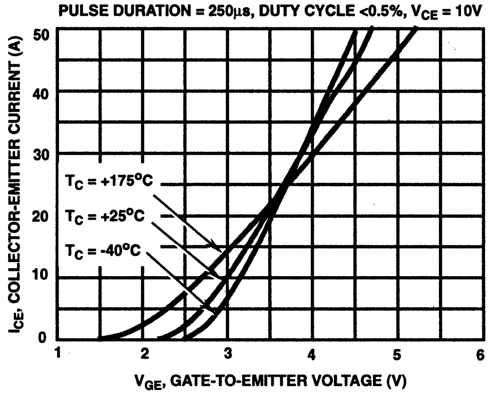


FIGURE 1. TRANSFER CHARACTERISTICS

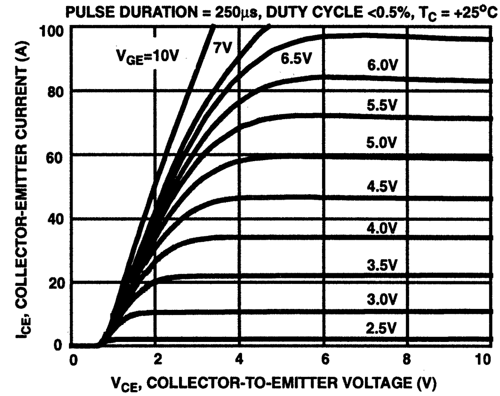


FIGURE 2. SATURATION CHARACTERISTICS

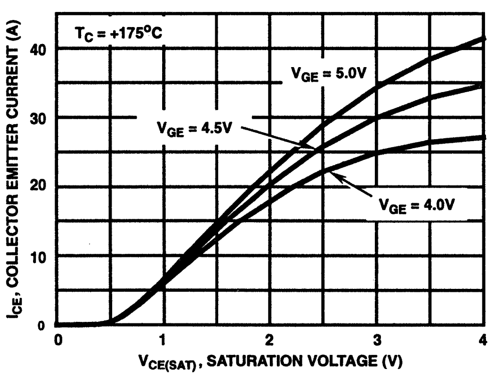


FIGURE 3. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE

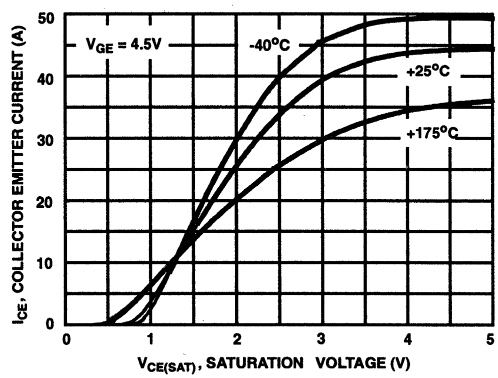


FIGURE 4. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF SATURATION VOLTAGE

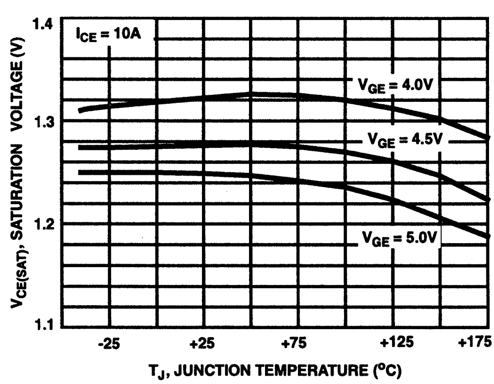


FIGURE 5. SATURATION VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

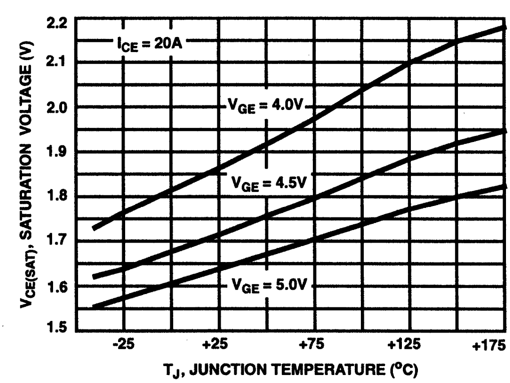


FIGURE 6. SATURATION VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

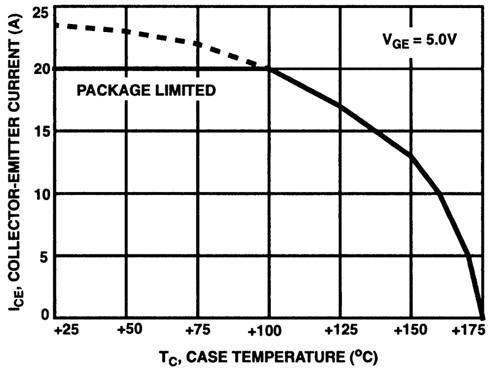


FIGURE 7. COLLECTOR-EMITTER CURRENT AS A FUNCTION OF CASE TEMPERATURE

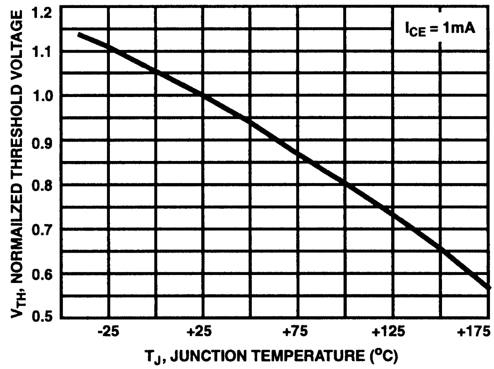


FIGURE 8. NORMALIZED THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

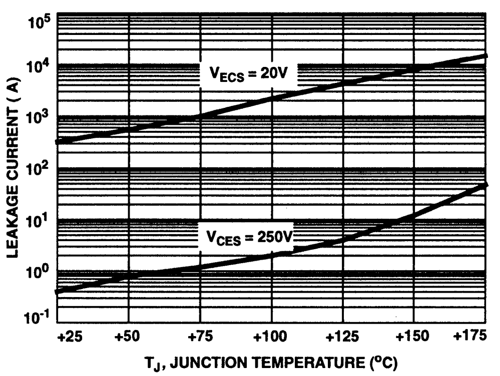


FIGURE 9. LEAKAGE CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

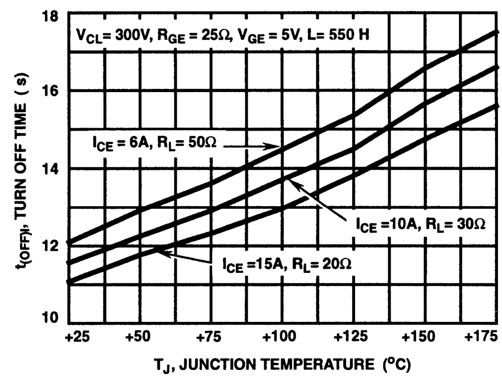


FIGURE 10. TURN-OFF TIME AS A FUNCTION OF JUNCTION TEMPERATURE

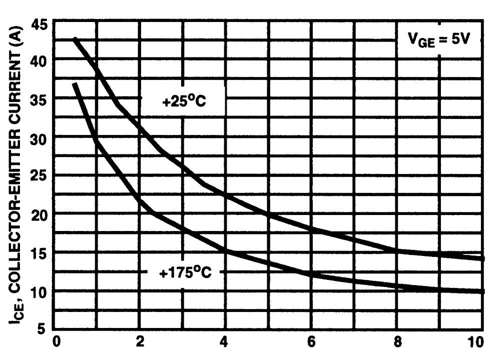


FIGURE 11. SELF CLAMPED INDUCTIVE SWITCHING CURRENT AS A FUNCTION OF INDUCTANCE

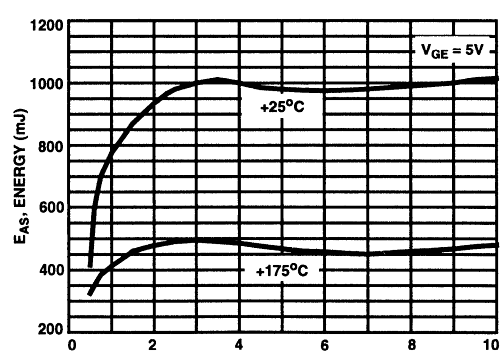


FIGURE 12. SELF CLAMPED INDUCTIVELY SWITCHING ENERGY AS A FUNCTION OF INDUCTANCE

Typical Performance Curves (Continued)

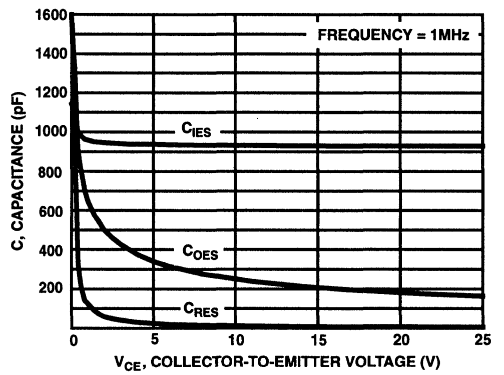


FIGURE 13. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

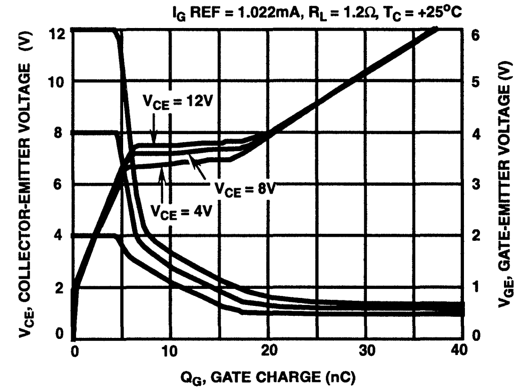


FIGURE 14. GATE CHARGE WAVEFORMS

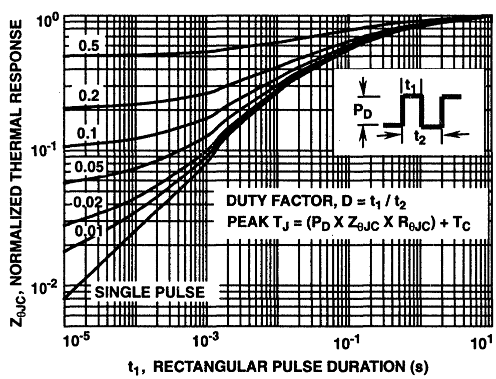


FIGURE 15. NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

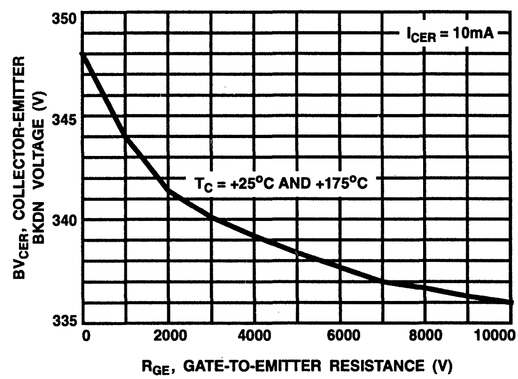


FIGURE 16. BREAKDOWN VOLTAGE AS A FUNCTION OF GATE - EMITTER RESISTANCE

Test Circuits

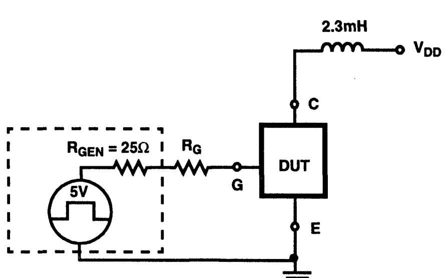


FIGURE 17. USE TEST CIRCUIT

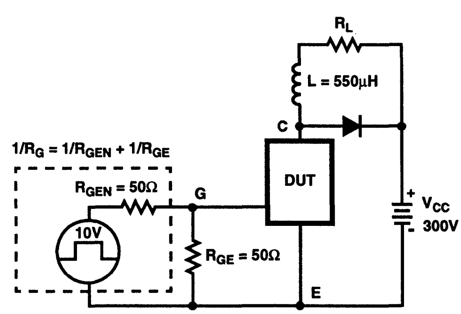


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

HARRIS SEMICONDUCTOR HGTG20N50C1D

April 1995

20A, 500V N-Channel IGBT with Anti-Parallel Ultrafast Diode

Features

- 20A, 500V
- Latch Free Operation
- Typical Fall Time < 500ns
- High Input Impedance
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{RR} < 60ns

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{RR} < 60ns) with soft recovery characteristic.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contractors.

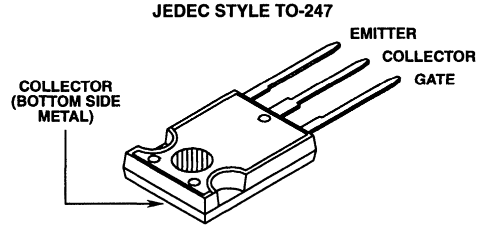
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG20N50C1D	TO-247	G20N50C1D

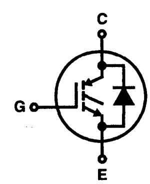
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Terminal Diagram



3

IGBTs

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTG20N50C1D	UNITS
Collector-Emitter Voltage	BV_{CES}	500	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	500	V
Collector Current Continuous at T_C = +25°C	I_{C25}	26	A
at T_C = +90°C	I_{C90}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	35	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Diode Forward Current at T_C = +25°C	I_{F25}	26	A
at T_C = +90°C	I_{F90}	20	A
Power Dissipation Total at T_C = +25°C	P_D	75	W
Power Dissipation Derating T_C > +25°C		0.8	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C

NOTE: 1. T_J = +150°C, Minimum R_{GE} = 25Ω without latch

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2796.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 1mA$, $V_{GE} = 0V$	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, $I_C = 1mA$	2	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = 500V$	-	250	μA
		$T_C = +125^oC$, $V_{CE} = 500V$	-	1000	μA
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm20V$, $V_{CE} = 0V$	-	100	nA
Collector-Emitter On-Voltage	$V_{CE(SAT)}$	$I_C = 20A$, $V_{GE} = 10V$	-	2.5	V
		$I_C = 35A$, $V_{GE} = 20V$	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = 10A$, $V_{CE} = 10V$	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 10A$, $V_{CE} = 10V$	-	33 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	$I_C = 20A$, $V_{CE(CLP)} = 300V$, $L = 25\mu H$, $T_J = +100^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	-	50	ns
Rise Time	t_{RI}		-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	ns
Fall Time	t_{FI}		400 (Typ)	500	ns
Turn-Off Energy Loss Per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	$I_C = 20A$, $V_{CE(CLP)} = 300V$, $L = 25\mu H$, $T_J = +100^oC$, $V_{GE} = 10V$, $R_G = 25\Omega$	1070 (Typ)		μJ
Thermal Resistance Junction-to-Case (IGBT)	$R_{\theta JC}$		-	1.25	°C/W
Thermal Resistance of Diode	$R_{\theta JC}$		-	1.5	ns
Diode Forward Voltage	V_{EC}	$I_{EC} = 20A$	-	1.8	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 20A$, $di_{EC}/dt = 100A/\mu s$	-	60	ns

Typical Performance Curves

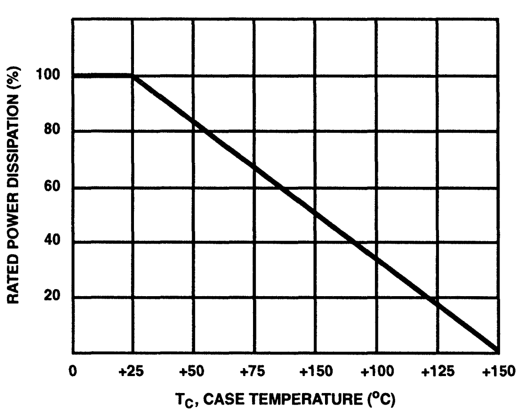


FIGURE 1. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

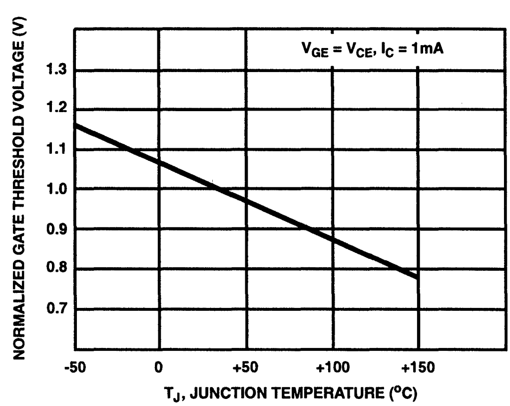


FIGURE 2. TYPICAL NORMALIZED GATE-THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

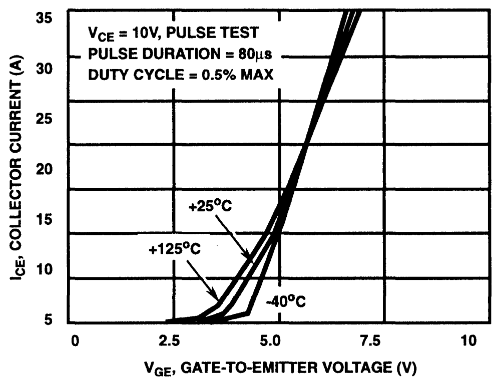


FIGURE 3. TYPICAL TRANSFER CHARACTERISTICS

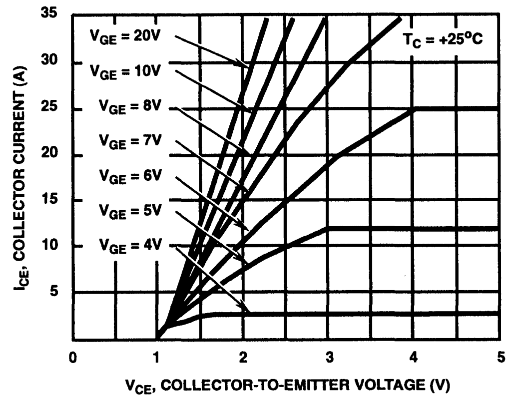


FIGURE 4. TYPICAL SATURATION CHARACTERISTICS

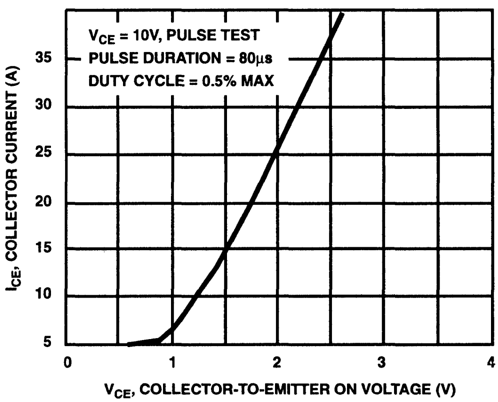


FIGURE 5. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

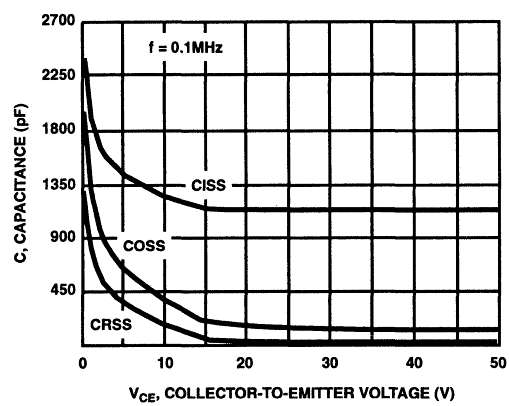


FIGURE 6. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

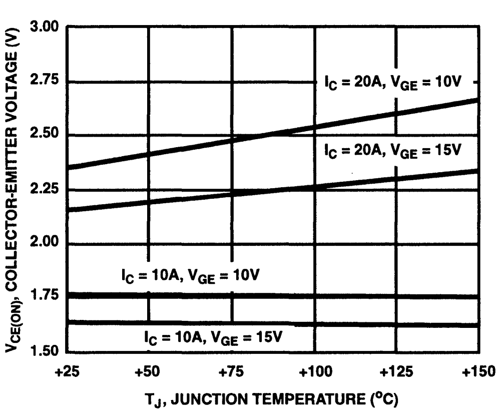


FIGURE 7. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

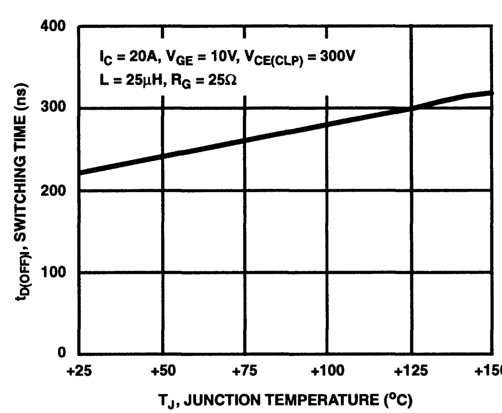


FIGURE 8. TYPICAL TURN-OFF DELAY TIME

Typical Performance Curves (Continued)

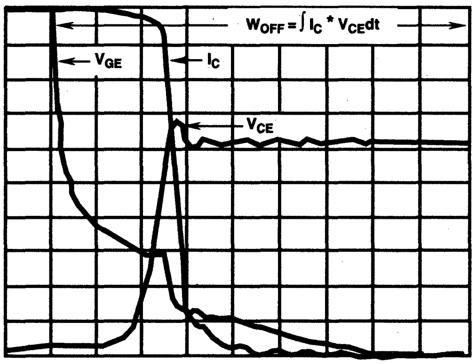


FIGURE 9. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

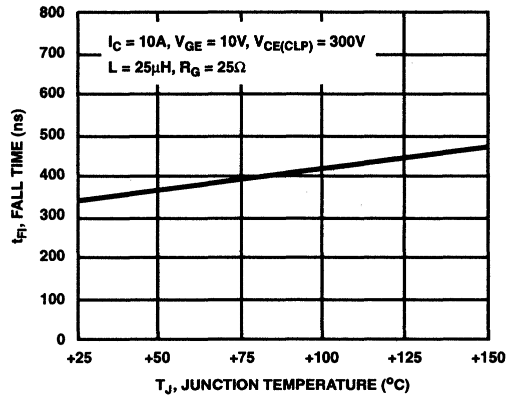


FIGURE 10. TYPICAL FALL TIME (I_C = 10A)

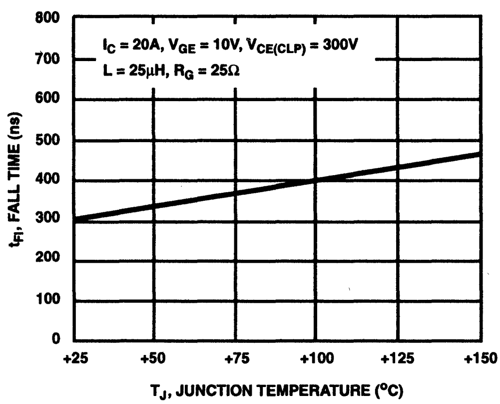


FIGURE 11. TYPICAL FALL TIME (I_C = 20A)

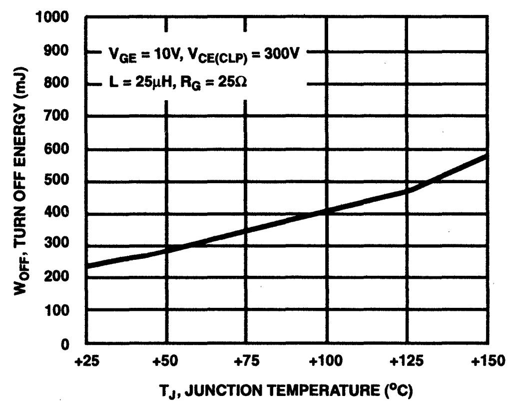
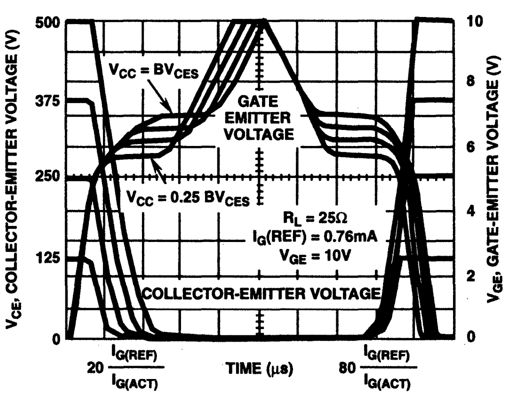


FIGURE 12. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE



NOTE: For Turn-Off gate currents in excess of 3mA. V_{CE} Turn-Off is not accurately represented by this normalization.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

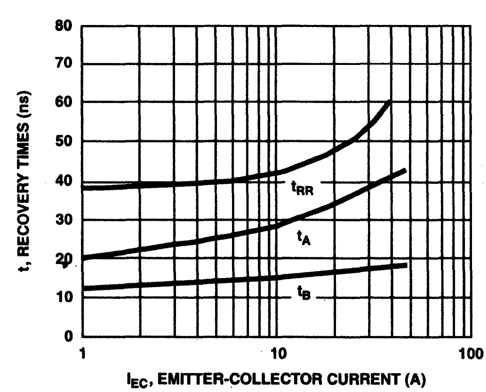


FIGURE 14. TYPICAL t_{RR}, t_A, t_B vs FORWARD CURRENT

Typical Performance Curves (Continued)

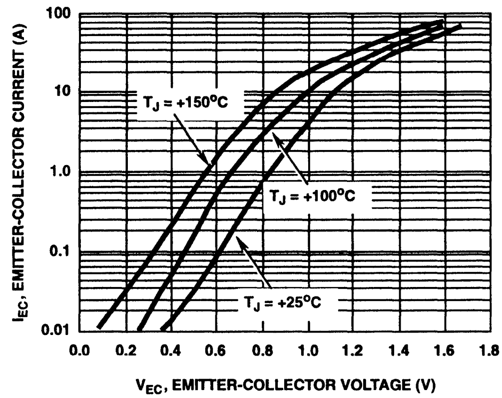


FIGURE 15. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

Test Circuit

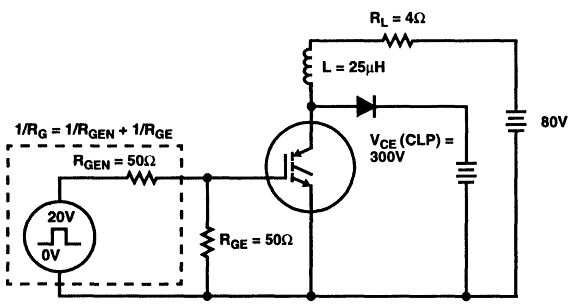


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

HARRIS SEMICONDUCTOR

HGTH20N40C1D, HGTH20N40E1D, HGTH20N50C1D, HGTH20N50E1D

20A, 400V and 500V N-Channel IGBTs with Anti-Parallel Ultrafast Diodes

April 1995

Features

- 20A, 400V and 500V
- $V_{CE(ON)}$ 2.5V Max.
- T_{FALL} 1µs, 0.5µs
- Low On-State Voltage
- Fast Switching Speeds
- High Input Impedance
- Anti-Parallel Diode

Applications

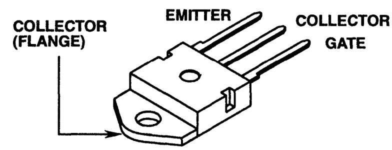
- Power Supplies
- Motor Drives
- Protective Circuits

Description

The HGTH20N40C1D, HGTH20N40E1D, HGTH20N50C1D, and HGTH20N50E1D are n-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drivers. They feature a discrete anti-parallel diode that shunts current around the IGBT in the reverse direction without introducing carriers into the depletion region. These types can be operated directly from low power integrated circuits.

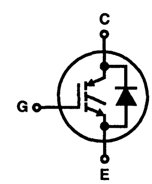
Package

JEDEC TO-218AC



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTH20N40C1D	TO-218AC	G20N40C1D
HGTH20N40E1D	TO-218AC	G20N40E1D
HGTH20N50C1D	TO-218AC	G20N50C1D
HGTH20N50E1D	TO-218AC	G20N50E1D

NOTE: When ordering, use the entire part number.

Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTH20N40C1D HGTH20N40E1D	HGTH20N50C1D HGTH20N50E1D	UNITS
Collector-Emitter Voltage	V_{CES}	400	500	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	V_{CGR}	400	500	V
Gate-Emitter Voltage	V_{GE}	±20	±20	V
Collector Current Continuous	I_C	20	20	A
Collector Current Pulsed	I_{CM}	35	35	A
Diode Forward Current Continuous at $T_C = +25^oC$	I_{F25}	35	35	A
at $T_J = +90^oC$	I_{F90}	20	20	A
Power Dissipation Total at $T_C = +25^oC$	P_D	100	100	W
Power Dissipation Derating $T_C > +25^oC$		0.8	0.8	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2271.4**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			HGTH20N40C1D, HGTH20N40E1D		HGTH20N50C1D, HGTH20N50E1D		
			MIN	MAX	MIN	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 1mA, V_{GE} = 0	400	-	500	-	V
Gate Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, I_C = 1mA	2.0	4.5	2.0	4.5	V
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 400V, T_C = +25°C	-	250	-	-	µA
		V_{CE} = 500V, T_C = +25°C	-	-	-	250	µA
		V_{CE} = 400V, T_C = +125°C	-	1000	-	-	µA
		V_{CE} = 500V, T_C = +125°C	-	-	-	1000	µA
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V, V_{CE} = 0	-	100	-	100	nA
Collector-Emitter On Voltage	$V_{CE(ON)}$	I_C = 20A, V_{GE} = 10V	-	2.5	-	2.5	V
		I_C = 35A, V_{GE} = 20V	-	3.2	-	3.2	V
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = 10A, V_{CE} = 10V	-	6 (Typ)	-	6 (Typ)	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 10A, V_{CE} = 10V	-	33 (Typ)	-	33 (Typ)	nC
Turn-On Delay Time	$t_{D(ON)I}$	I_C = 20A, $V_{CE(CLP)}$ = 300V, L = 25µH, T_J = +100°C, V_{GE} = 10V, R_G = 25Ω	-	50	-	50	ns
Rise Time	t_{RI}		-	50	-	50	ns
Turn-Off Delay Time	$t_{D(OFF)I}$		-	400	-	400	ns
Fall Time	t_{FI}						
40E1D, 50E1D			680 (Typ)	1000	680 (Typ)	1000	ns
40C1D, 50C1D			400 (Typ)	500	400 (Typ)	500	ns
Turn-Off Energy Loss per Cycle (Off Switching Dissipation = W_{OFF} x Frequency)	W_{OFF}	I_C = 20A, $V_{CE(CLP)}$ = 300V, L = 25µH, T_J = +100°C, V_{GE} = 10V, R_G = 25Ω					
40E1D, 50E1D			1810 (Typ)				µJ
40C1D, 50C1D			1070 (Typ)				µJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	1.25	-	1.25	°C/W
Diode Forward Voltage	V_{EC}	I_{EC} = 20A	-	2	-	2	V
Diode Reverse Recovery Time	t_{RR}	I_{EC} = 20A, dI_{EC}/dt = 100A/µs	-	100	-	100	ns

Typical Performance Curves

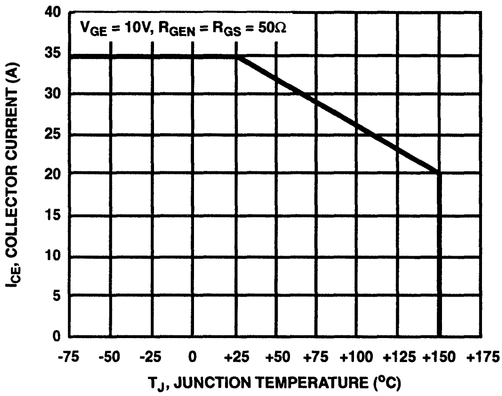


FIGURE 1. MAX. SWITCHING CURRENT LEVEL. $R_G = 50\Omega$, $V_{GE} = 0V$ ARE THE MIN. ALLOWABLE VALUES

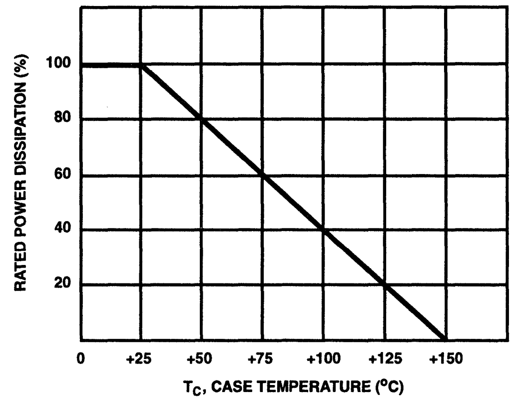


FIGURE 2. POWER DISSIPATION vs TEMPERATURE DERATING CURVE

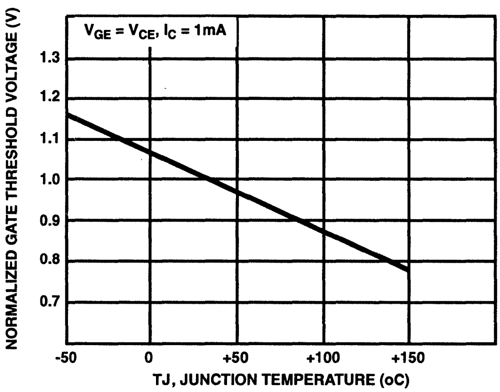


FIGURE 3. TYPICAL NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

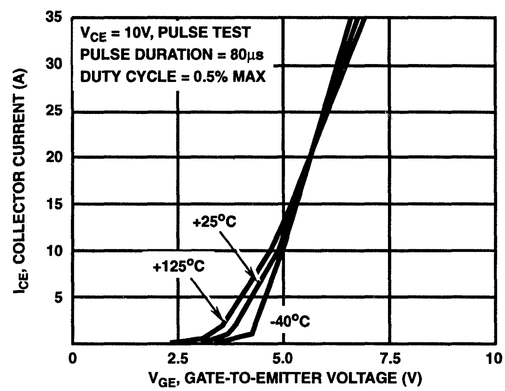


FIGURE 4. TYPICAL TRANSFER CHARACTERISTICS

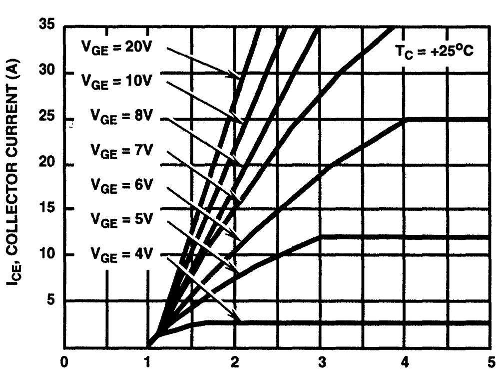


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

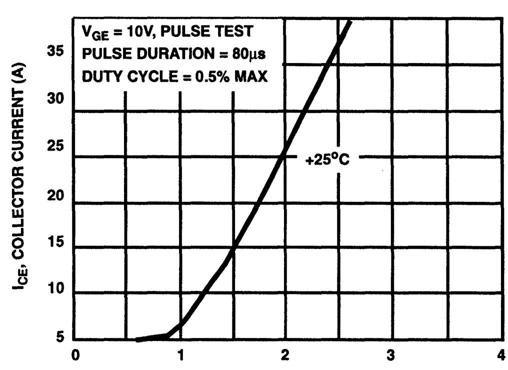


FIGURE 6. TYPICAL COLLECTOR-TO-EMITTER ON-VOLTAGE vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

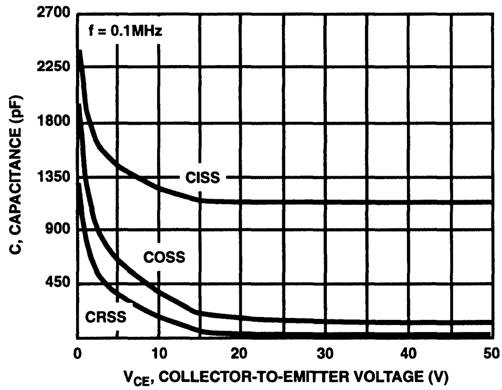


FIGURE 7. CAPACITANCE vs COLLECTOR-TO-EMITTER VOLTAGE

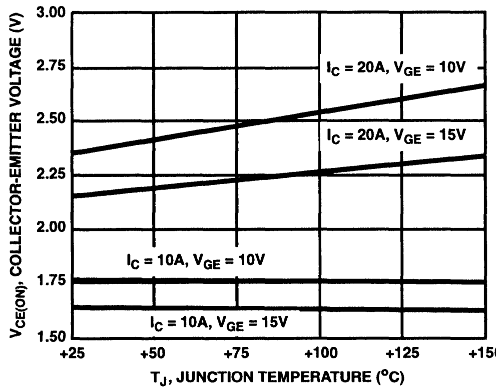


FIGURE 8. TYPICAL $V_{CE(ON)}$ vs TEMPERATURE

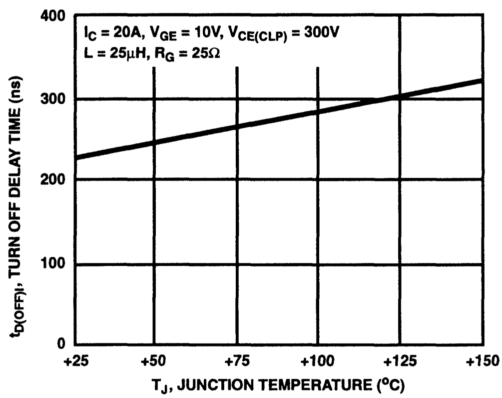


FIGURE 9. TYPICAL TURN-OFF DELAY TIME

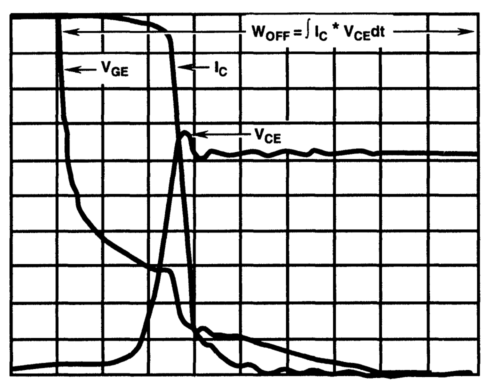


FIGURE 10. TYPICAL INDUCTIVE SWITCHING WAVEFORMS

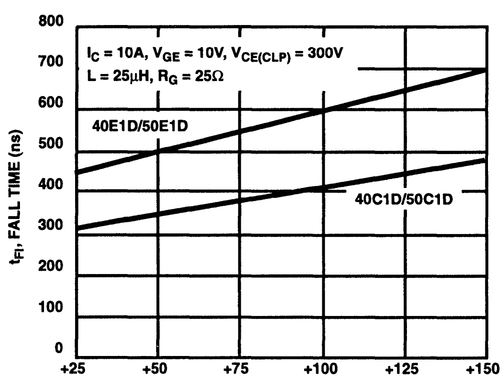


FIGURE 11. TYPICAL FALL TIME (I_C = 10A)

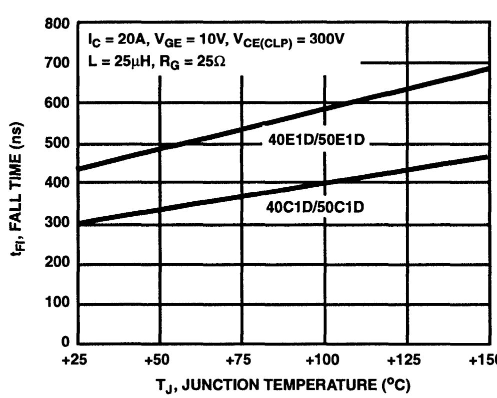


FIGURE 12. TYPICAL FALL TIME (I_C = 20A)

Typical Performance Curves (Continued)

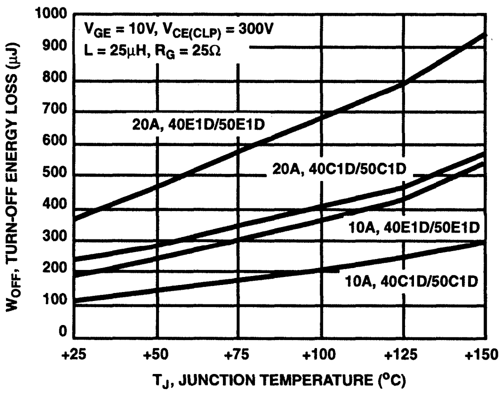
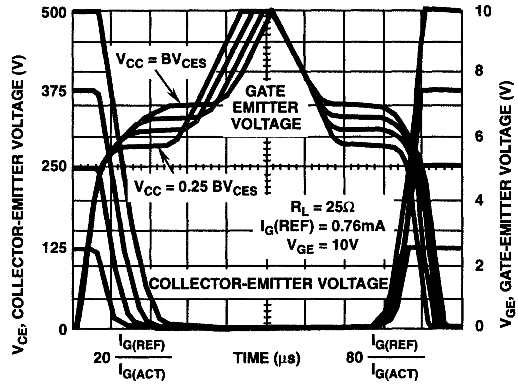


FIGURE 13. TYPICAL CLAMPED INDUCTIVE TURN-OFF SWITCHING LOSS/CYCLE



NOTE: For Turn-Off gate currents in excess of 3mA. V_{CE} Turn-Off is not accurately represented by this normalization.

FIGURE 14. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

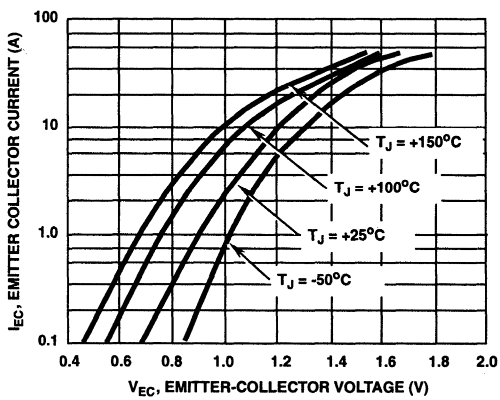


FIGURE 15. TYPICAL DIODE EMITTER-COLLECTOR VOLTAGE vs CURRENT

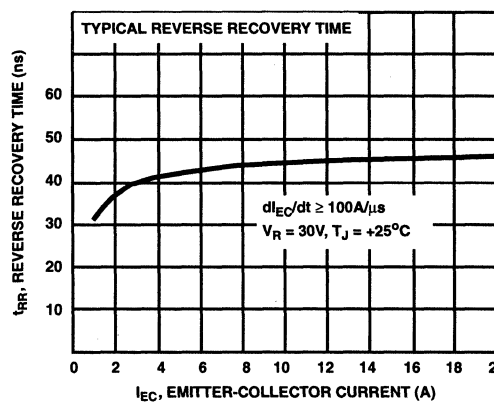


FIGURE 16. TYPICAL DIODE REVERSE RECOVERY TIME

Test Circuit

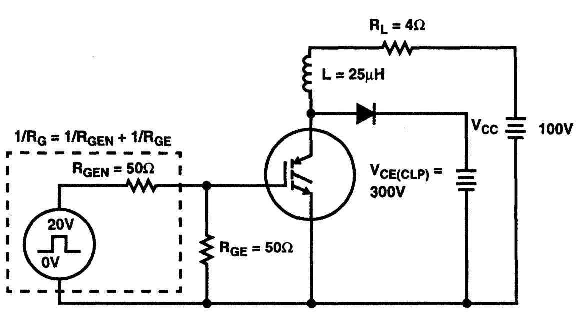


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUIT

HGTP20N60B3

March 1995

40A, 600V, UFS Series N-Channel IGBT

Features

- 40A, 600V at $T_C = +25^oC$
- Square Switching SOA Capability
- Typical Fall Time - 140ns at $+150^oC$
- Short Circuit Rated
- Low Conduction Loss

Description

The HGTP20N60B3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

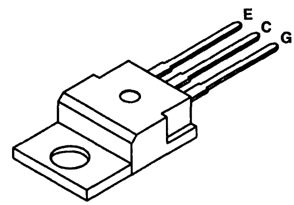
PART NUMBER	PACKAGE	BRAND
HGTP20N60B3	TO-220AB	G20N60B3

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49050.

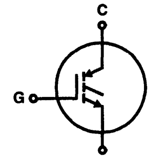
Package

JEDEC TO-220AB



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTP20N60B3	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous			
At $T_C = +25^oC$	I_{C25}	40	A
At $T_C = +110^oC$	I_{C110}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = +150^oC$	SSOA	80A at 0.8 BV_{CES}	
Power Dissipation Total at $T_C = +25^oC$	P_D	165	W
Power Dissipation Derating $T_C > +25^oC$		1.32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

NOTE:
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3723.1**

Electrical Specifications
$T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	250	µA
		$V_{CE} = BV_{CES}$	$T_C = +150^oC$	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C110}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.8	2.0	V
			$T_C = +150^oC$	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Latching Current	I_L	$T_C = +150^oC$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 10\Omega$ $L = 45\mu H$		80	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$		-	8.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C110}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	80	105	nC
			$V_{GE} = 20V$	-	105	135	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_C = 150^oC$ $I_{CE} = I_{C110}$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 10\Omega$ $L = 100\mu H$		-	25	-	ns
Current Rise Time	t_{RI}			-	20	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	220	275	ns
Current Fall Time	t_{FI}			-	140	200	ns
Turn-On Energy	E_{ON}			-	475	-	µJ
Turn-Off Energy (Note 1)	E_{OFF}			-	1050	-	µJ
Thermal Resistance	$R_{\theta JC}$			-	-	0.76	$^oC/W$

NOTE:

1. Turn-off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTP20N60B3 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

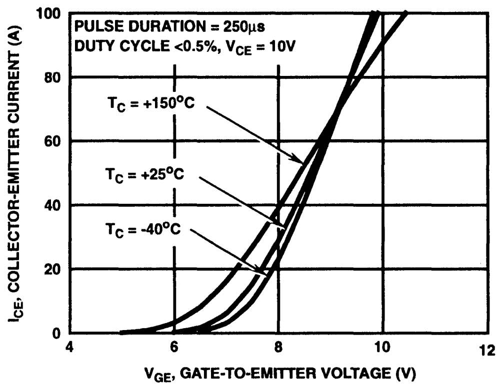


FIGURE 1. TRANSFER CHARACTERISTICS

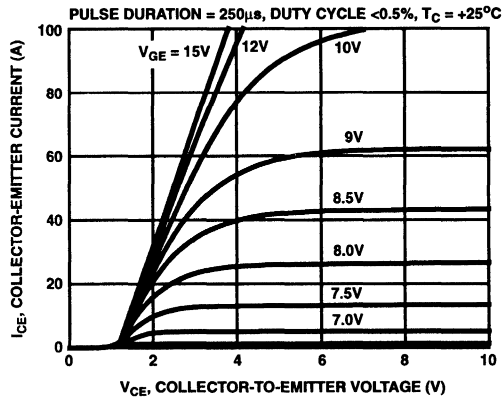


FIGURE 2. SATURATION CHARACTERISTICS

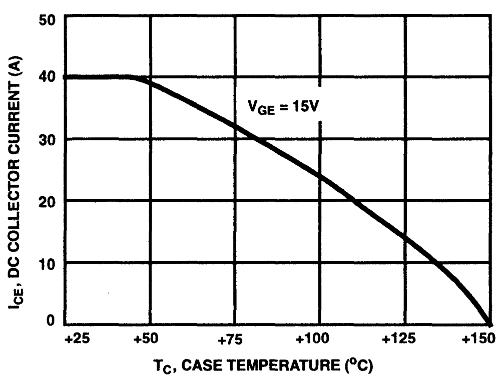


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

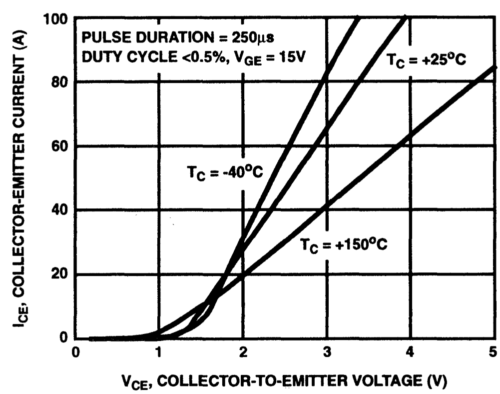


FIGURE 4. COLLECTOR-EMITTER ON - STATE VOLTAGE

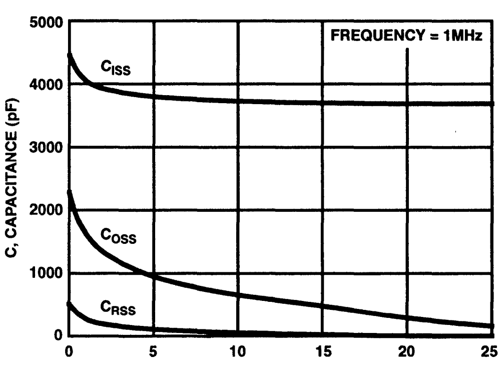


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

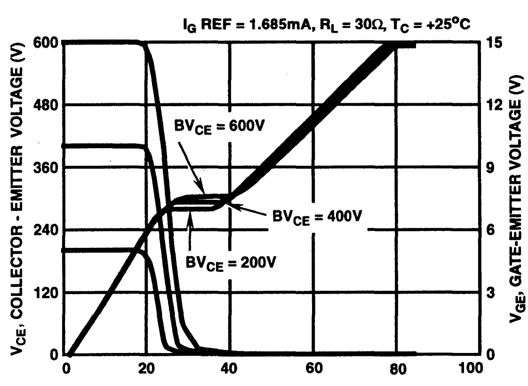


FIGURE 6. GATE CHARGE WAVEFORMS

Typical Performance Curves (Continued)

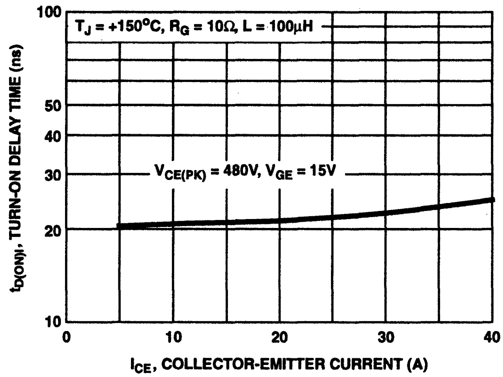


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

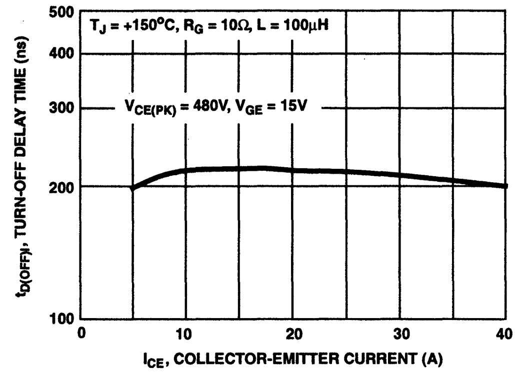


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

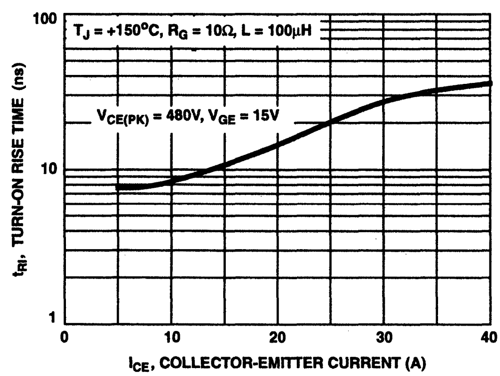


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

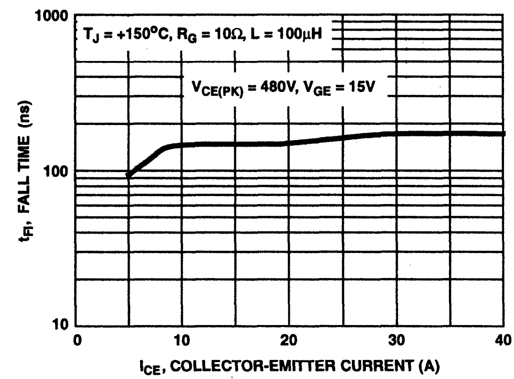


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

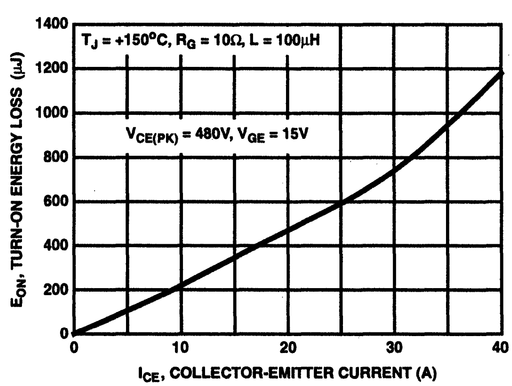


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

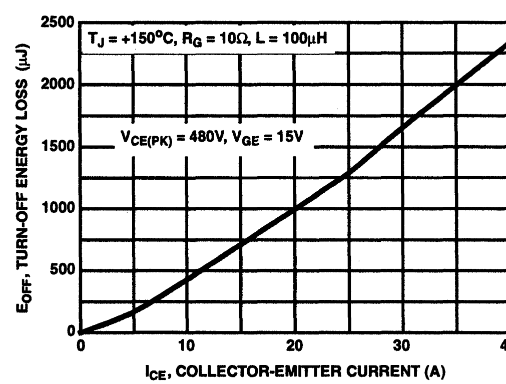


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

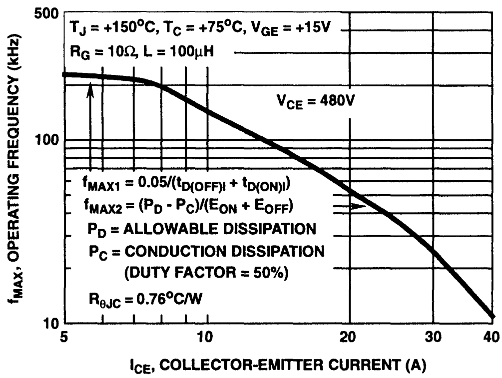


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

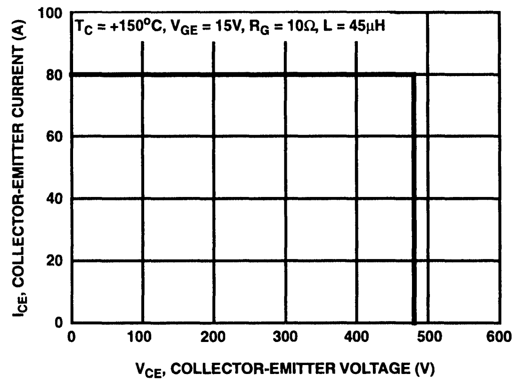


FIGURE 14. SWITCHING SAFE OPERATING AREA

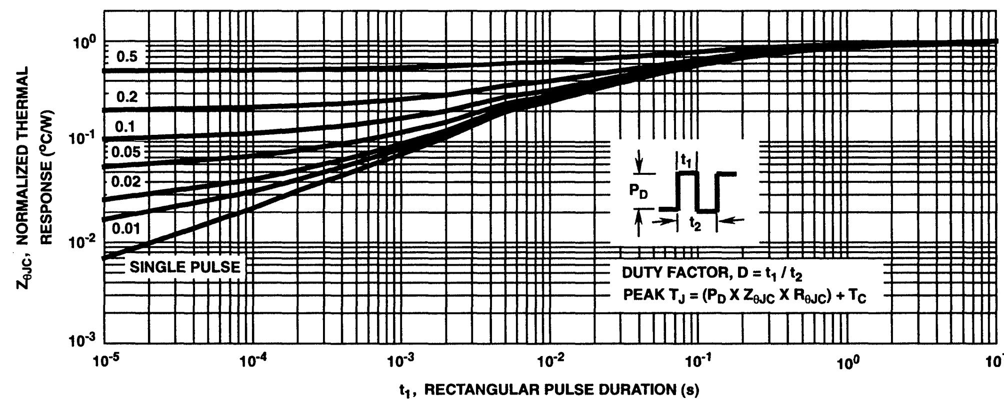


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$.

The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn-on and E_{OFF} is the integral of the instantaneous power loss (I_{CE} x V_{CE}) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero (I_{CE} = 0).

Test Circuit

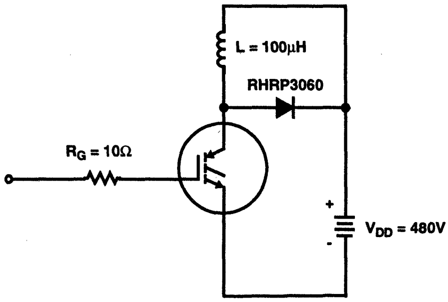


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

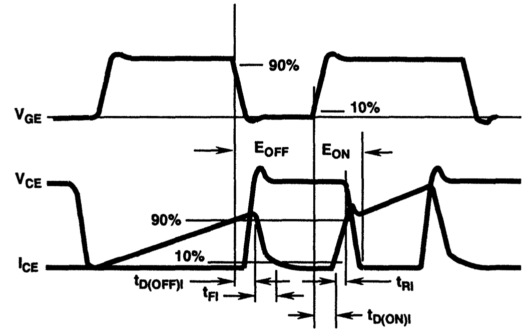


FIGURE 17. SWITCHING TEST WAVEFORMS

Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "†ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR HGTG20N60B3D

40A, 600V, UFS Series N-Channel IGBT with Anti-Parallel Hyperfast Diode

May 1995

Features

- 40A, 600V at $T_C = +25^oC$
- Typical Fall Time - 140ns at $+150^oC$
- Short Circuit Rated
- Low Conduction Loss
- Hyperfast Anti-Parallel Diode

Description

The HGTG20N60B3D is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in anti-parallel with the IGBT is the RHRP3060.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential.

PACKAGING AVAILABILITY

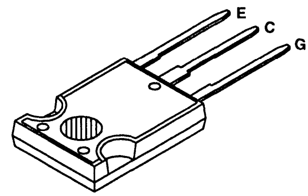
PART NUMBER	PACKAGE	BRAND
HGTG20N60B3D	TO-247	G20N60B3D

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49016.

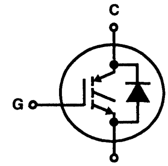
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTG20N60B3D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous			
At $T_C = +25^oC$	I_{C25}	40	A
At $T_C = +110^oC$	I_{C110}	20	A
Average Diode Forward Current at +110°C	$I_{(AVG)}$	20	A
Collector Current Pulsed (Note 1)	I_{CM}	160	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = +150^oC$	SSOA	80A at 0.8 BV_{CES}	
Power Dissipation Total at $T_C = +25^oC$	P_D	165	W
Power Dissipation Derating $T_C > +25^oC$		1.32	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	4	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

3

IGBTs

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 3739.2

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = BV_{CES}	T_C = +150°C	-	-	2.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C110}, V_{GE} = 15V	T_C = +25°C	-	1.8	2.0	V
			T_C = +150°C	-	2.1	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 250μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	5.0	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±100	nA
Latching Current	I_L	T_C = +150°C, $V_{CE(PK)}$ = 0.8 BV_{CES}, V_{GE} = 15V, R_G = 10Ω, L = 45μH		80	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}		-	8.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = I_{C110}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	80	105	nC
			V_{GE} = 20V	-	105	135	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	T_C = +150°C, I_{CE} = I_{C110}, $V_{CE(PK)}$ = 0.8 BV_{CES}, V_{GE} = 15V, R_G = 10Ω, L = 100μH		-	25	-	ns
Current Rise Time	t_{RI}			-	20	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	220	275	ns
Current Fall Time	t_{FI}			-	140	200	ns
Turn-On Energy	E_{ON}			-	475	-	μJ
Turn-Off Energy (Note 1)	E_{OFF}			-	1050	-	μJ
Diode Forward Voltage	V_{EC}	I_{EC} = 20A		-	1.5	1.9	V
Diode Reverse Recovery Time	t_{RR}	I_{EC} = 20A, dI_{EC}/dt = 100A/μs		-	-	55	ns
		I_{EC} = 1A, dI_{EC}/dt = 100A/μs		-	-	45	ns
Thermal Resistance	$R_{θJC}$	IGBT		-	-	0.76	°C/W
		Diode		-	-	1.2	°C/W

NOTE:

1. Turn-off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTG20N60B3D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

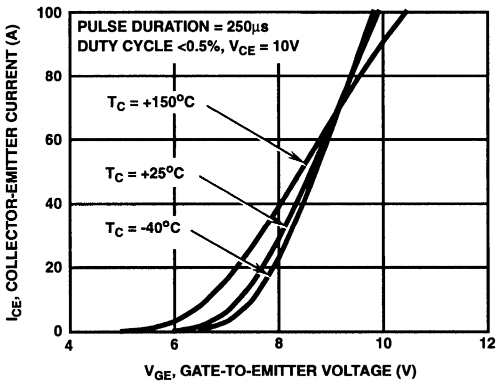


FIGURE 1. TRANSFER CHARACTERISTICS

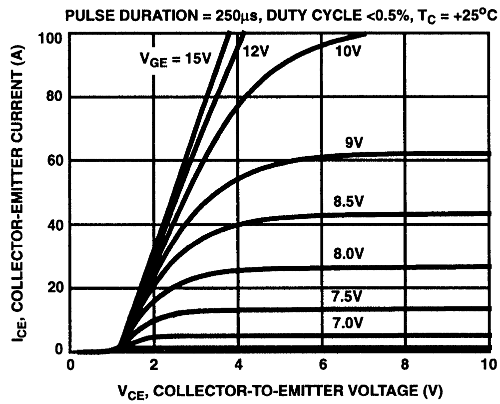


FIGURE 2. SATURATION CHARACTERISTICS

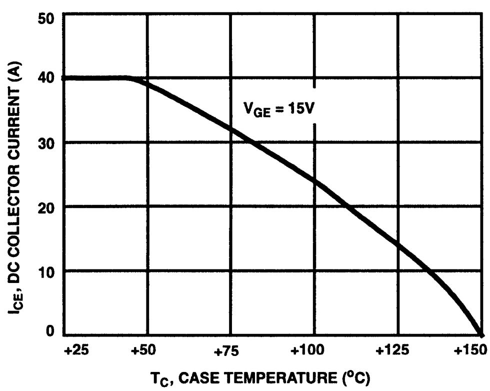


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

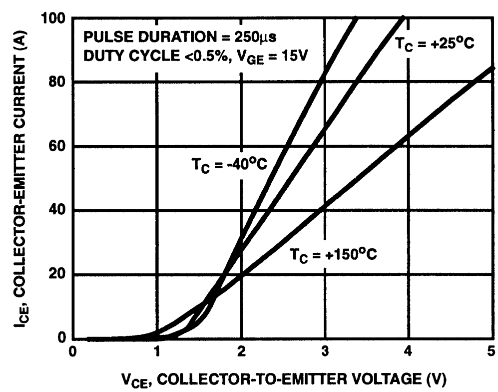


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

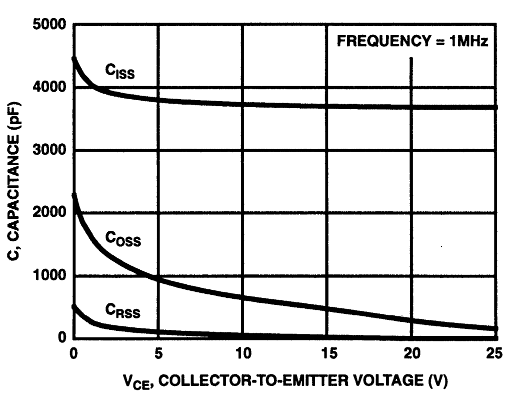


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

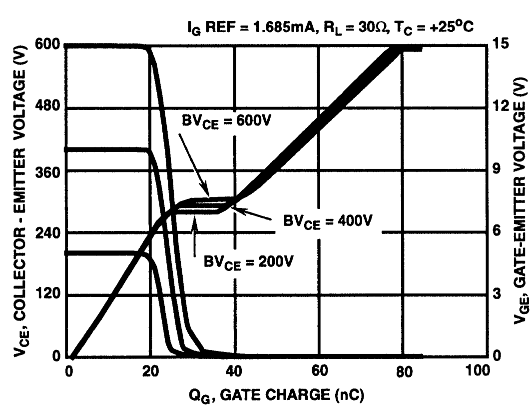


FIGURE 6. GATE CHARGE WAVEFORMS

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IGBTs

Typical Performance Curves (Continued)

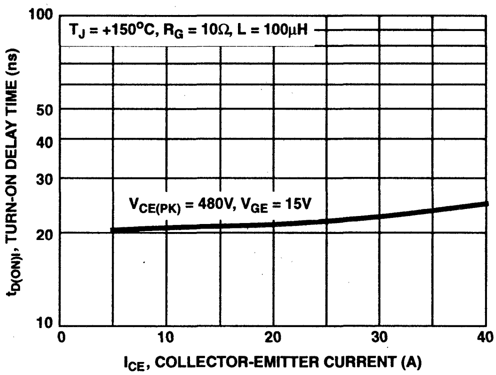

FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

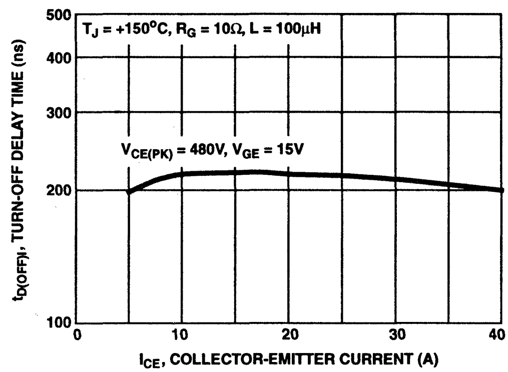

FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

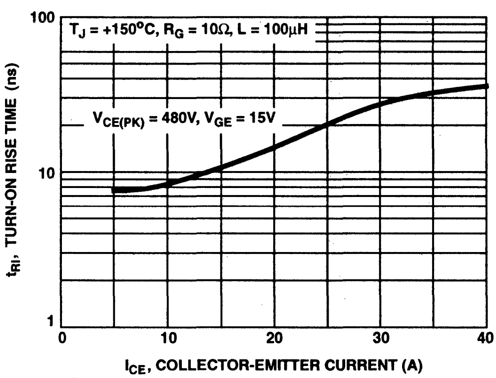

FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

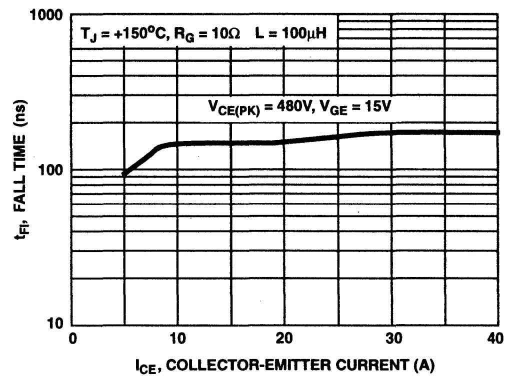

FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

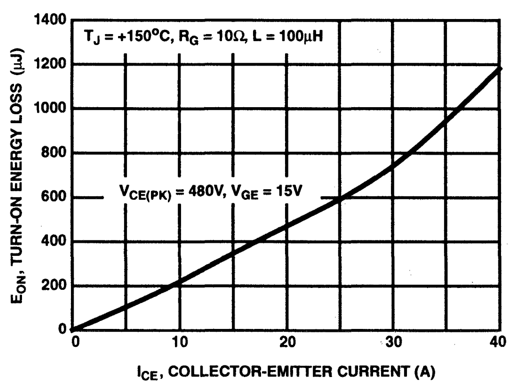

FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

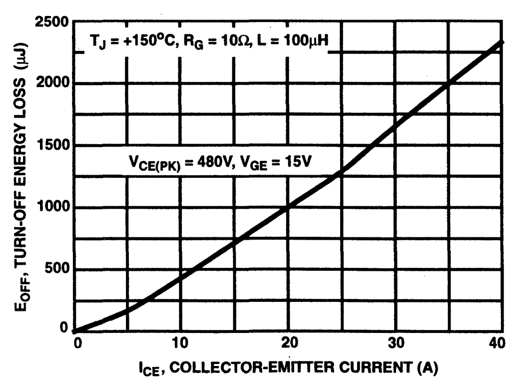

FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

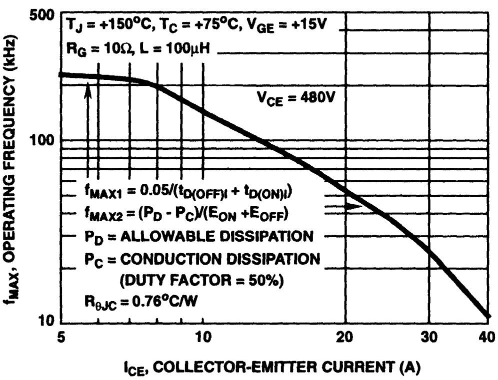

FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

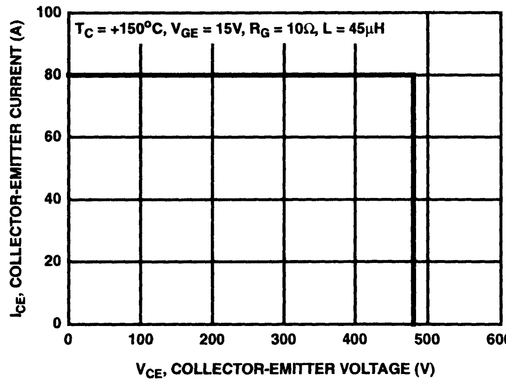

FIGURE 14. SWITCHING SAFE OPERATING AREA

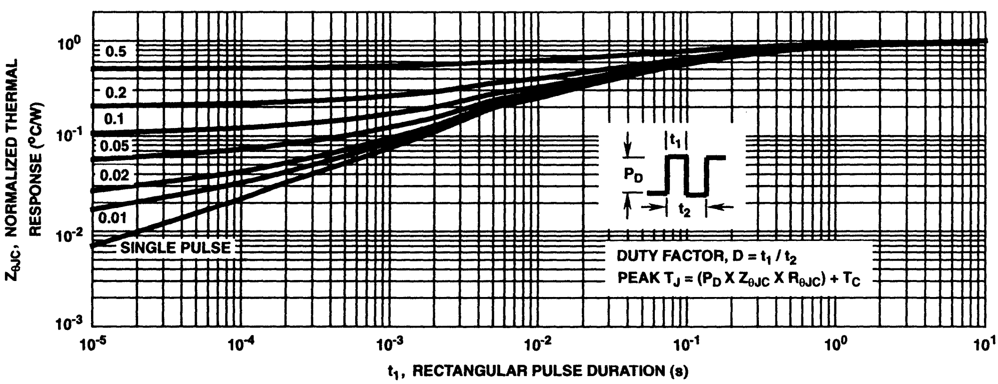

FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

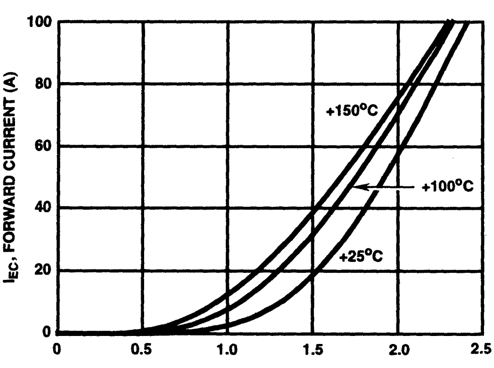

FIGURE 16. DIODE FORWARD CURRENT AS A FUNCTION OF FORWARD VOLTAGE DROP

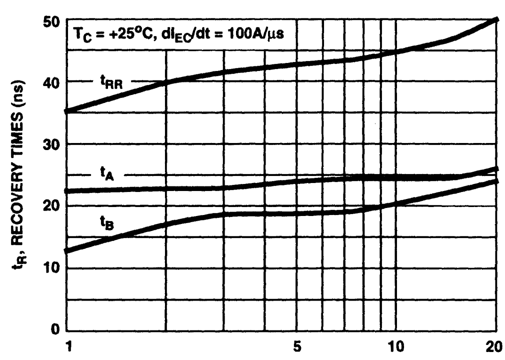

FIGURE 17. RECOVERY TIMES AS A FUNCTION OF FORWARD CURRENT

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IGBTs

Test Circuit and Waveforms

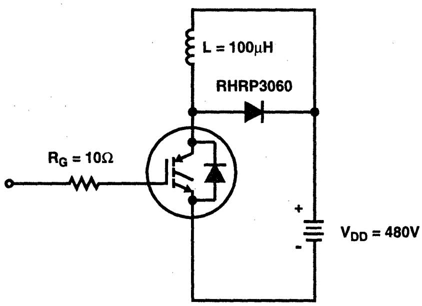


FIGURE 18. INDUCTIVE SWITCHING TEST CIRCUIT

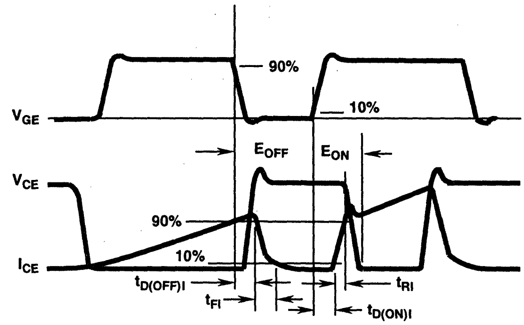


FIGURE 19. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on- state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 19.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 19. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e. the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and discharge procedures, however, IGBT's are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †"ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

†Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR

HGTG20N100D2

May 1995

20A, 1000V N-Channel IGBT

Features

- 34A, 1000V
- Latch Free Operation
- Typical Fall Time 520ns
- High Input Impedance
- Low Conduction Loss

Description

The HGTG20N100D2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

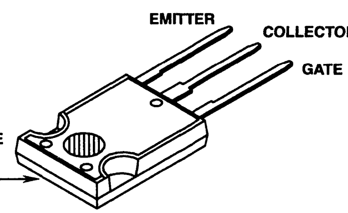
IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG20N100D2	TO-247	G20N100D2

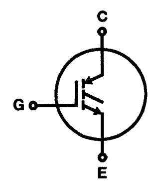
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



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IGBTs

Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		HGTG20N100D2	UNITS
Collector-Emitter Voltage	BV_{CES}	1000	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	BV_{CGR}	1000	V
Collector Current Continuous at $T_C = +25°C$	I_{C25}	34	A
at $T_C = +90°C$	I_{C90}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	100	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = +150°C$	SSOA	100A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25°C$	P_D	150	W
Power Dissipation Derating $T_C > +25°C$		1.20	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125 inch from case for 5 seconds)	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	3	µs
at $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 600V$, $T_C = +125°C$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2826.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250mA$, $V_{GE} = 0V$		1000	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	250	μA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	3.1	3.8	V
			$T_C = +125^oC$	-	2.9	3.6	V
		$I_C = I_{C90}$, $V_{GE} = 10V$	$T_C = +25^oC$	-	3.3	4.1	V
			$T_C = +125^oC$	-	3.2	4.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 500\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±250	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.1	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	120	160	nC
			$V_{GE} = 20V$	-	163	212	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	500	650	ns
Current Fall Time	t_{FI}			-	520	680	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	3.7	-	mJ
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 10V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off	$t_{D(OFF)I}$			-	410	530	ns
Current Fall Time	t_{FI}			-	520	680	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	3.7	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.7	0.83	°C/W

NOTE: 1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG20N100D2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

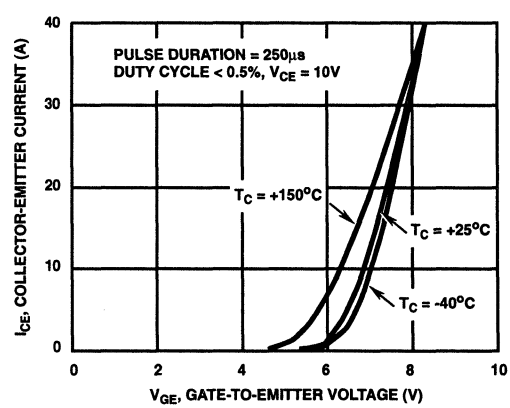


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

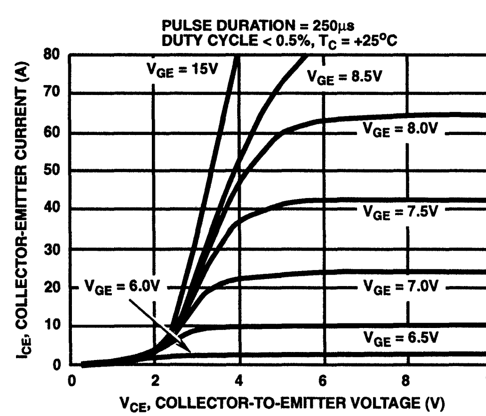


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

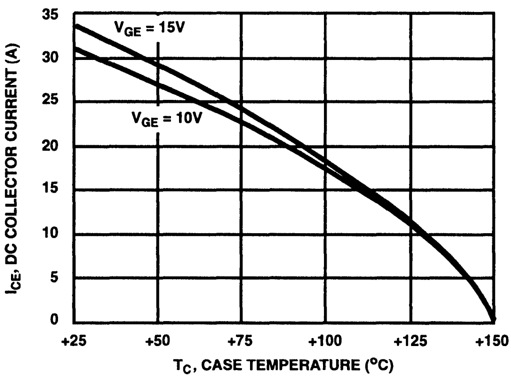


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

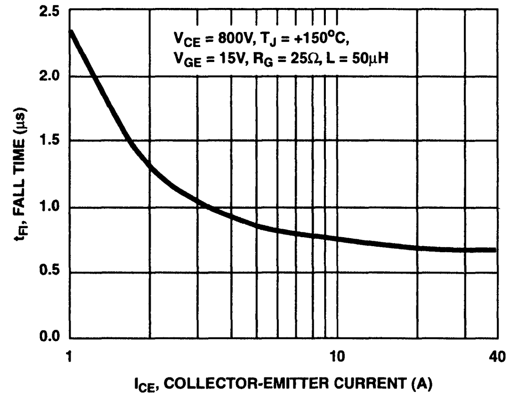


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

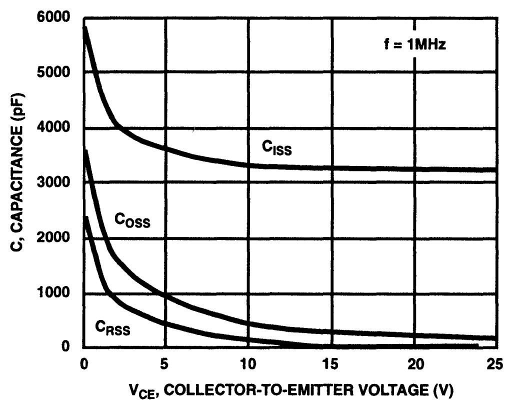


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

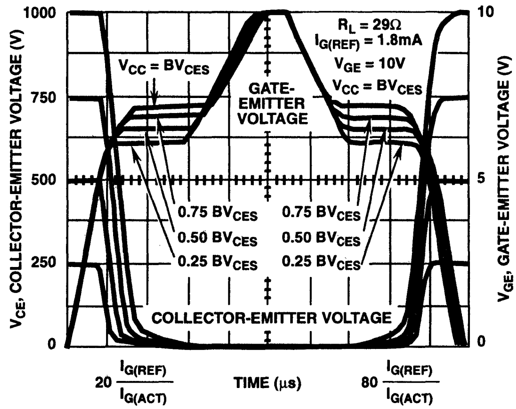


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

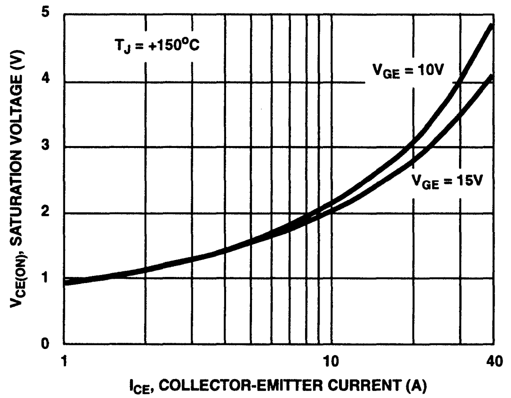


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

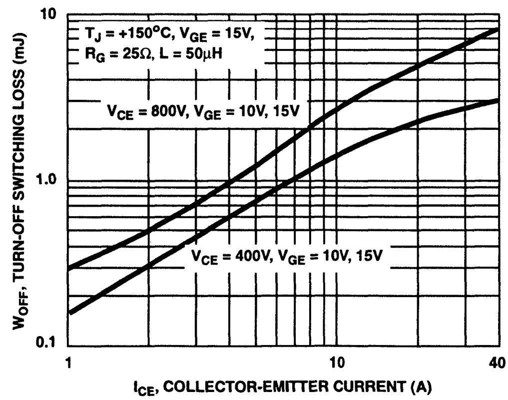


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

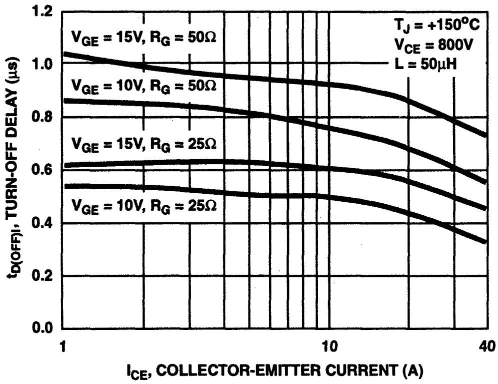
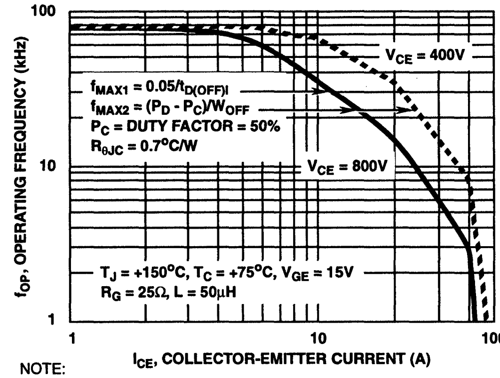


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

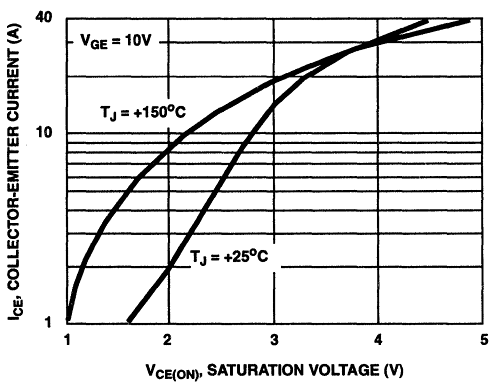


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

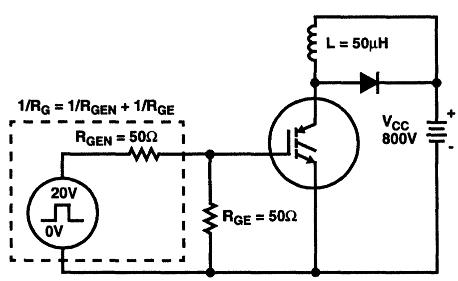


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR HGTG20N120E2

April 1995

34A, 1200V N-Channel IGBT

Features

- 34A, 1200V
- Latch Free Operation
- Typical Fall Time - 780ns
- High Input Impedance
- Low Conduction Loss

Description

The HGTG20N120E2 is a MOS gated, high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

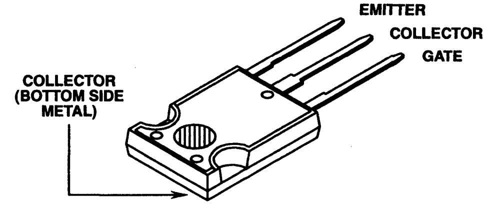
IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors. The development type number for this device is TA49009.

PACKAGING AVAILABILITY

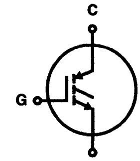
PART NUMBER	PACKAGE	BRAND
HGTG20N120E2	TO-247	G20N120E2

Package

JEDEC STYLE TO-247



Terminal Diagram



Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		HGTG20N120E2	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	1200	V
Collector-Gate Breakdown Voltage $R_{GE} = 1M\Omega$	BV_{CGR}	1200	V
Collector Current Continuous			
At $T_C = +25°C$	I_{C25}	34	A
At $T_C = +90°C$	I_{C90}	20	A
Collector Current Pulsed (Note 1)	I_{CM}	100	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching SOA at $T_C = +150°C$	SSOA	100A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25°C$	P_D	150	W
Power Dissipation Derating $T_C > +25°C$		1.20	W/°C
Operating and Storage Junction Temperature	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5 seconds)	T_L	260	°C
Short Circuit Withstand Time (Note 2)			
At $V_{GE} = 15V$	t_{SC}	3	µs
At $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 720V$, $T_C = +125°C$, $R_{GE} = 25\Omega$

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3370.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		1200	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	2.9	3.5	V
			T_C = +125°C	-	3.0	3.6	V
		I_C = I_{C90}, V_{GE} = 10V	T_C = +25°C	-	3.1	3.8	V
			T_C = +125°C	-	3.3	4.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 500μA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±250	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	7.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	110	150	nC
			V_{GE} = 20V	-	150	200	nC
Current Turn-on Delay Time	$t_{D(ON)}$	R_L = 48Ω	I_C = I_{C90}, V_{GE} = 15V, V_{CE} = 0.8 BV_{CES}, R_G = 25Ω, T_J = +125°C	-	100	-	ns
Current Rise Time	t_R			-	150	-	ns
Current Turn-off Delay Time	$t_{D(OFF)I}$	L = 50μH		-	520	620	ns
Current Fall Time	t_{FI}			-	780	1000	ns
Turn-off Energy (Note 1)	W_{OFF}			-	7.0	-	mJ
Current Turn-on Delay Time	$t_{D(ON)}$	R_L = 48Ω	I_C = I_{C90}, V_{GE} = 10V, V_{CE} = 0.8 BV_{CES}, R_G = 25Ω, T_J = +125°C	-	100	-	ns
Current Rise Time	t_R			-	150	-	ns
Current Turn-off Delay Time	$t_{D(OFF)I}$	L = 50μH		-	420	520	ns
Current Fall Time	t_{FI}			-	780	1000	ns
Turn-off Energy (Note 1)	W_{OFF}			-	7.0	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.70	0.83	°C/W

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). The HGTG20N120E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

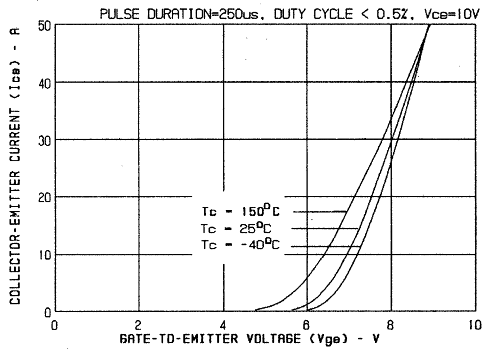


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

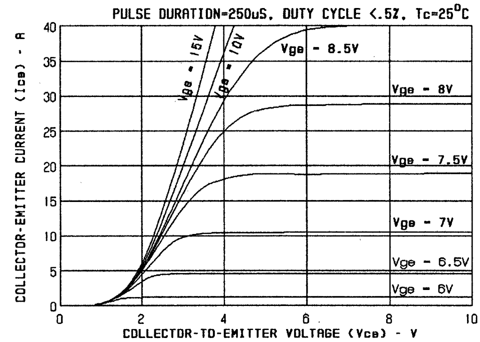


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

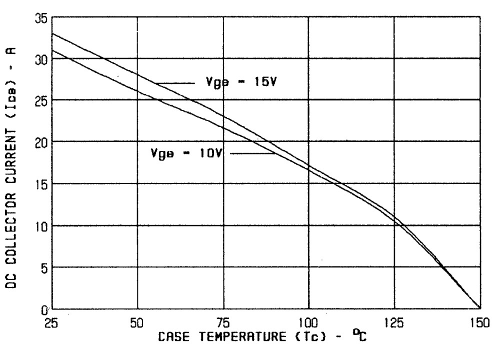


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

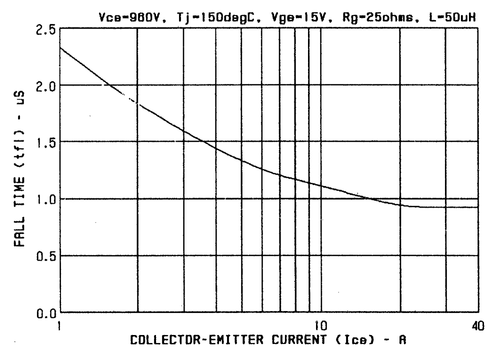


FIGURE 4. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

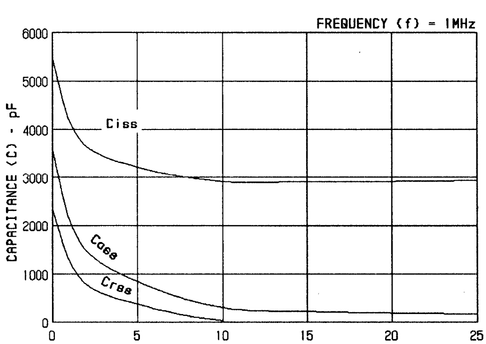


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

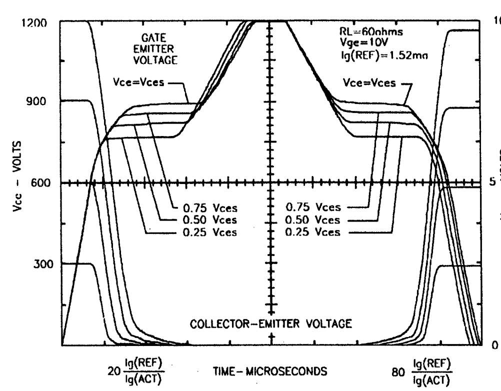


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

Typical Performance Curves (Continued)

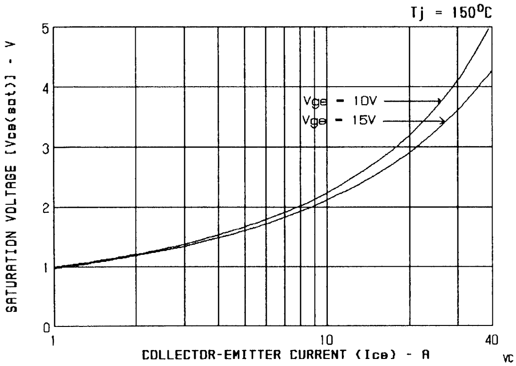


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

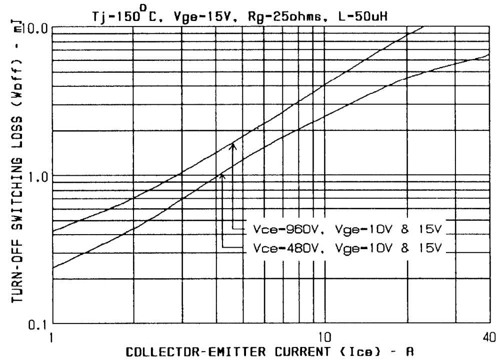


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

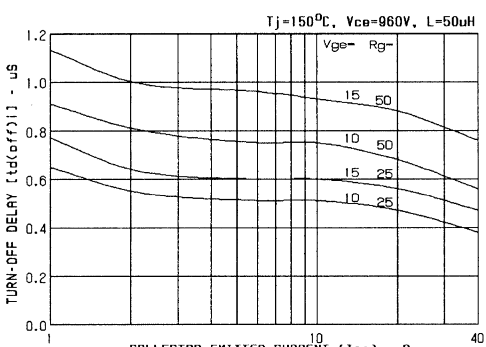


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

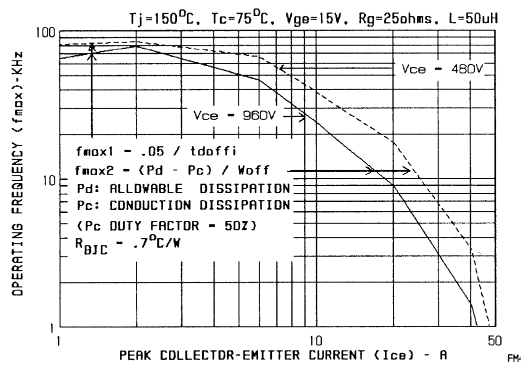


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

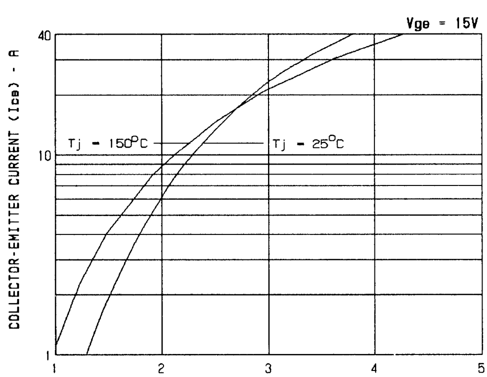


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

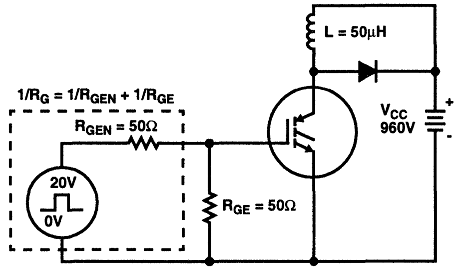


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition. f_{MAX2} is defined by $f_{MAX2} = (Pd - Pc)/W_{OFF}$. The allowable dissipation (Pd) is defined by $Pd = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed Pd. A 50% duty factor was used (Figure 10) and the conduction losses (Pc) are approximated by $Pc = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "† ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of VGEM. Exceeding the rated VGE can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR

HGTG24N60D1

May 1995

24A, 600V N-Channel IGBT

3

IGBTs

Features

- 24A, 600V
- Latch Free Operation
- Typical Fall Time <500ns
- High Input Impedance
- Low Conduction Loss

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

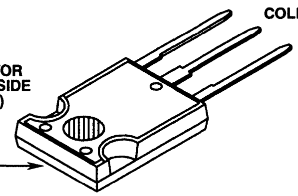
IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG24N60D1	TO-247	G24N60D1

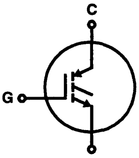
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specific

		HGTG24N60D1	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	40	A
at $V_{GE} = 15V$ at $T_C = +90^oC$	I_{C90}	24	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at $T_J = +150^oC$	SSOA	60A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25^oC$	P_D	125	W
Power Dissipation Derating $T_C > +25^oC$		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125 inch from case for 5s)	T_L	260	°C

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	mA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.7	2.3	V
			$T_C = +125^oC$	-	1.9	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	6.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	120	155	nC
			$V_{GE} = 20V$	-	155	200	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 500\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +150^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	700	900	ns
Current Fall Time	t_{FI}			-	450	600	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	4.3	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	-	1.00	$^oC/W$

NOTE: 1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG24N60D1 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

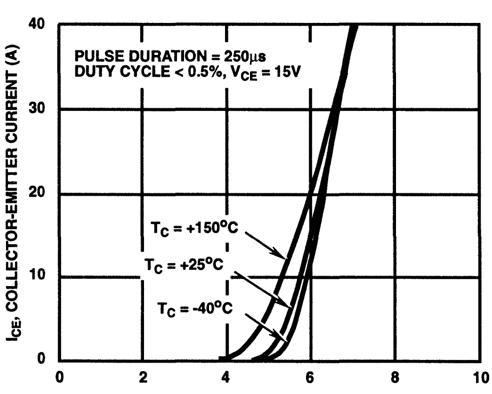


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

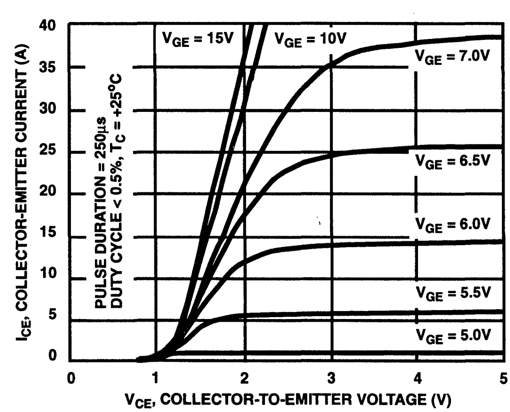


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

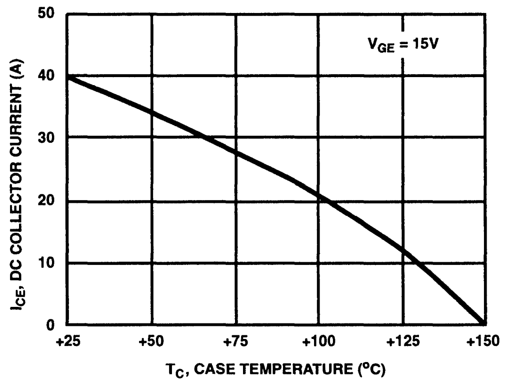


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

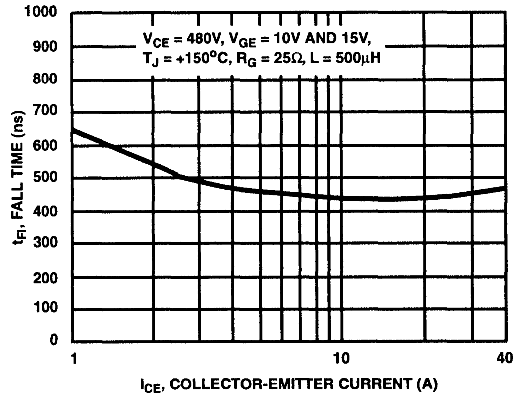


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

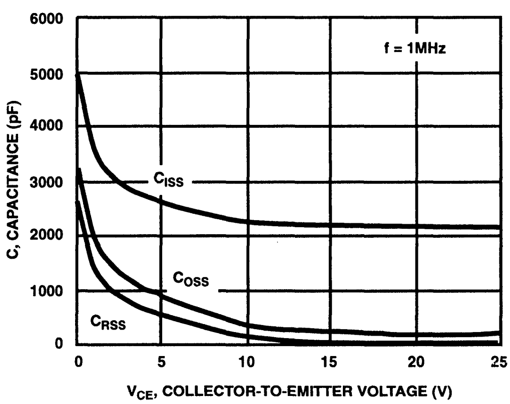


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

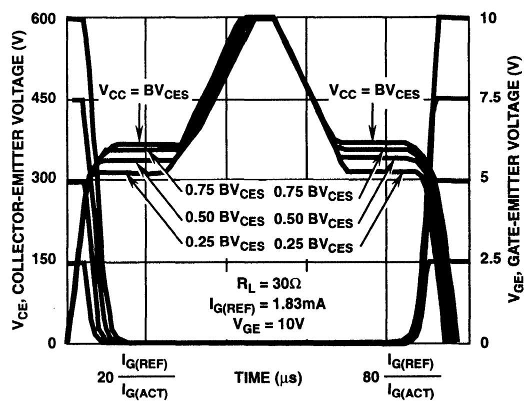


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

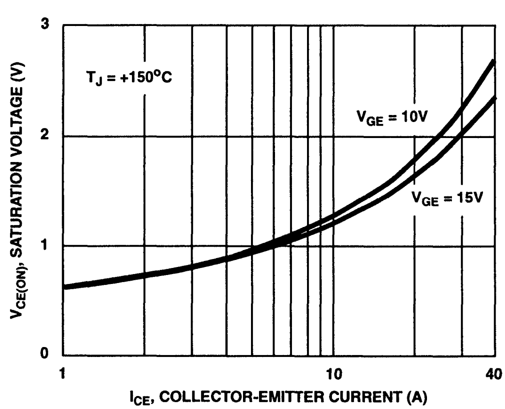


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

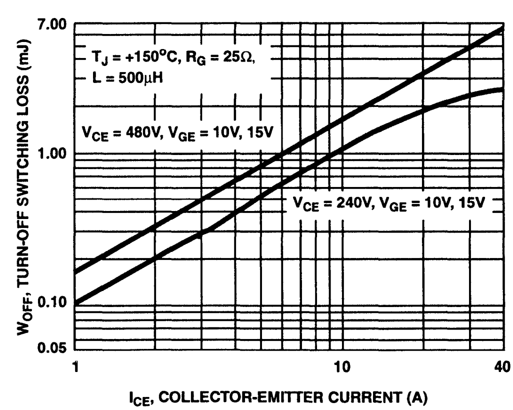


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

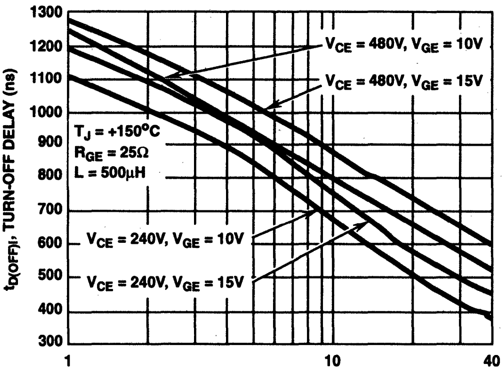
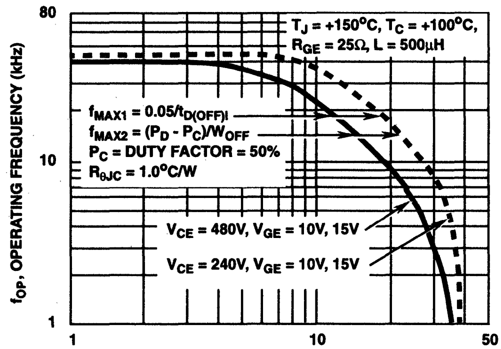


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

HGTG24N60D1D

24A, 600V N-Channel IGBT with Anti-Parallel Ultrafast Diode

April 1995

Features

- 24A, 600V
- Latch Free Operation
- Typical Fall Time <500ns
- Low Conduction Loss
- With Anti-Parallel Diode
- t_{RR} < 60ns

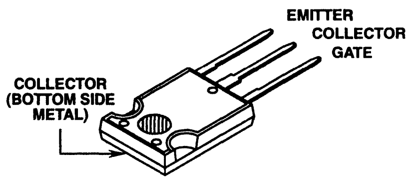
Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C. The diode used in parallel with the IGBT is an ultrafast (t_{RR} < 60ns) with soft recovery characteristic.

The IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

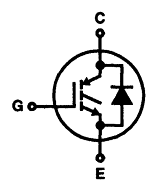
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG24N60D1D	TO-247	G24N60D1D

NOTE: When ordering, use the entire part number.

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specific

		HGTG24N60D1D	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage R_{GE} = 1MΩ	BV_{CGR}	600	V
Collector Current Continuous at T_C = +25°C	I_{C25}	40	A
at T_C = +90°C	I_{C90}	24	A
Collector Current Pulsed (Note 1)	I_{CM}	96	A
Gate-Emitter Voltage Continuous	V_{GES}	±25	V
Switching Safe Operating Area at T_J = +150°C	SSOA	60A at 0.8 BV_{CES}	-
Diode Forward Current at T_C = +25°C	I_{F25}	40	A
at T_C = +90°C	I_{F90}	24	A
Power Dissipation Total at T_C = +25°C	P_D	125	W
Power Dissipation Derating T_C > +25°C		1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.125 inch from case for 5s)	T_L	260	°C

NOTE: 1. Repetitive Rating: Pulse width limited by maximum junction temperature.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2797.4**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 280\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	280	µA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	5.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	1.7	2.3	V
			$T_C = +125^oC$	-	1.9	2.5	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	6.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	120	155	nC
			$V_{GE} = 20V$	-	155	200	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 500\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +150^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	700	900	ns
Current Fall Time	t_{FI}			-	450	600	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	4.3	-	mJ
Thermal Resistance (IGBT)	$R_{\theta JC}$			-	-	1.00	$^oC/W$
Thermal Resistance Diode	$R_{\theta JC}$			-	-	1.50	$^oC/W$
Diode Forward Voltage	V_{EC}	$I_{EC} = 24A$		-	-	1.50	V
Diode Reverse Recovery Time	t_{RR}	$I_{EC} = 24A$, $di/dt = 100A/\mu s$		-	-	60	ns

NOTE: 1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG24N60D1D was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

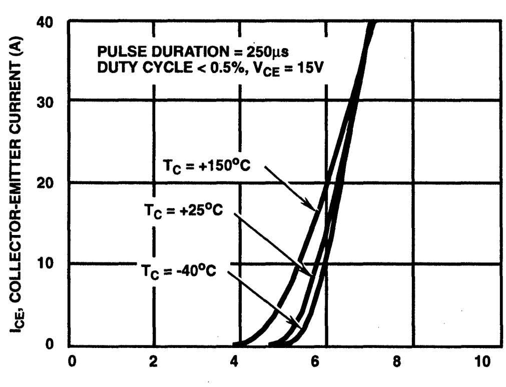


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

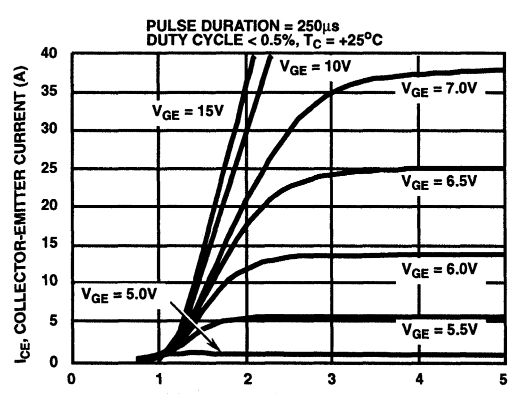


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

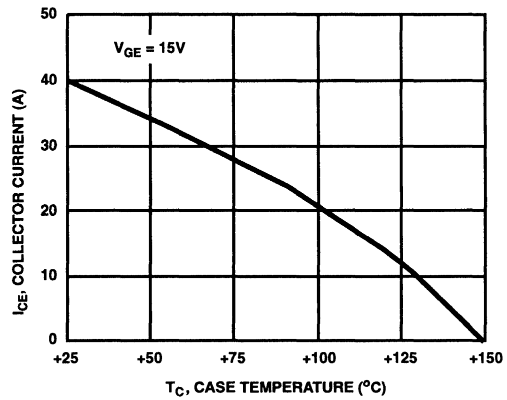


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

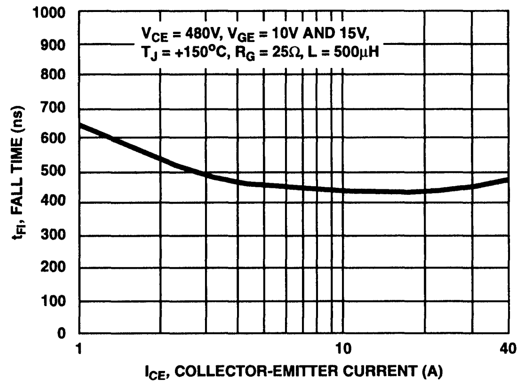


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

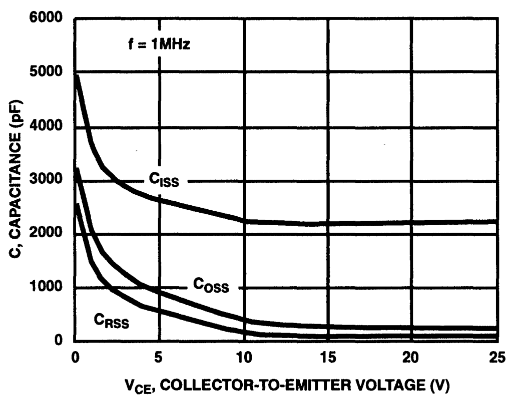


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

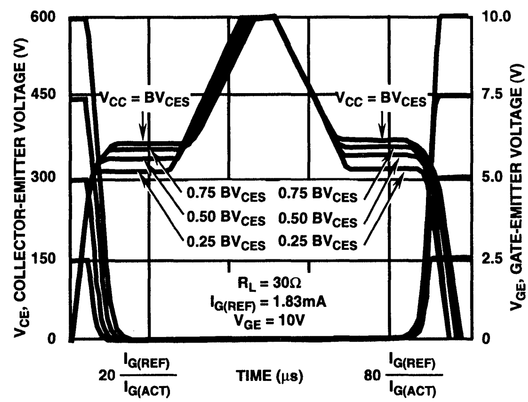


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

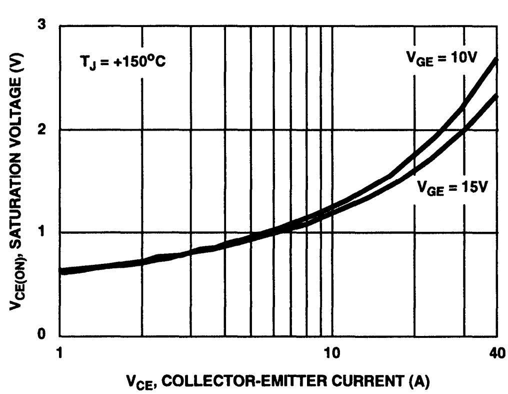


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

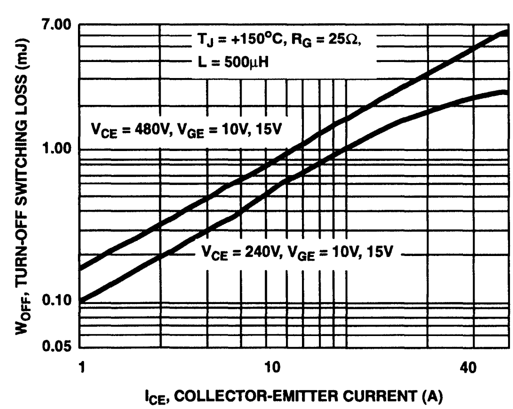


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

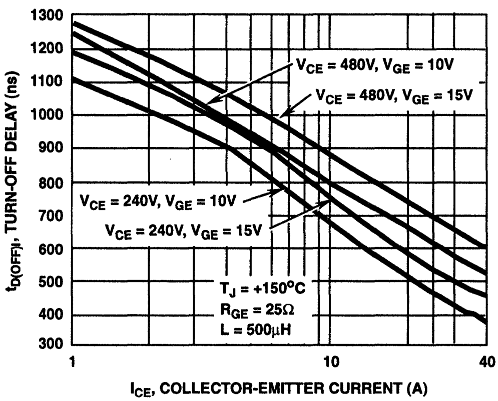
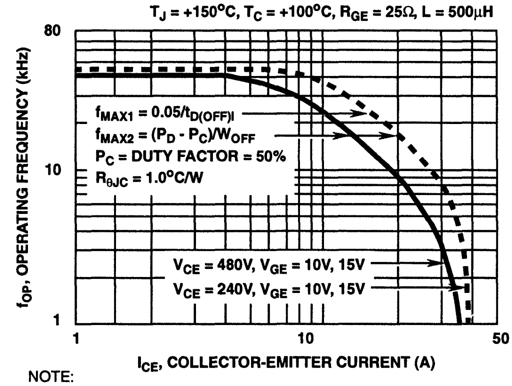


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

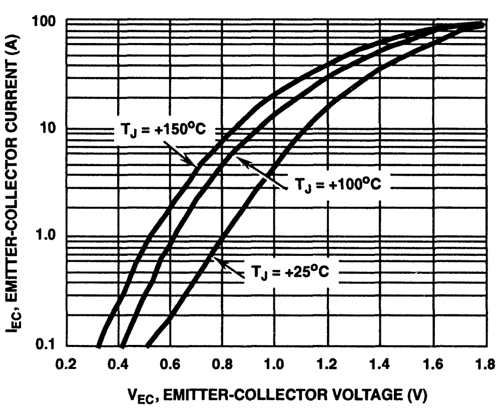


FIGURE 11. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

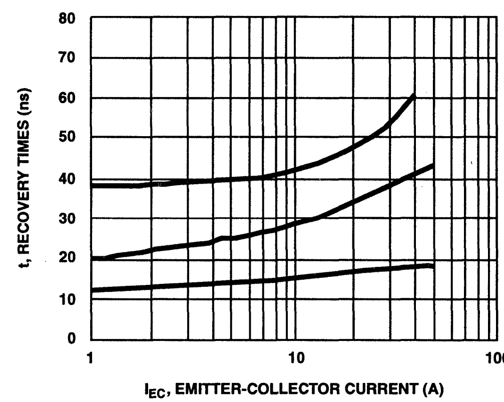


FIGURE 12. TYPICAL t_{RR}, t_A, t_B vs FORWARD CURRENT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

HGTG30N120D2

April 1995

30A, 1200V N-Channel IGBT

Features

- 30A, 1200V
- Latch Free Operation
- Typical Fall Time - 580ns
- High Input Impedance
- Low Conduction Loss

Description

The HGTG30N120D2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

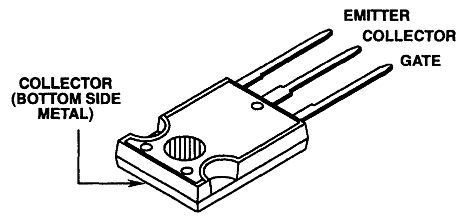
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG30N120D2	TO-247	G30N120D2

Formerly Developmental Type TA49010

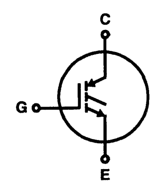
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



3

IGBTs

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTG30N120D2	UNITS
Collector-Emitter Voltage	BV_{CES}	1200	V
Collector-Gate Voltage, R_{GE} =1MΩ	V_{CGR}	1200	V
Collector Current Continuous at T_C = +25°C	I_{C25}	50	A
at V_{GE} =15V at T_C = +90°C	I_{C90}	30	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at T_J = +150°C	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at T_C = +25°C	P_D	208	W
Power Dissipation Total Derating T_C > +25°C		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at V_{GE} = 15V	t_{SC}	6	µS
at V_{GE} = 10V	t_{SC}	15	µS

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)}$ = 720V, T_C = +125°C, R_{GE} = 25Ω.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2834.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		1200	-	-	V
Zero Gate Voltage Collector Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	mA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	3.0	3.5	V
			$T_C = +125^oC$	-	3.2	3.5	V
		$I_C = I_{C90}$, $V_{GE} = 10V$	$T_C = +25^oC$	-	3.2	3.8	V
			$T_C = +125^oC$	-	3.4	3.8	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$V_{GE} = V_{CE}$, $I_C = 1mA$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	185	240	nC
			$V_{GE} = 20V$	-	240	315	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	760	990	ns
Current Fall Time	t_{FI}			-	580	750	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	8.4	-	mJ
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 10V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	610	790	ns
Current Fall Time	t_{FI}			-	580	750	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	8.4	-	mJ
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	0.5	0.6	°C/W

NOTE: 1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG20N100D2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

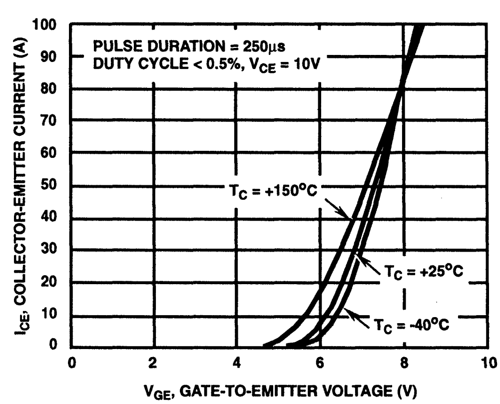


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

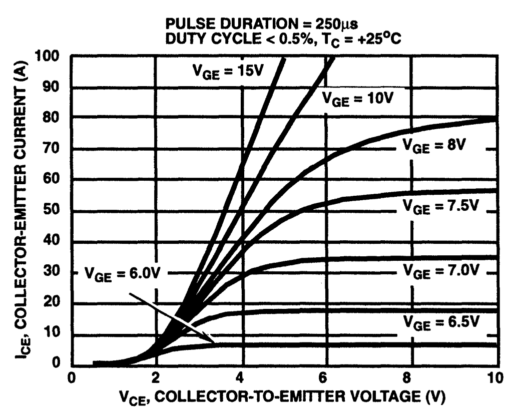


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

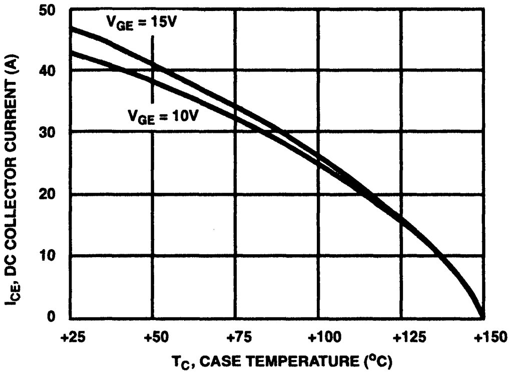


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

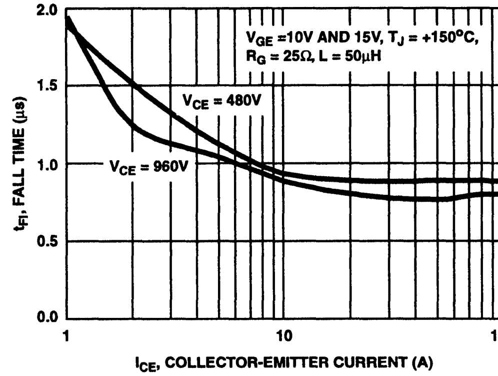


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

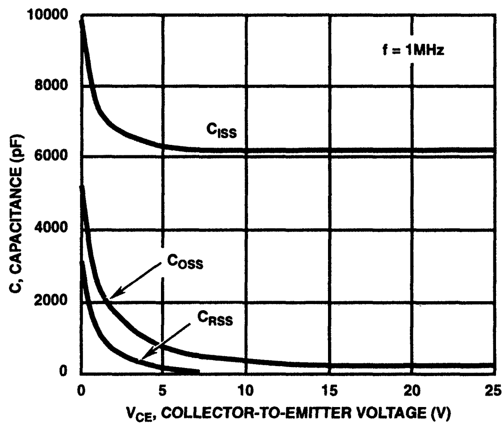


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

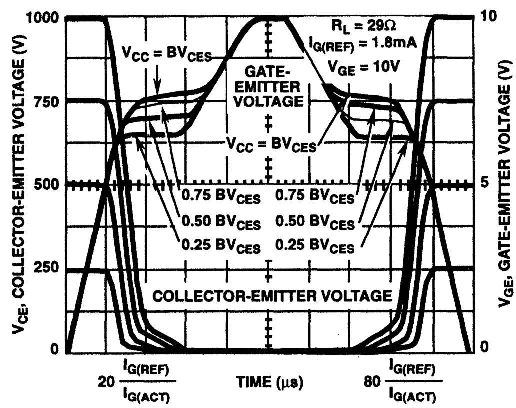


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

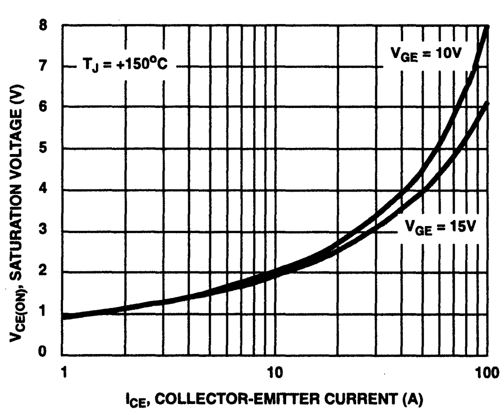


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

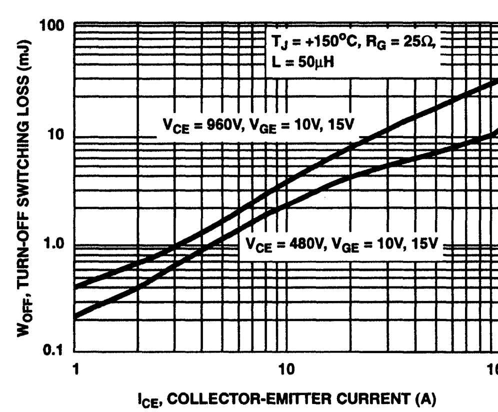


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

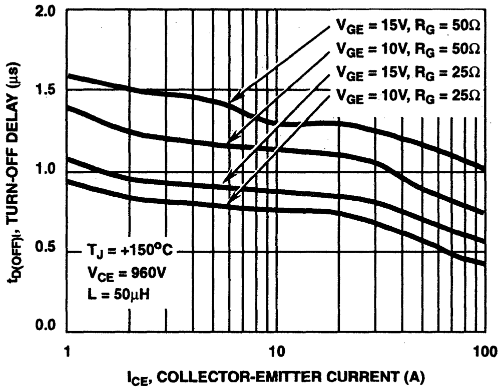
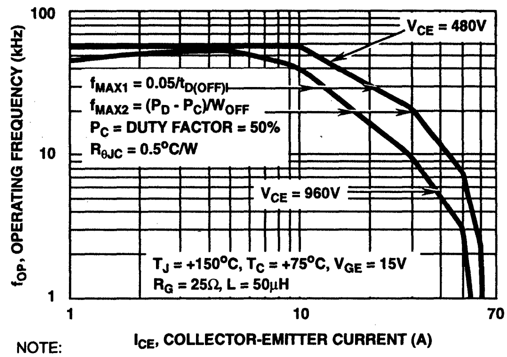


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

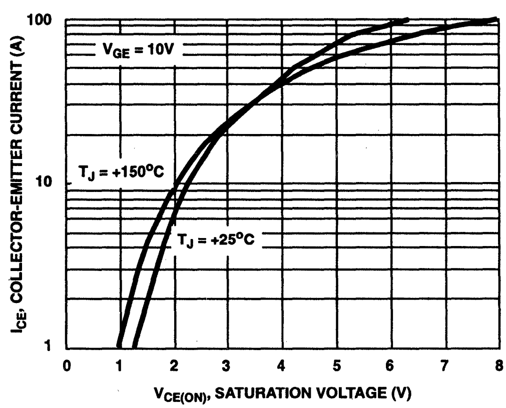


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

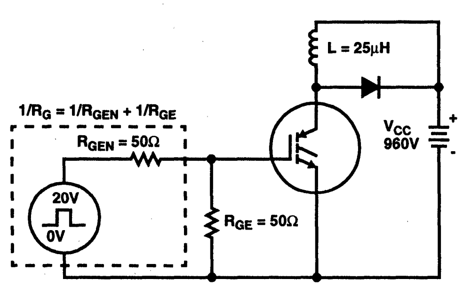


FIGURE 12. INDUCTIVE SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

HGTA32N60E2

April 1995

32A, 600V N-Channel IGBT

Features

- 32A, 600V
- Latch Free Operation
- Typical Fall Time 620ns
- High Input Impedance
- Low Conduction Loss

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

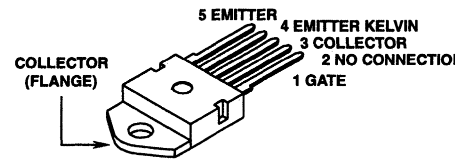
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTA32N60E2	TO-218	GA32N60E2

NOTE: When ordering, use the entire part number.

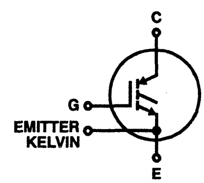
Package

JEDEC MO-093AA (5 LEAD TO-218)



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		HGTA32N60E2	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	V_{CGR}	600	V
Collector Current Continuous at $T_C = +25°C$	I_{C25}	50	A
at $V_{GE} = 15V$ at $T_C = +90°C$	I_{C90}	32	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Sage Operating Area $T_J = +150°C$	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25°C$	P_D	208	W
Power Dissipation Derating $T_C > +25°C$		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	3	µs
at $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junctions temperature.
2. $V_{CE(PEAK)} = 360V$, $T_C = +125°C$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 250μA, V_{GE} = 0V		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = BV_{CES}	T_C = +25°C	-	-	250	μA
		V_{CE} = 0.8 BV_{CES}	T_C = +125°C	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = I_{C90}, V_{GE} = 15V	T_C = +25°C	-	2.4	2.9	V
			T_C = +125°C	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_C = 1.0mA, V_{CE} = V_{GE}	T_C = +25°C	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}		-	6.5	-	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = I_{C90}, V_{CE} = 0.5 BV_{CES}	V_{GE} = 15V	-	200	260	nC
			V_{GE} = 20V	-	265	345	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	L = 500μH, I_C = I_{C90}, R_G = 25Ω, V_{GE} = 15V, T_J = +125°C, V_{CE} = 0.8 BV_{CES}		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	630	820	ns
Current Fall Time	t_{FI}			-	620	800	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	3.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	°C/W

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A) The HGTA32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

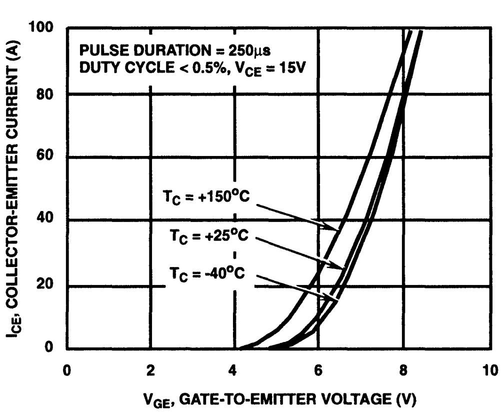


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

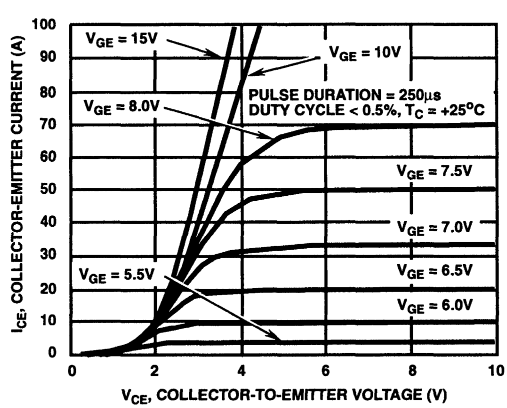


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

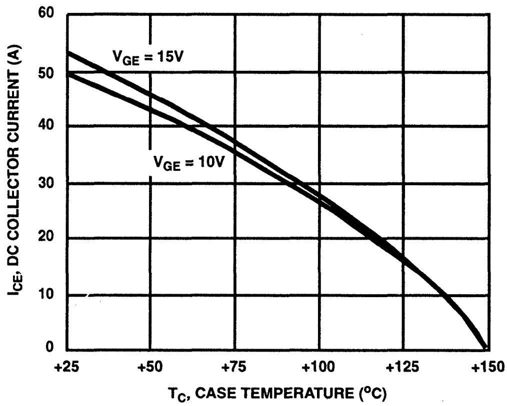


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT vs CASE TEMPERATURE

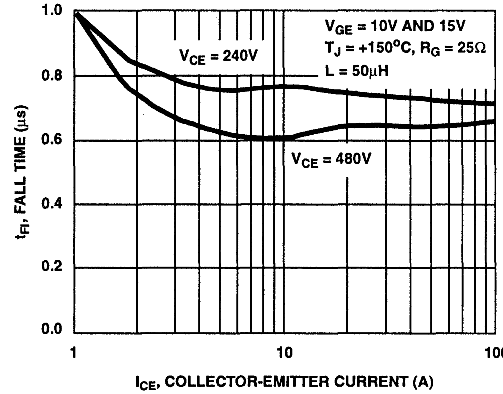


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

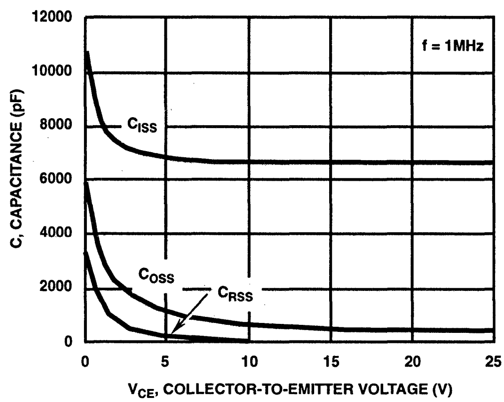


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

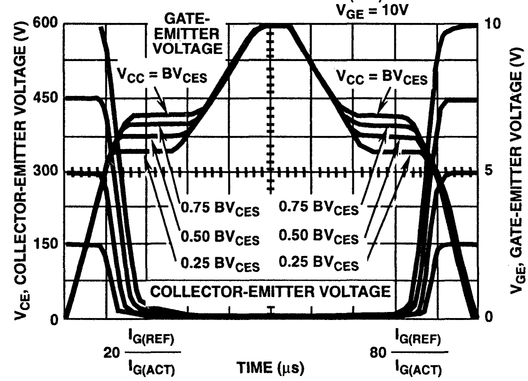


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

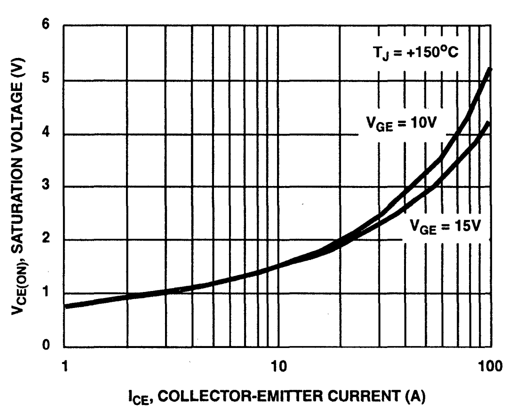


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

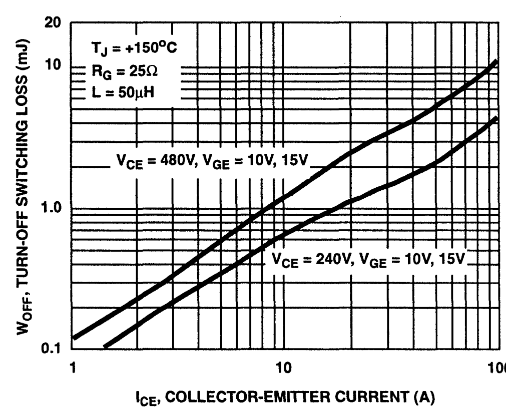


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

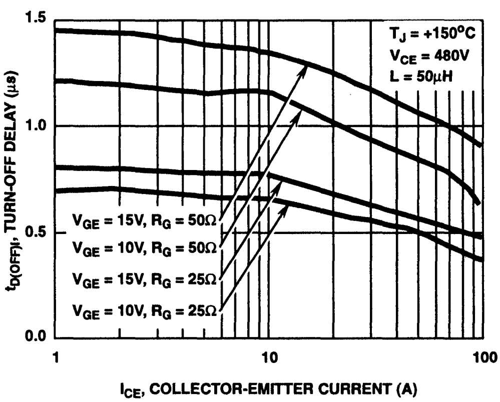
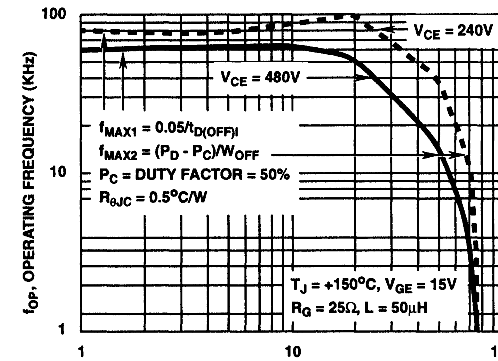


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{MAX1} \times W_{OFF}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

HGTG32N60E2

April 1995

32A, 600V N-Channel IGBT

Features

- 32A, 600V
- Latch Free Operation
- Typical Fall Time - 600ns
- High Input Impedance
- Low Conduction Loss

Description

The IGBT is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

IGBTs are ideal for many high voltage switching applications operating at frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

This device incorporates generation two design techniques which yield improved peak current capability and larger short circuit withstand capability than previous designs.

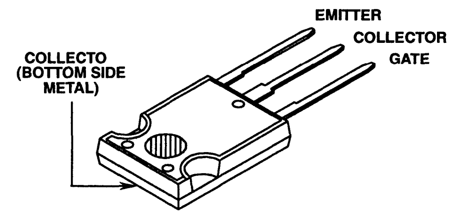
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HGTG32N60E2	TO-247	G32N60E2

NOTE: When ordering, use the entire part number.

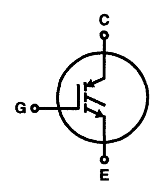
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTG32N60E2	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage $R_{GE} = 1M\Omega$	V_{CGR}	600	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	50	A
at $V_{GE} = 15V$, at $T_C = +90^oC$	I_{C90}	32	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = +150^oC$	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25^oC$	P_D	208	W
Power Dissipation Derating $T_C > +25^oC$		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	3	µs
at $V_{GE} = 10V$	t_{SC}	15	µs

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 360V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2828.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	250	μA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	2.4	2.9	V
			$T_C = +125^oC$	-	2.4	3.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	6.5	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	200	260	nC
			$V_{GE} = 20V$	-	265	345	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 500\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	630	820	ns
Current Fall Time	t_{FI}			-	620	800	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	3.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

NOTE:

1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG32N60E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-off Switching Loss. This test method produces the true total Turn-off Energy Loss.

Typical Performance Curves

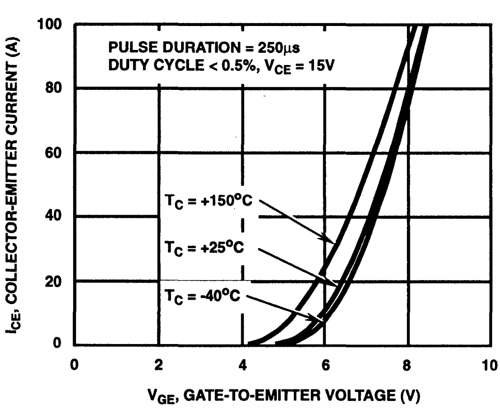


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

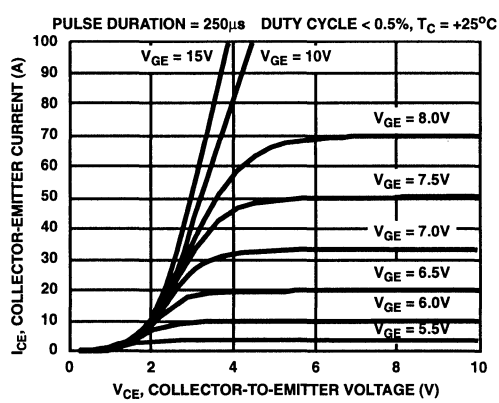


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

Typical Performance Curves (Continued)

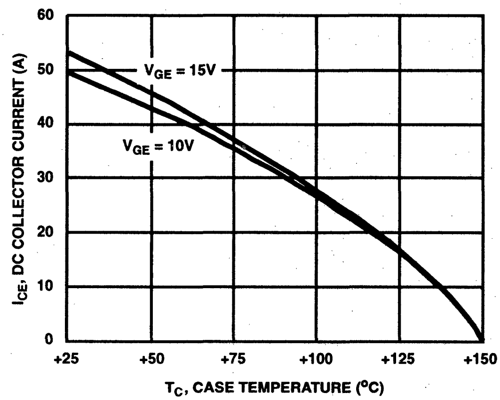


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT vs CASE TEMPERATURE

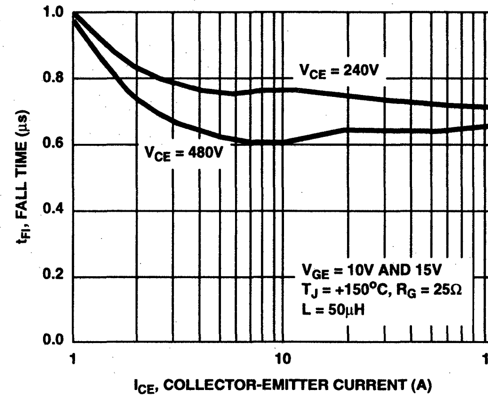


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

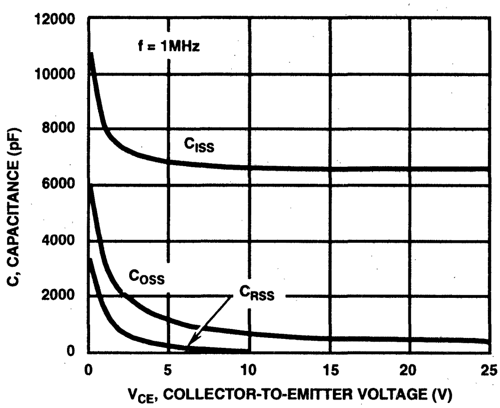


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

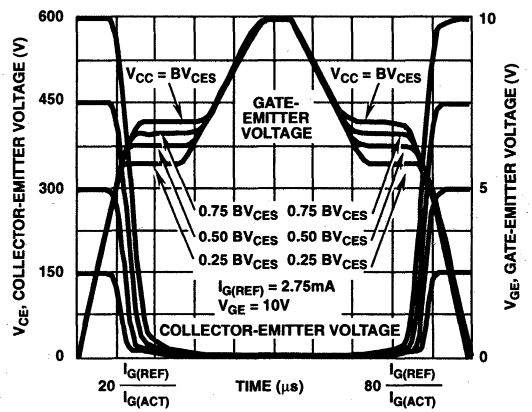


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260).

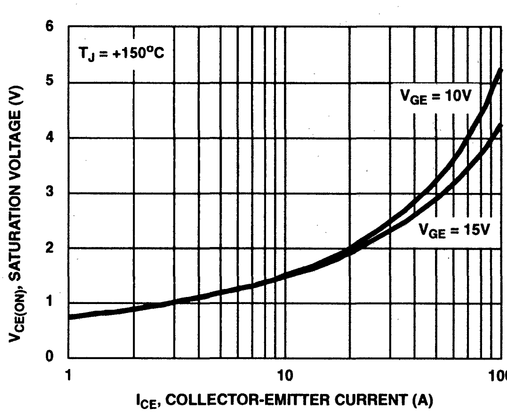


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

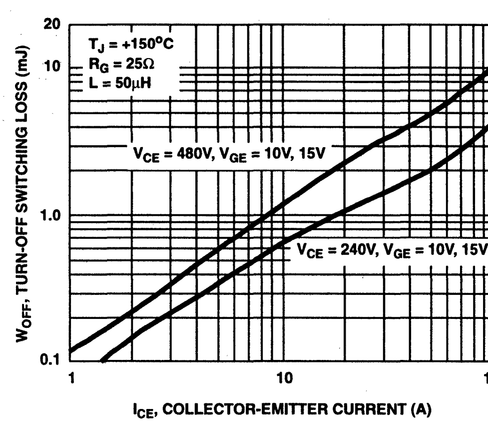


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

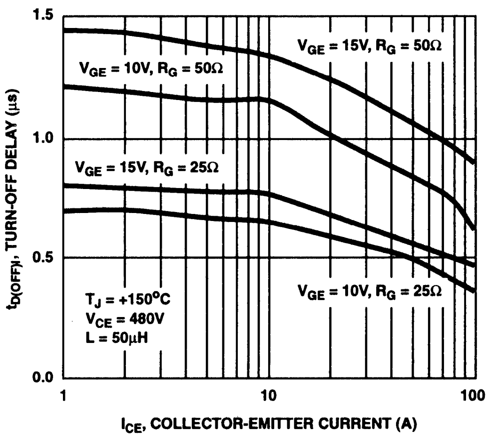


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT

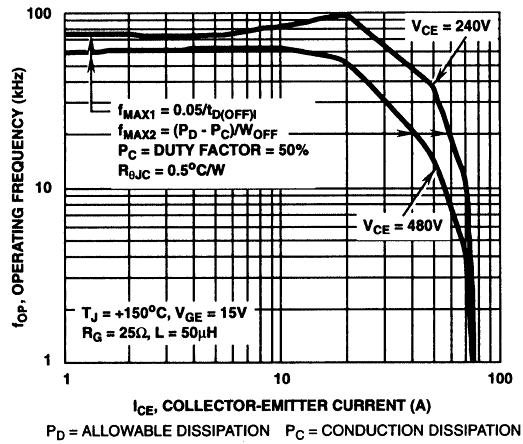


FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) so that the conduction losses (P_C) can be approximated by $P_C = (V_{CE} \times I_{CE})/2$. W_{OFF} is defined as the sum of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} - 0A).

The switching power loss (Figure 10) is defined as $f_{MAX1} \times W_{OFF}$. Turn on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

3

IGBTs

HARRIS SEMICONDUCTOR HGTG34N100E2

April 1995

34A, 1000V N-Channel IGBT

Features

- 34A, 1000V
- Latch Free Operation
- Typical Fall Time - 710ns
- High Input Impedance
- Low Conduction Loss

Description

The HGTG34N100E2 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBTs are ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

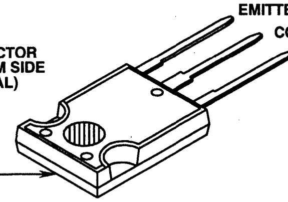
PART NUMBER	PACKAGE	BRAND
HGTG34N100E2	TO-247	G34N100E2

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA9895.

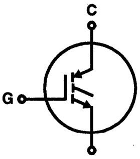
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTG34N100E2	UNITS
Collector-Emitter Voltage	BV_{CES}	1000	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	V_{CGR}	1000	V
Collector Current Continuous at $T_C = +25^oC$	I_{C25}	55	A
at $V_{GE} = 15V$, at $T_C = +90^oC$	I_{C90}	34	A
Collector Current Pulsed (Note 1)	I_{CM}	200	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_J = +150^oC$	SSOA	200A at 0.8 BV_{CES}	-
Power Dissipation Total at $T_C = +25^oC$	P_D	208	W
Power Dissipation Derating $T_C > +25^oC$		1.67	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	3	µs
at $V_{GE} = 10V$	t_{SC}	10	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PEAK)} = 600V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2827.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$		1000	-	-	V
Collector-Emitter Leakage Voltage	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	1.0	mA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +125^oC$	-	-	4.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = I_{C90}$, $V_{GE} = 15V$	$T_C = +25^oC$	-	2.8	3.2	V
			$T_C = +125^oC$	-	2.8	3.1	V
		$I_C = I_{C90}$, $V_{GE} = 10V$	$T_C = +25^oC$	-	2.9	3.3	V
			$T_C = +125^oC$	-	3.0	3.4	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1mA$, $V_{CE} = V_{GE}$	$T_C = +25^oC$	3.0	4.5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±500	nA
Gate-Emitter Plateau Voltage	V_{GEP}	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$		-	7.3	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = I_{C90}$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	185	240	nC
			$V_{GE} = 20V$	-	240	315	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 15V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	610	795	ns
Current Fall Time	t_{FI}			-	710	925	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	7.1	-	mJ
Current Turn-On Delay Time	$t_{D(ON)I}$	$L = 50\mu H$, $I_C = I_{C90}$, $R_G = 25\Omega$, $V_{GE} = 10V$, $T_J = +125^oC$, $V_{CE} = 0.8\ BV_{CES}$		-	100	-	ns
Current Rise Time	t_{RI}			-	150	-	ns
Current Turn-Off	$t_{D(OFF)I}$			-	460	600	ns
Current Fall Time	t_{FI}			-	670	870	ns
Turn-Off Energy (Note 1)	W_{OFF}			-	6.5	-	mJ
Thermal Resistance	$R_{\theta JC}$			-	0.5	0.6	$^oC/W$

NOTE: 1. Turn-off Energy Loss (W_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$) The HGTG34N100E2 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves

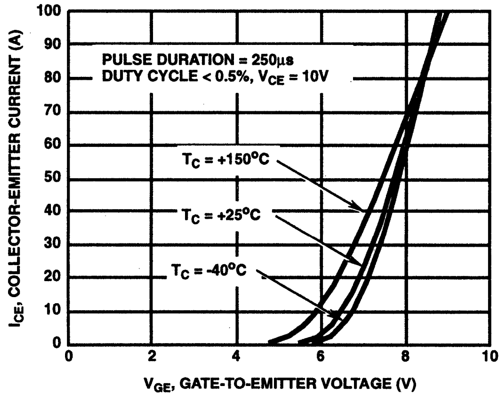


FIGURE 1. TRANSFER CHARACTERISTICS (TYPICAL)

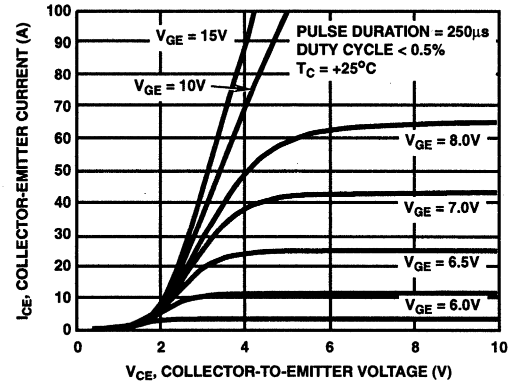


FIGURE 2. SATURATION CHARACTERISTICS (TYPICAL)

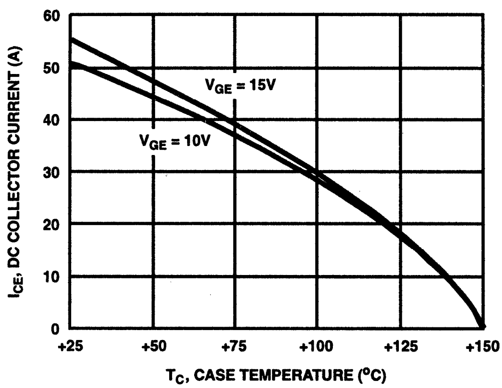


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

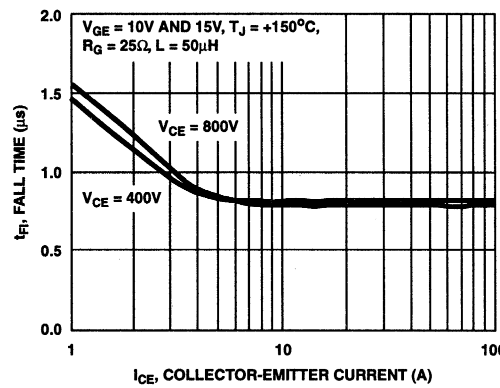


FIGURE 4. FALL TIME vs COLLECTOR-EMITTER CURRENT

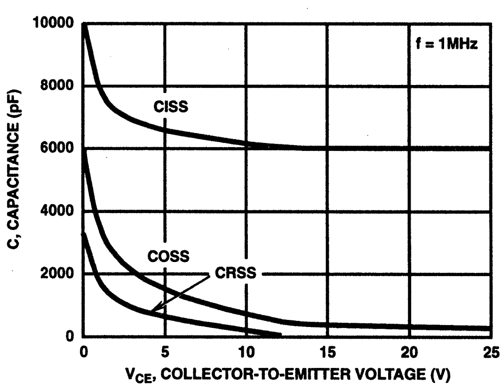


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

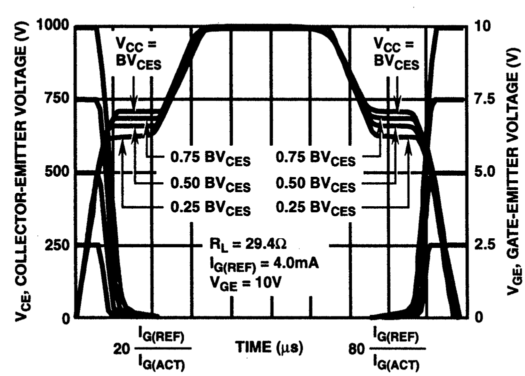


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT (REFER TO APPLICATION NOTES AN7254 AND AN7260)

Typical Performance Curves (Continued)

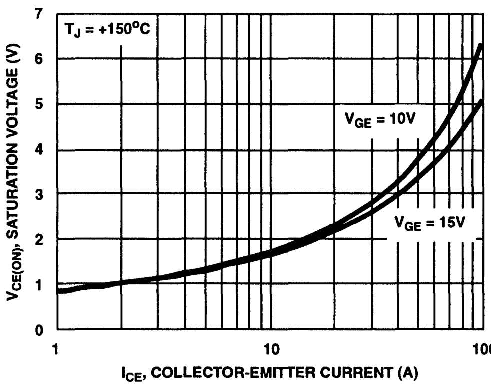


FIGURE 7. SATURATION VOLTAGE vs COLLECTOR-EMITTER CURRENT

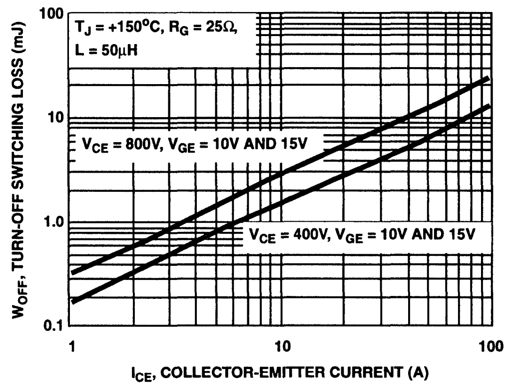


FIGURE 8. TURN-OFF SWITCHING LOSS vs COLLECTOR-EMITTER CURRENT

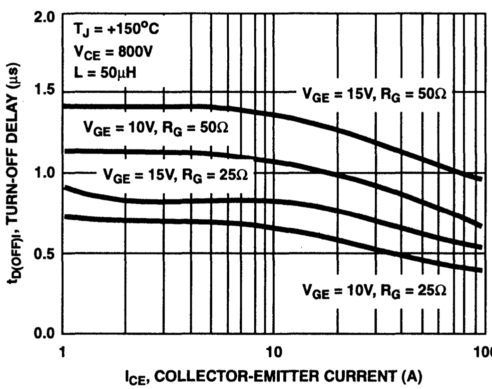
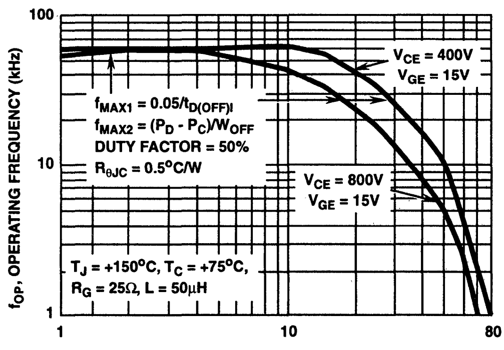


FIGURE 9. TURN-OFF DELAY vs COLLECTOR-EMITTER CURRENT



NOTE:
P_D = ALLOWABLE DISSIPATION P_C = CONDUCTION DISSIPATION

FIGURE 10. OPERATING FREQUENCY vs COLLECTOR-EMITTER CURRENT AND VOLTAGE

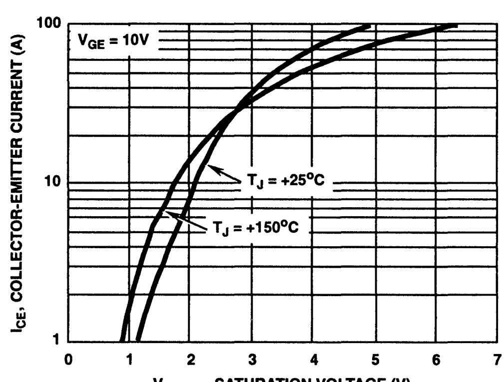


FIGURE 11. COLLECTOR-EMITTER SATURATION VOLTAGE

Test Circuit

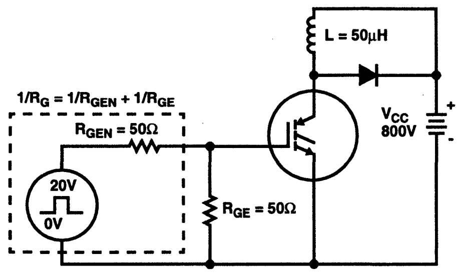


FIGURE 12. INDUCTION SWITCHING TEST CIRCUIT

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 7, 8 and 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/W_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 10) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \bullet I_{CE})/2$. W_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet W_{OFF}$. Turn-on switching losses are not included because they can be greatly influenced by external circuit conditions and components.

HARRIS SEMICONDUCTOR

HGTD8P50G1, HGTD8P50G1S

May 1996

8A, 500V P-Channel IGBTs

Features

- 8A, 500V
- 3.7V $V_{CE(SAT)}$
- Typical Fall Time - 1800ns
- High Input Impedance
- T_J = +150°C

Description

The HGTD8P50G1 and the HGTD8P50G1S are P-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drives. This P- channel IGBT can be paired with N-Channel IGBTs to form a complementary power switch and it is ideal for half bridge circuit configurations. These types can be operated directly from low power integrated circuits.

PACKAGING AVAILABILITY

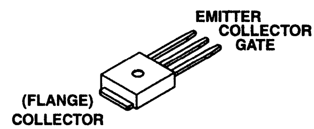
PART NUMBER	PACKAGE	BRAND
HGTD8P50G1	TO-251AA	G8P50G
HGTD8P50G1S	TO-252AA	G8P50G

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., HGTD8P50G1S9A.

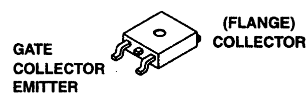
The development type number for these devices is TA49015.

Package

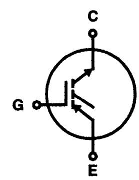
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		HGTD8P50G1/G1S	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	-500	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	10	V
Collector Current Continuous			
At T_C = +25°C	I_{C25}	-12	A
At T_C = +90°C	I_{C90}	-8	A
Collector Current Pulsed (Note 1)	I_{CM}	-18	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching SOA at T_C = +25°C, V_{CL} = -350V	SSOA		
No Snubber, Figure 17 - Circuit 1		-3	A
With 0.1μF Capacitor, Figure 17 - Circuit 2		-18	A
Power Dissipation Total at T_C = +25°C	P_D	66	W
Power Dissipation Derating T_C > +25°C		0.53	W/°C
Operating and Storage Junction Temperature	T_J, T_{STG}	-40 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5s)	T_L	+260	°C

NOTE:

1. T_J = 25°C, V_{CL} = 350V, R_{GE} = 25Ω, Figure 17 - Circuit 2 (C_1 = 0.1μF)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3649.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_{CE} = -250\mu A$ $V_{CL} = -600V$	$V_{GE} = 0V$	-500	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	$I_{EC} = 1mA$	$V_{GE} = 0V$	10	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	-250	µA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +150^oC$	-	-	-1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{CE} = -3.0A$ $V_{GE} = -15V$	$T_C = +25^oC$	-	-2.5	-2.9	V
			$T_C = +150^oC$	-	-2.3	-2.8	V
		$I_{CE} = I_{C90}$ $V_{GE} = -15V$	$T_C = +25^oC$	-	-3.0	-3.7	V
			$T_C = +150^oC$	-	-3.3	-4.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_{CE} = -1.0mA$	$V_{CE} = V_{GE}$	-4.5	-6.0	-7.5	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±100	nA
Gate-Emitter Plateau Voltage	$V_{GE(PL)}$	$I_C = 3A$	$V_{CE} = 0.5\ BV_{CES}$	-	-7.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_C = 3A$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = -15V$	-	16	25	nC
			$V_{GE} = -20V$	-	22	30	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$R_L = 113\Omega$	$I_{CE} = -3A$, $V_{GE} = -15V$ $V_{CE} = -350V$ $R_G = 25\Omega$ $T_J = +150^oC$ Fig. 17, Circuit 1	-	45	-	ns
Current Rise Time	t_{RI}			-	85	-	ns
Current Turn-off Delay Time	$t_{D(OFF)I}$	$L = 100\mu H$		-	480	680	ns
Current Fall Time	t_{FI}			-	1800	2500	ns
Turn-Off Energy (Note 1)	E_{OFF}			-	0.8	-	mJ
Current Turn-Off Delay Time	$t_{D(OFF)I}$	$L = 100\mu H$	$I_{CE} = -8A$, $V_{GE} = -15V$ $V_{CE} = -350V$ $R_G = 25\Omega$ $T_J = +150^oC$ Fig. 17, Circuit 2 $C_1 = .022\mu F$	-	100	200	ns
Current Fall Time	t_{FI}			-	3500	4000	ns
Turn-Off Energy (Note 1)	E_{OFF}			-	1.3	-	mJ
Latching Current	I_L	$L = 100\mu H$	$V_{GE} = -15V$ $R_G = 25\Omega$ $T_J = +25^oC$ $V_{CE} = -350V$ Fig. 17, Circuit 1	-3	-	-	A
Thermal Resistance	$R_{\theta JC}$			-	1.75	1.90	°C/W

NOTE:

1. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTD8P50G1 and HGTD8P50G1S were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

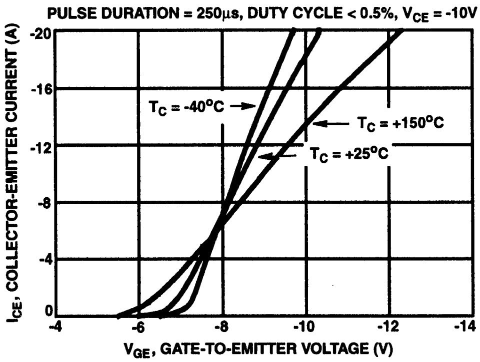


FIGURE 1. TRANSFER CHARACTERISTICS

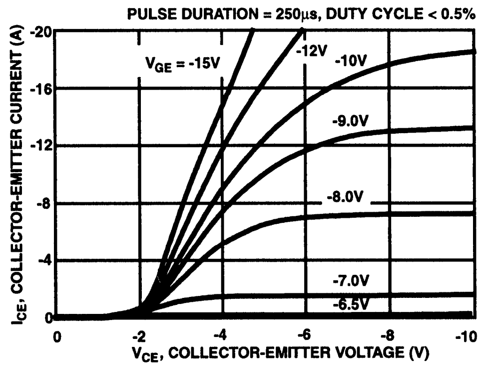


FIGURE 2. SATURATION CHARACTERISTICS

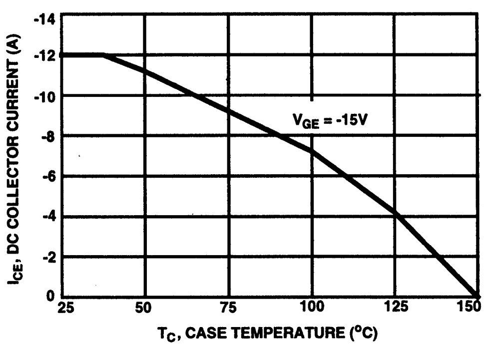


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

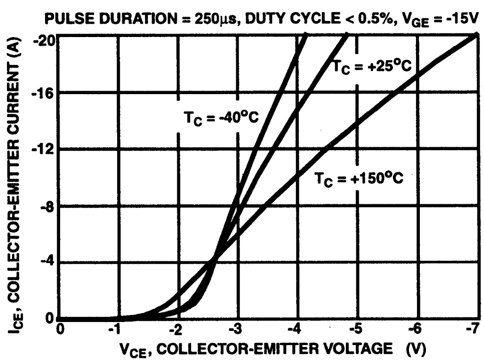


FIGURE 4. COLLECTOR-EMITTER SATURATION VOLTAGE

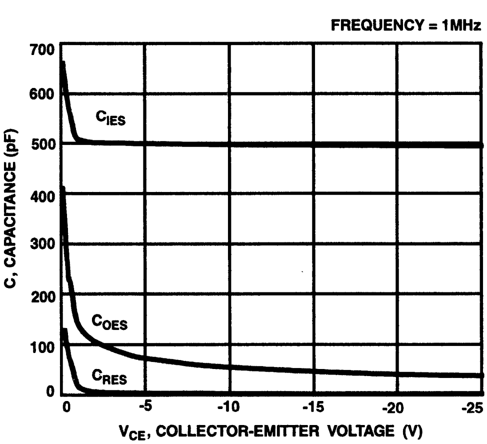


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

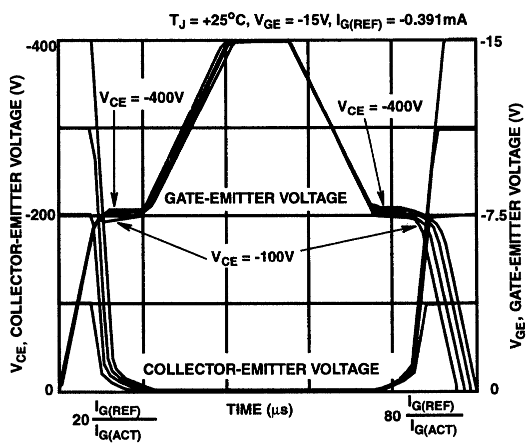


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

Typical Performance Curves (Continued)

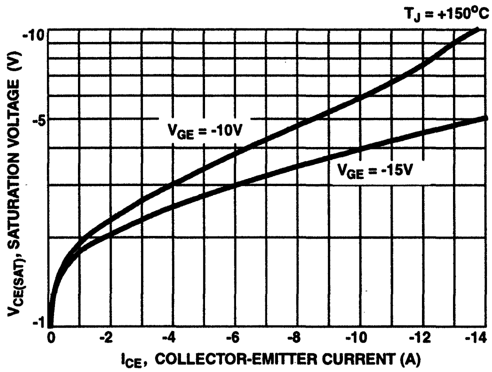


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

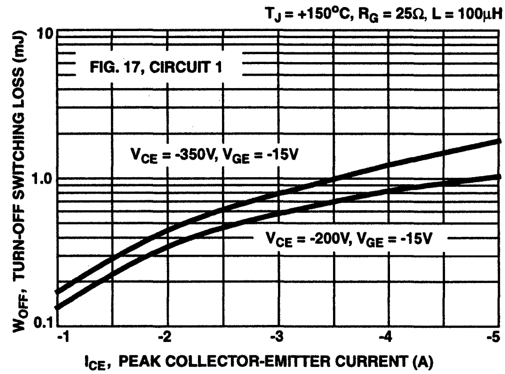


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

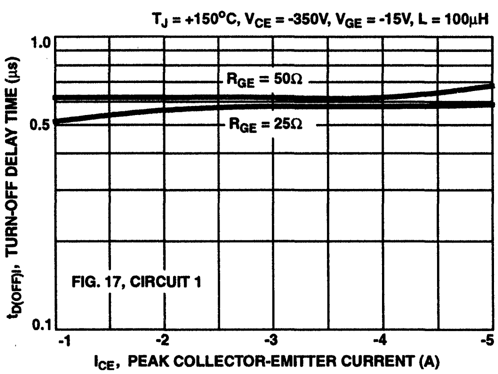


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

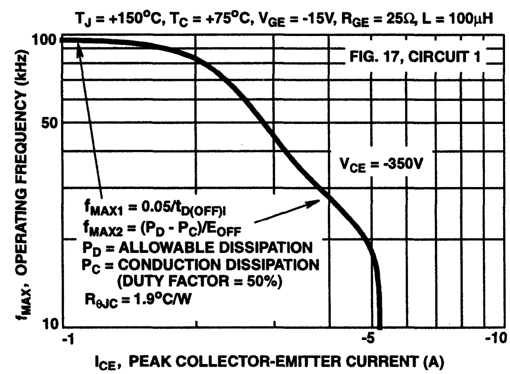


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

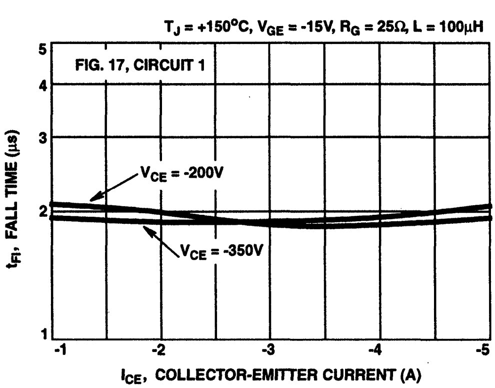


FIGURE 11. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

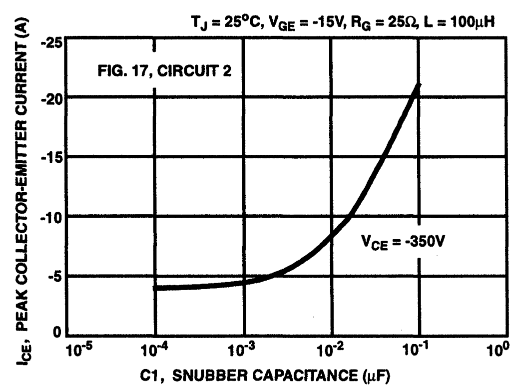


FIGURE 12. LATCHING CURRENT AS A FUNCTION OF SNUBBER CAPACITANCE

Typical Performance Curves (Continued)

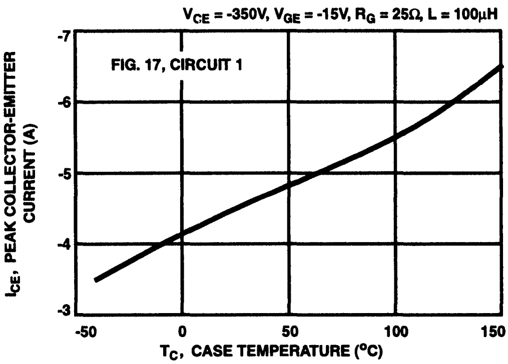


FIGURE 13. LATCHING CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

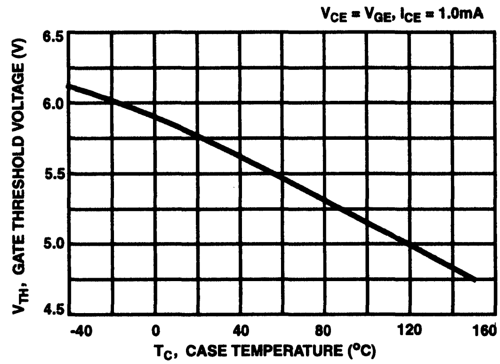


FIGURE 14. GATE THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

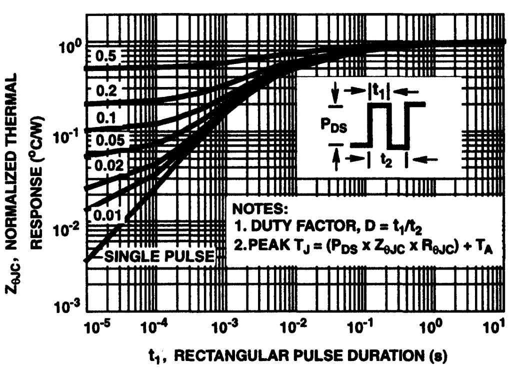


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

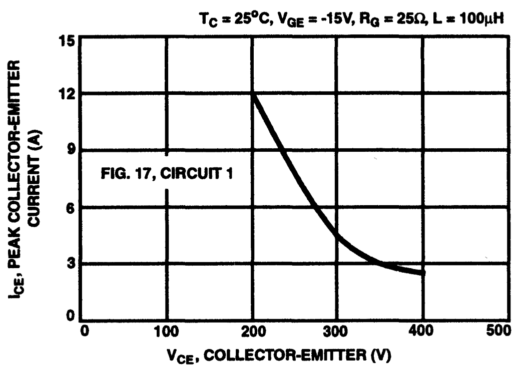


FIGURE 16. LATCHING CURRENT AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

Test Circuits

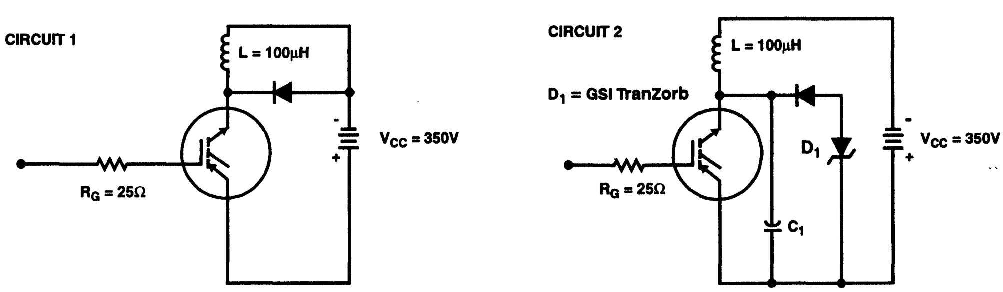


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUITS

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figure 7, Figure 8 and Figure 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device Turn-Off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition. f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/E_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed Pd. A 50% duty factor was used (Figure 10) and the conduction losses (Pc) are approximated by $Pc = (V_{CE} \bullet I_{CE})/2$. E_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet E_{OFF}$. Turn-On switching losses are not included because they can be greatly influenced by external circuit conditions and components.

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "†ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in Turn-On of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

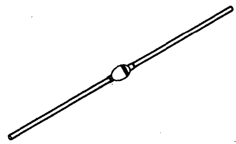
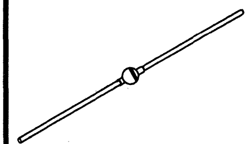
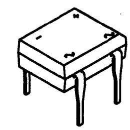
MCT/IGBT/DIODES 4

GENERAL PURPOSE DIODES

PAGE

Selection Guide

HARRIS STANDARD AND FAST RECOVERY RECTIFIER PRODUCT LINE

	 DO-204				 AL-3		 BR-4
	$I_{F(AVG)}$				$I_{F(AVG)}$		$I_{F(AVG)}$
V_{RRM}	**1A**	**1A**	**1A**	**1A**	**3A**	**3A**	**1A**
50V	A14F		GER4001	A114F	A15F	A115F	DB1F
100V	A14A		GER4002	A114A	A15A	A115A	DB1A
150V							
200V	1N5059	1N4245	GER4003	A114B	1N5624	A115B	DB1B
300V	A14C			A114C		A115C	
400V	1N5060	1N4246	GER4004	A114D	1N5625	A115D	DB1D
500V	A14E			A114E		A115E	
600V	1N5061	1N4247	GER4005	A114M	1N5626	A115M	DB1M
800V	1N5062	1N4248	GER4006		1N5627		DB1N
1000V	A14P	1N4249	GER4007				DB1P
t_{RR}(µs)	5/6	5		0.2	5	0.15/0.25	

HRP2540

April 1995

Power Rectifier/Power Surge Suppressor

Features

- Low Forward Voltage Drop (1.1V Max at 100A)
- High Reverse Energy Capability
- Controlled Maximum Avalanche Voltage (40V Max at 40A)

Applications

- Alternator Rectification
- Accessory Load Dump Protector
- High Current Forward Voltage Clamp

Description

The HRP2540 (TA9673) is a high forward current, high reverse energy controlled avalanche power rectifier. It uses an ion-implanted planar epitaxial construction. This device was designed for use as the output rectifier in the three phase six diode bridge assembly of an automotive alternator system. It provides "Load Dump" suppression by virtue of its precisely controlled reverse avalanche breakdown voltage. When used singly it can also serve as a transient suppressor for an automotive accessory. This device can provide forward voltage clamping and reverse voltage bypassing. This will protect the accessory from L-C inductive spikes and/or field decay transients.

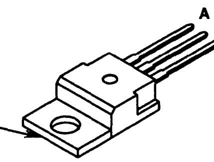
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
HRP2540	TO-220AB	HRP2540

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol

Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HRP2540	UNITSVm
DC Peak Repetitive Reverse Voltage	V_{RRM}	23	V
RMS Forward Current ($T_C = 125^oC$)	I_{RMS}	25	A
Average Rectified Forward Current (Single Phase Resistive Load $T_C = 125^oC$)	I_O	22	A
Non-Repetitive Peak Forward Surge Current (Surge Applied at Rated Load Conditions, Halfwave, Single Phase 60Hz)	I_{FSM}	600	A
Power Dissipation	P_T		
At $T_C = 25^oC$		100	W
Derated above 25^oC		0.8	$W/^oC$
Operating and Storage Junction Temperature Range	T_{STG}, T_J	-65 to 150	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Forward Voltage Drop (Note 1)	V_F	$I_F = 100A$	-	1.1	V
Reverse Current	I_R	$V_R = 20V$	-	1	mA
Reverse Current $T_C = 100^oC$	I_R	$V_R = 20V$	-	50	mA
Breakdown Voltage	B_V	$I_R = 100mA$	24	32	V
Breakdown Voltage (Note 2) $T_C = 85^oC$	BV_M	$I_R = 40A$	-	40	V
Thermal Resistance	-	$R_{\theta JC}$	-	1.25	$^oC/W$

NOTES:

1. Pulse Test: Pulse width <300μs duty cycle <2.0%.
2. Pulse Test: Pulse width <10ms, duty cycle <2.0%.

Typical Performance Curves

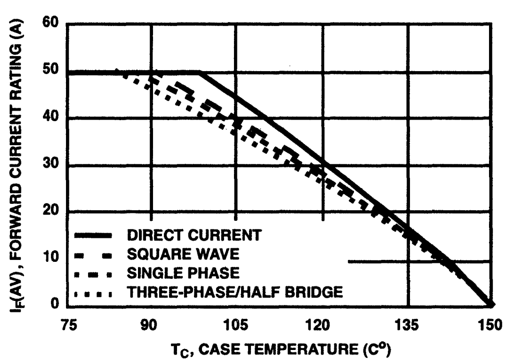


FIGURE 1. MAXIMUM FORWARD CURRENT vs TEMPERATURE DERATING CURVE

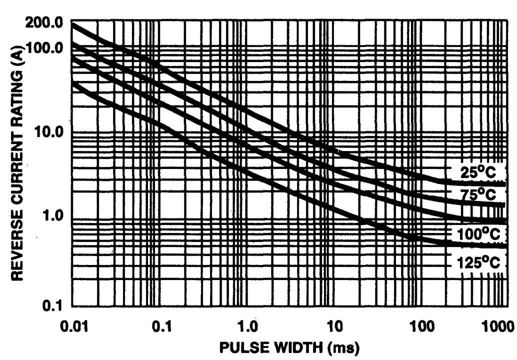


FIGURE 2. MAXIMUM REVERSE CURRENT vs PULSE WIDTH

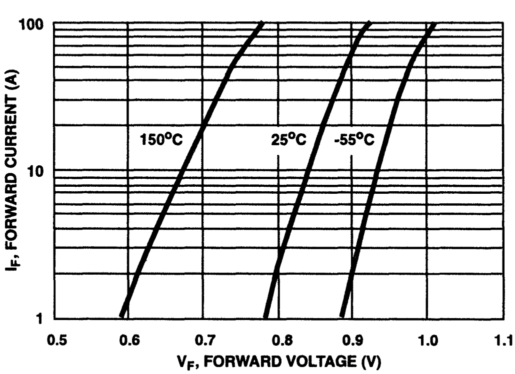


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE

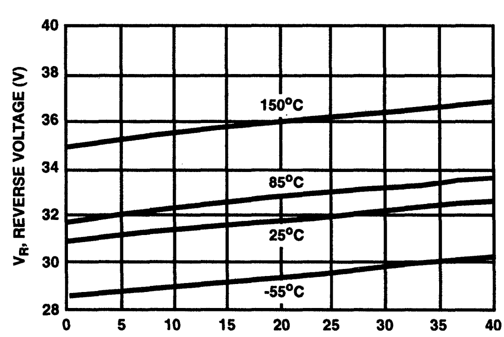


FIGURE 4. TYPICAL REVERSE VOLTAGE vs REVERSE CURRENT

Typical Performance Curves (Continued)

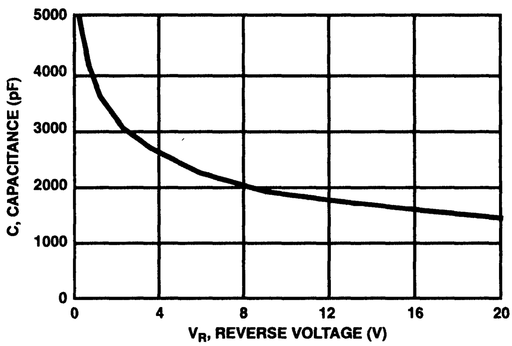


FIGURE 5. TYPICAL CAPACITANCE vs REVERSE VOLTAGE

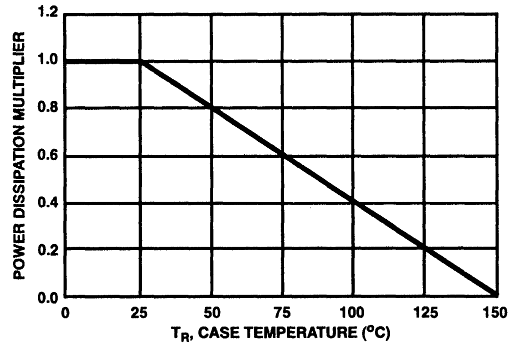


FIGURE 6. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

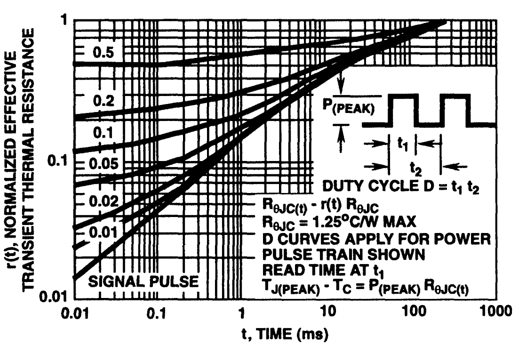
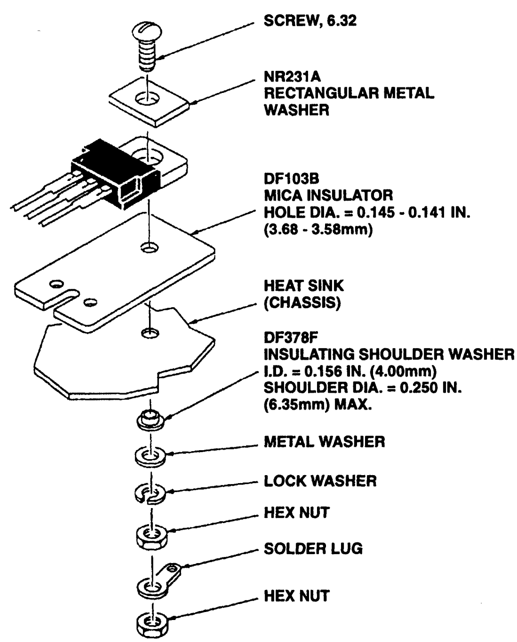


FIGURE 7. TRANSIENT THERMAL RESISTANCE

Exploded View

SUGGESTED MOUNTING HARDWARE FOR JEDEC TO-220AB



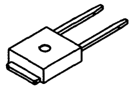
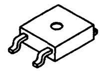
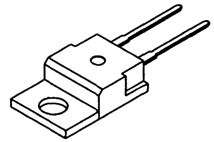
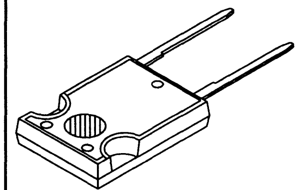
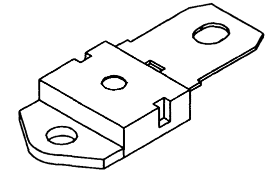
NOTE: Maximum torque applied to mounting flange is 8 in. lb. (0.09kgf m).

MCT/IGBT/DIODES 5

ULTRAFAST SINGLE DIODES

Ultrafast Single Diodes (Continued)

HARRIS ULTRA-FAST RECOVERY RECTIFIER PRODUCT LINE

	 TO-251		 TO-252		 TO-220AC			 2 LEAD TO-247			 SINGLE LEAD TO-218			
	$I_{F(AVG)}$		$I_{F(AVG)}$		$I_{F(AVG)}$			$I_{F(AVG)}$			$I_{F(AVG)}$			
V_{RRM}	4A	6A	4A	6A	8A	15A	30A	30A	50A	75A/80A	50A	75A/80A	100A	150A
100V	RURD410 1.0V 35ns	RURD610 1.0V 35ns	RURD410S 1.0V 35ns	RURD610S 1.0V 35ns	MUR810 RURP810 0.975V 35ns†	MUR1510 RURP1510 1.05V 35ns	RURP3010 1.0V 50ns	RURG3010 1.0V 50ns						
150V	RURD415 1.0V 35ns	RURD615 1.0V 35ns	RURD415S 1.0V 35ns	RURD615S 1.0V 35ns	MUR815 RURP815 0.975V 35ns†	MUR1515 RURP1515 1.05V 35ns	RURP3015 1.0V 50ns	RURG3015 1.0V 50ns						
200V	RURD420 1.0V 35ns	RURD620 1.0V 35ns	RURD420S 1.0V 35ns	RURD620S 1.0V 35ns	MUR820 RURP820 1.0V 35ns†	MUR1520 RURP1520 1.05V 35ns	RURP3020 1.0V 50ns	RURG3020 1.0V 50ns						
400V	RURD440 1.5V 60ns	RURD640 1.5V 60ns	RURD440S 1.5V 60ns	RURD640S 1.5V 60ns	MUR840 RURP840 1.3V 60ns†	MUR1540 RURP1540 1.25V 60ns	RURP3040 1.5V 60ns	RURG3040 1.5V 60ns	RURG5040 1.6V 75ns	RURG8040 1.6V 85ns	RURU5040 1.6V 75ns	RURU8040 1.6V 85ns	RURU10040 1.6V 100ns	RURU15040 1.6V 100ns
500V	RURD450 1.5V 60ns	RURD650 1.5V 60ns	RURD450S 1.5V 60ns	RURD650S 1.5V 60ns	MUR850 RURP850 1.5V 60ns†	MUR1550 RURP1550 1.5V 60ns	RURP3050 1.5V 60ns	RURG3050 1.5V 60ns	RURG5050 1.6V 75ns	RURG8050 1.6V 85ns	RURU5050 1.6V 75ns	RURU8050 1.6V 85ns	RURU10050 1.6V 100ns	RURU15050 1.6V 100ns
600V	RURD460 1.5V 60ns	RURD660 1.5V 60ns	RURD460S 1.5V 60ns	RURD660S 1.5V 60ns	MUR860 RURP860 1.5V 60ns†	MUR1560 RURP1560 1.5V 60ns	RURP3060 1.5V 60ns	RURG3060 1.5V 60ns	RURG5060 1.6V 75ns	RURG8060 1.6V 85ns	RURU5060 1.6V 75ns	RURU8060 1.6V 85ns	RURU10060 1.6V 100ns	RURU15060 1.6V 100ns
700V					MUR870E RURP870 1.8V 110ns	RURP1570 1.8V 125ns	RURP3070 1.8V 150ns	RURG3070 1.8V 150ns	RURG5070 1.9V 200ns	RURG8070 1.9V 200ns	RURU5070 1.9V 200ns	RURU8070 1.9V 200ns	*RURU10070*	RURU15070 1.9V 200ns
800V					MUR880E RURP880 1.8V 110ns	RURP1580 1.8V 125ns	RURP3080 1.8V 150ns	RURG3080 1.8V 150ns	RURG5080 1.9V 200ns	RURG8080 1.9V 200ns	RURU5080 1.9V 200ns	RURU8080 1.9V 200ns	*RURU10080*	RURU15080 1.9V 200ns
900V					MUR890E RURP890 1.8V 110ns	RURP1590 1.8V 125ns	RURP3090 1.8V 150ns	RURG3090 1.8V 150ns	RURG5090 1.9V 200ns	RURG8090 1.9V 200ns	RURU5090 1.9V 200ns	RURU8090 1.9V 200ns	*RURU10090*	RURU15090 1.9V 200ns
1000V					MUR8100E RURP8100 1.8V 110ns	RURP15100 1.8V 125ns	RURP30100 1.8V 150ns	RURG30100 1.8V 150ns	RURG50100 1.9V 200ns	RURG80100 1.9V 200ns	RURU50100 1.9V 200ns	RURU80100 1.9V 200ns	*RURU100100*	RURU150100 1.9V 200ns
1200V	RURD4120 2.1V 90ns	RURD6120 2.1V 90ns	RURD4120S 2.1V 90ns	RURD6120S 2.1V 90ns	RURP8120 2.1V 110ns	RURP15120 2.1V 130ns	RURP30120 2.1V 150ns	RURG30120 2.1V 150ns	RURG50120 2.1 200ns	RURG75120 2.1V 200ns	RURU50120 2.1V 200ns	RURU75120 2.1V 200ns	RURU100120 2.1V 200ns	*RURU150120*

ITALICS = Future Product Offerings; V_F at $I_{F(AVG)}$, $T_J = 25^oC$; T_{RR} at $I_{F(AVG)}$, $dI_F/dt = 100A/\mu sec$ $T_J = 25^oC$; † T_{RR} at $I_F = 1A$.

MUR810, MUR815, MUR820, RURP810, RURP815, RURP820

June 1995

8A, 100V - 200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <25ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

MUR810, MUR815, MUR820, RURP810, RURP815 and RURP820 are ultrafast diodes with soft recovery characteristics (t_{RR} < 25ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGE AVAILABILITY

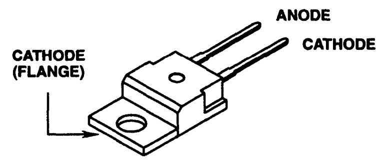
PART NUMBER	PACKAGE	BRAND
MUR810	TO-220AC	MUR810
MUR815	TO-220AC	MUR815
MUR820	TO-220AC	MUR820
RURP810	TO-220AC	RURP810
RURP815	TO-220AC	RURP815
RURP820	TO-220AC	RURP820

NOTE: When ordering, use the entire part number.

Formerly developmental type TA09223.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MUR810 RURP810	MUR815 RURP815	MUR820 RURP820	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	100	150	200	V
Working Peak Reverse Voltage	V_{RWM}	100	150	200	V
DC Blocking Voltage	V_R	100	150	200	V
Average Rectified Forward Current (T_C = +157°C)	$I_{F(AV)}$	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	A
Maximum Power Dissipation	P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MUR810, RURP810			MUR815, RURP815			MUR820, RURP820			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 8A, T_C = +25^oC$	-	-	0.975	-	-	0.975	-	-	0.975	V
	$I_F = 8A, T_C = +150^oC$	-	-	0.895	-	-	0.895	-	-	0.895	V
I_R	$V_R = 100V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	μA
	$V_R = 150V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	μA
	$V_R = 200V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	μA
I_R	$V_R = 100V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 150V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 200V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	μA
t_{RR}	$I_F = 1A, dI_F/dt = 200A/\mu s$	-	-	25	-	-	25	-	-	25	ns
	$I_F = 8A, dI_F/dt = 200A/\mu s$	-	-	30	-	-	30	-	-	30	ns
t_A	$I_F = 8A, dI_F/dt = 200A/\mu s$	-	13	-	-	13	-	-	13	-	ns
t_B	$I_F = 8A, dI_F/dt = 200A/\mu s$	-	5	-	-	5	-	-	5	-	ns
Q_{RR}	$I_F = 8A, dI_F/dt = 200A/\mu s$	-	25	-	-	25	-	-	25	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	60	-	-	60	-	-	60	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current .

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled Avalanche Energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

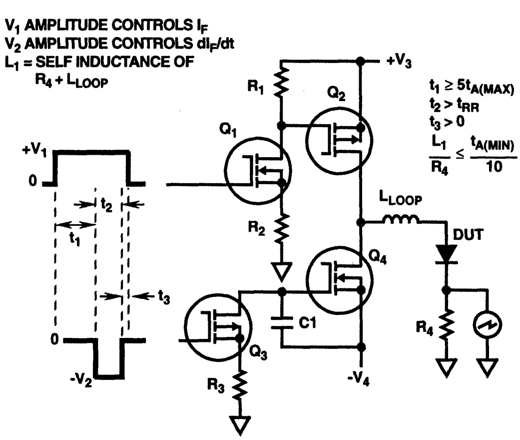


FIGURE 1. t_{RR} TEST CIRCUIT

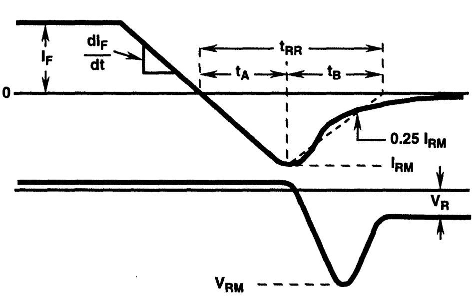


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

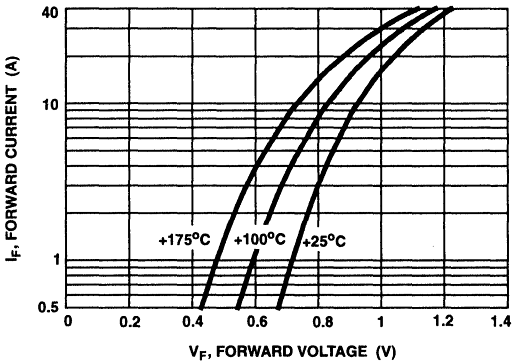


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

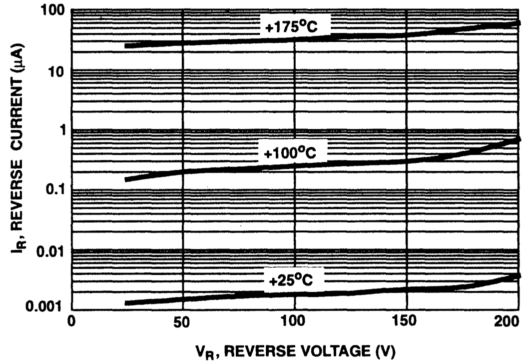


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

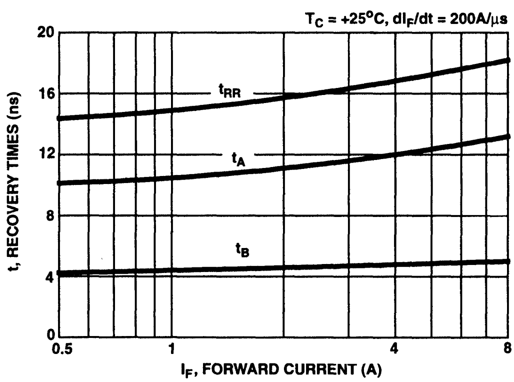


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

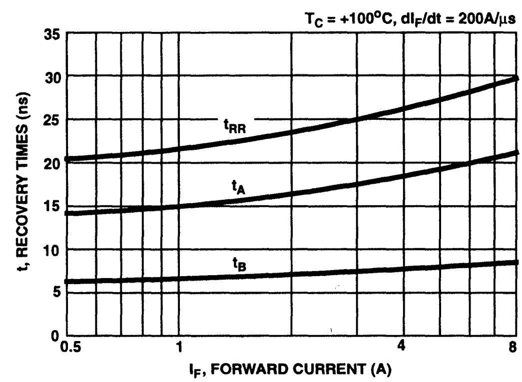


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

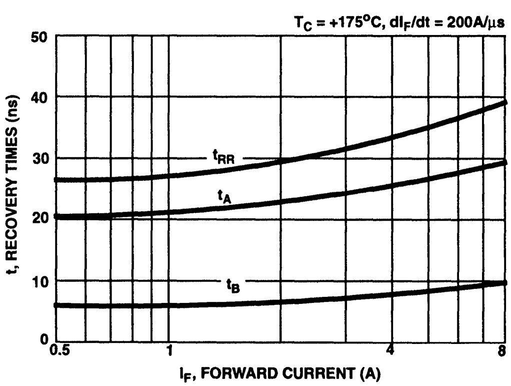


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

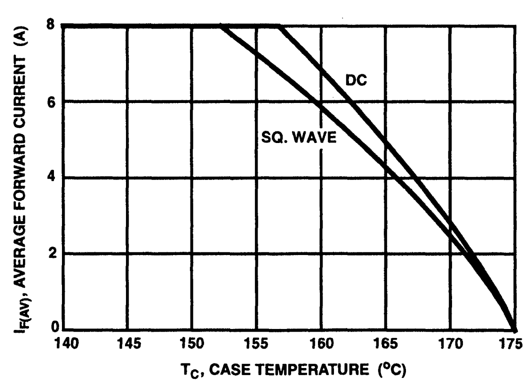


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

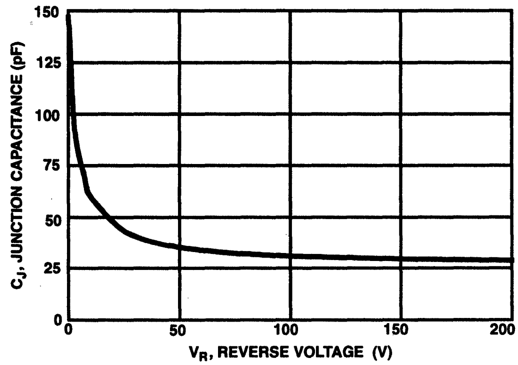


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

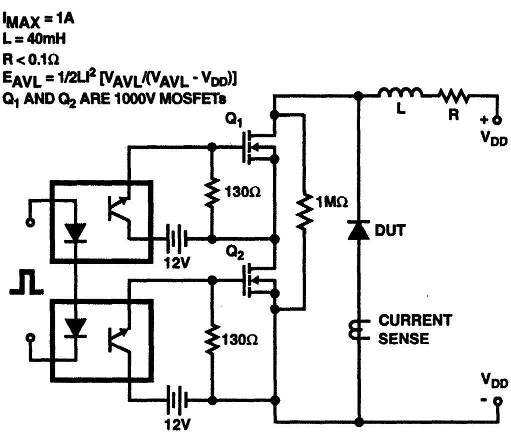


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

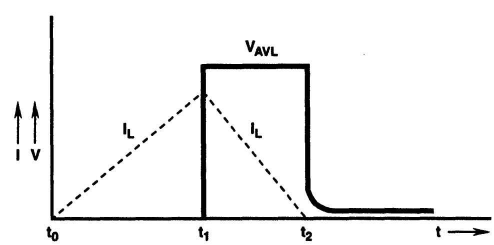


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

MUR840, MUR850, MUR860, RURP840, RURP850, RURP860

HARRIS SEMICONDUCTOR

June 1995

8A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast Recovery Time (t_{RR} < 50ns)
- Low Forward Voltage
- Low Thermal Resistance
- Hard Glass Passivation
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Output Rectification in Switching Power Supplies

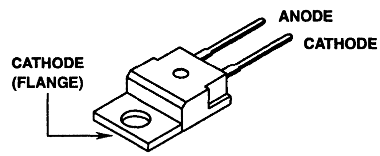
Description

MUR840, MUR850, MUR860 and RURP840, RURP850, RURP860 are low forward voltage drop ultrafast recovery rectifiers (t_{RR} < 50ns). They use a glass-passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodes in a variety of high-frequency pulse-width modulated switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

Package

JEDEC TO-220AC



Symbol

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR840	TO-220AC	MUR840
RURP840	TO-220AC	RURP840
MUR850	TO-220AC	MUR850
RURP850	TO-220AC	RURP850
MUR860	TO-220AC	MUR860
RURP860	TO-220AC	RURP860

NOTE: When ordering, use the entire part number.

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MUR840 RURP840	MUR850 RURP850	MUR860 RURP860
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage, V_{RWM} DC Blocking Voltage, V_R	V_{RRM}	400V	500V	600V
Average Rectified Forward Current Total Device, (Rated V_R), T_C = +150°C	$I_{F(AV)}$	8A	8A	8A
Peak Repetitive Forward Current (Rated V_R, Square Wave, 20kHz), T_C = +150°C	I_{FM}	16A	16A	16A
Nonrepetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60Hz)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C
Maximum Lead Temperature During Solder (At distance > $^1/_8$" (3.17mm) from case for 10s max)	T_L	260°C	260°C	260°C

File Number **2091.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR840, RURP840			MUR850, RURP850			MUR860, RURP860			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A, T_C = +150°C	-	-	1.0	-	-	1.2	-	-	1.2	V
	I_F = 8A, T_C = +25°C	-	-	1.3	-	-	1.5	-	-	1.5	V
IR at T_C = +150°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
IR at T_C = +25°C	V_R = 400V	-	-	100	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	100	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A (Note 1)	-	-	60	-	-	60	-	-	60	ns
	I_F = 0.5 (Note 2)	-	-	50	-	-	50	-	-	50	ns
$R_{\theta JC}$		-	-	2	-	-	2	-	-	2	°C/W

NOTES:

1. dI_F/dt = 50A/µs.
2. I_R = 1.0A, I_{REC} = 0.25A.

Typical Performance Curves

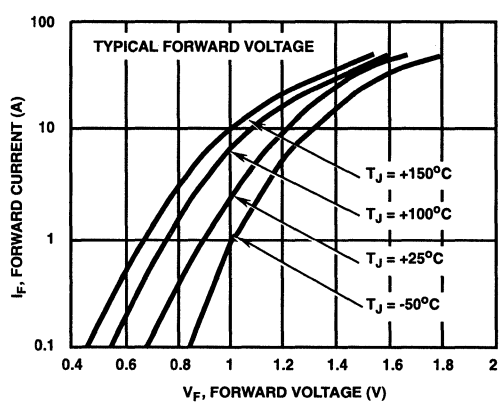


FIGURE 1. TYPICAL FORWARD VOLTAGE (MUR840, RUR840)

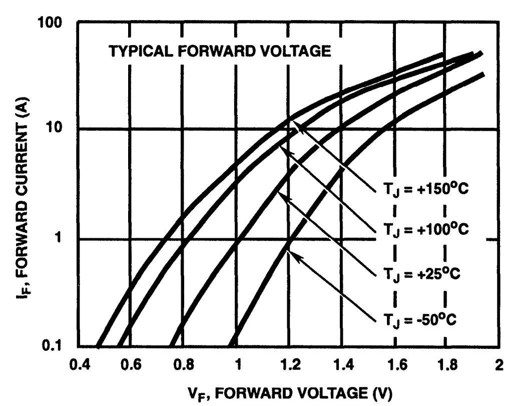


FIGURE 2. TYPICAL FORWARD VOLTAGE (MUR850, MUR860, RUR850, AND RUR860)

Typical Performance Curves (Continued)

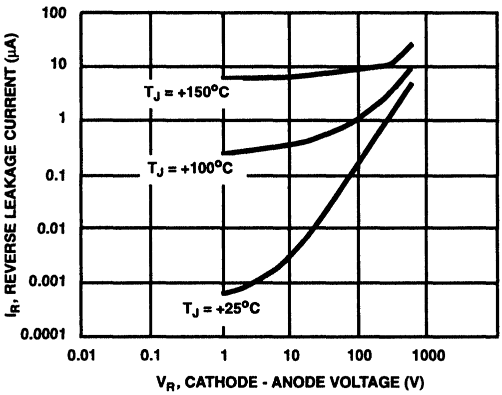


FIGURE 3.TYPICAL REVERSE LEAKAGE (MUR840, RURP840)

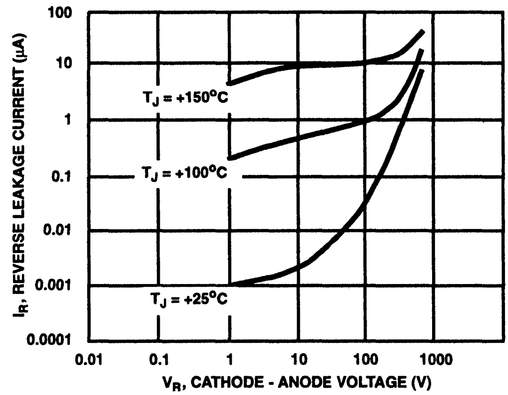


FIGURE 4. TYPICAL REVERSE LEAKAGE (MUR850, MUR860, RURP850, AND RURP860)

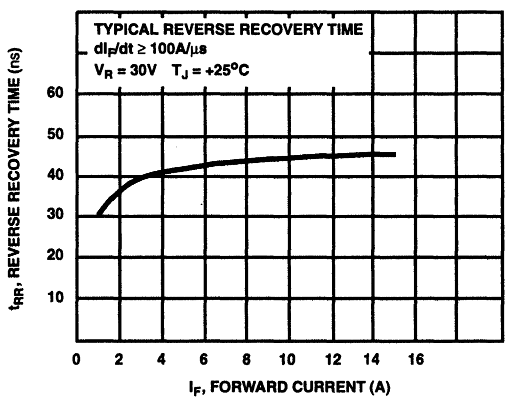


FIGURE 5. TYPICAL REVERSE RECOVERY TIME (ALL TYPES)

5

ULTRAFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

MUR870E, MUR880E, MUR890E, MUR8100E, RURP870, RURP880, RURP890, RURP8100

April 1995

8A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 75ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

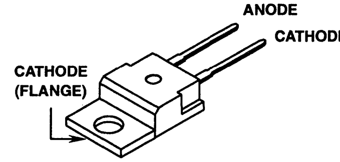
Description

MUR870E, MUR880E, MUR890E, MUR8100E and RUR870, RUR880, RUR890, RUR8100 are ultrafast dual diodes (t_{RR} < 75ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

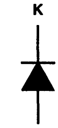
These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

Package

JEDEC TO-220AC



Symbol



PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR870E	TO-220AC	MUR870
MUR880E	TO-220AC	MUR880
MUR890E	TO-220AC	MUR890
MUR8100E	TO-220AC	MUR8100
RURP870	TO-220AC	RURP870
RURP880	TO-220AC	RURP880
RURP890	TO-220AC	RURP890
RURP8100	TO-220AC	RURP8100

NOTE: When ordering, use entire part number.

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	MUR870E RURP870	MUR880E RURP880	MUR890E RURP890	MUR8100E RURP8100
Peak Repetitive Reverse Voltage . . . . . V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage . . . . . V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage . . . . . V_R	700V	800V	900V	1000V
Average Rectified Forward Current . . . . . $I_{F(AV)}$ Total device forward current at rated V_R and T_C = +150°C)	8A	8A	8A	8A
Peak Forward Repetitive Current . . . . . I_{FRM} (Rated V_R, square wave 20kHZ)	16A	16A	16A	16A
Nonrepetitive Peak Surge Current . . . . . I_{FSM} (Surge applied at rated load condition halfwave 1 phase 60Hz)	100A	100A	100A	100A
Operating and Storage Temperature . . . . . T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS MUR870E, RURP870 MIN	TYP	MAX	MUR880E, RURP880 MIN	TYP	MAX	MUR890E, RURP890 MIN	TYP	MAX	MUR8100E, RURP8100 MIN	TYP	MAX	UNITS
V_F	$I_F = 8A$, $T_C = +150^oC$	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	$I_F = 8A$, $T_C = +25^oC$	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at $T_C = +150^oC$	$V_R = 700V$	-	-	500	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V$	-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V$	-	-	-	-	-	-	-	-	500	-	-	-	μA
	$V_R = 1000V$	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R at $T_C = +25^oC$	$V_R = 700V$	-	-	100	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V$	-	-	-	-	-	100	-	-	-	-	-	-	μA
	$V_R = 900V$	-	-	-	-	-	-	-	-	100	-	-	-	μA
	$V_R = 1000V$	-	-	-	-	-	-	-	-	-	-	-	100	μA
t_{RR}	$I_F = 1A$	-	-	100	-	-	100	-	-	100	-	-	100	ns
	$I_F = 8A$	-	-	110	-	-	110	-	-	110	-	-	110	ns
t_A	$I_F = 1A$	-	40	-	-	40	-	-	40	-	-	40	-	ns
	$I_F = 8A$	-	45	-	-	45	-	-	45	-	-	45	-	ns
t_B	$I_F = 1A$	-	20	-	-	20	-	-	20	-	-	20	-	ns
	$I_F = 8A$	-	20	-	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	2.0	-	-	2.0	-	-	2.0	-	-	2.0	$^oC/W$
E_{AVL}	See Fig. 7 & 8	-	-	20	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time at dI_F/dt = 100A/μs (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current at dI_F/dt = 100A/μs (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

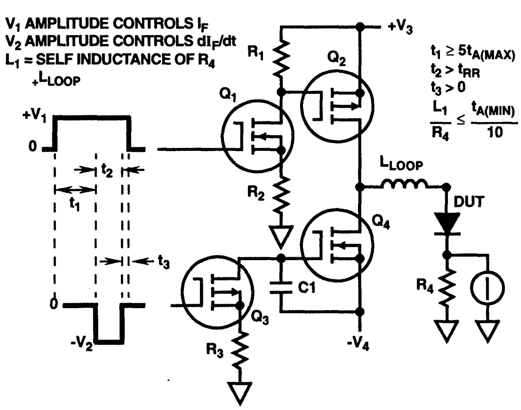


FIGURE 1. t_{RR} TEST CIRCUIT

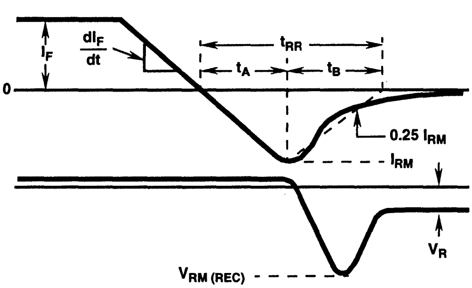


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

5
ULTRAFAST SINGLE DIODES

Typical Performance Curves

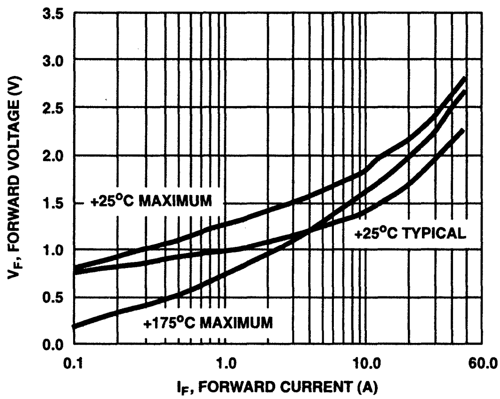


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

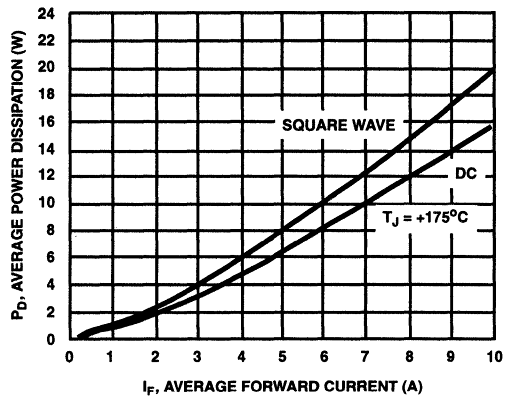


FIGURE 4. AVERAGE FORWARD CURRENT vs AVERAGE POWER DISSIPATION

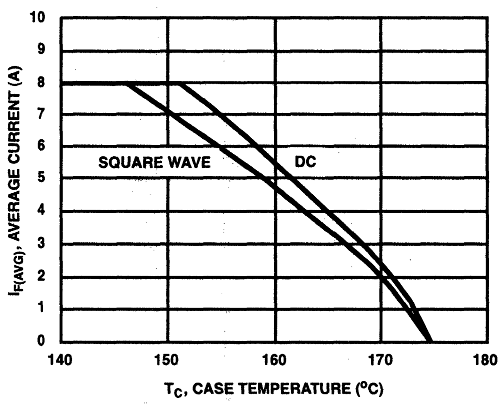


FIGURE 5. AVERAGE FORWARD CURRENT vs CASE TEMPERATURE

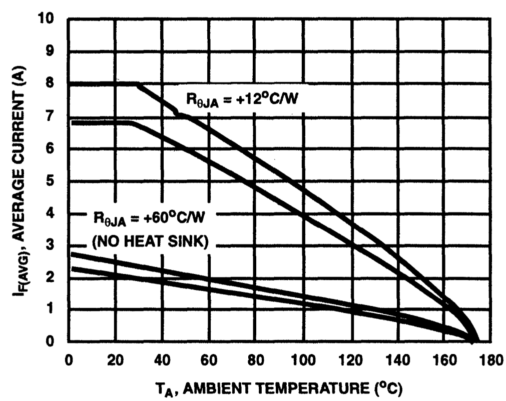


FIGURE 6. AVERAGE FORWARD CURRENT vs AMBIENT TEMPERATURE

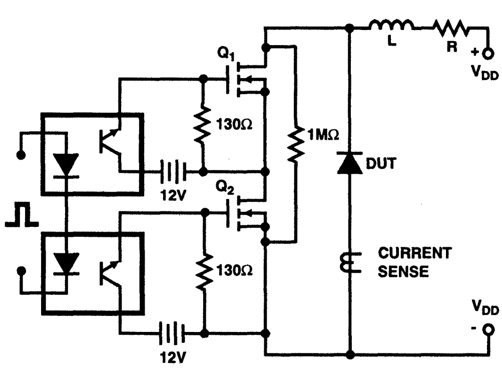


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

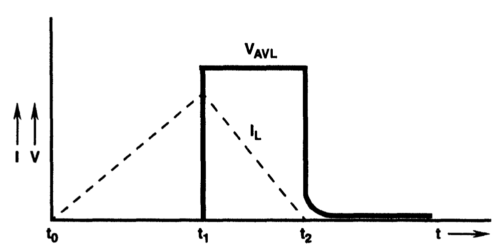


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2)\ LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

MUR1510, MUR1515, MUR1520, RURP1510, RURP1515, RURP1520

April 1995

15A, 100V - 200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 30ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

MUR1510, MUR1515, MUR1520 and RURP1510, RURP1515, RURP1520 are ultrafast dual diodes (t_{RR} < 30ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

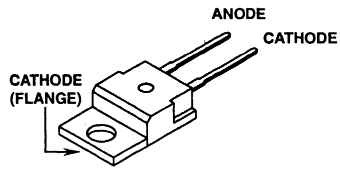
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR1510	TO-220AC	MUR1510
RURP1510	TO-220AC	RURP1510
MUR1515	TO-220AC	MUR1515
RURP1515	TO-220AC	RURP1515
MUR1520	TO-220AC	MUR1520
RURP1520	TO-220AC	RURP1520

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MUR1510 RURP1510	MUR1515 RURP1515	MUR1520 RURP1520
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, Square Wave 20kHz)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

File Number **2779.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR1510, RURP1510			MUR1515, RURP1515			MUR1520, RURP1520			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
	I_F = 15A, T_C = +25°C	-	-	1.05	-	-	1.05	-	-	1.05	V
I_R at T_C = +150°C	V_R = 100V	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +25°C	V_R = 100V	-	-	100	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	100	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	30	-	-	30	-	-	30	ns
	I_F = 15A	-	-	35	-	-	35	-	-	35	ns
t_A	I_F = 1A	-	18	-	-	18	-	-	18	-	ns
	I_F = 15A	-	20	-	-	20	-	-	20	-	ns
t_B	I_F = 1A	-	9	-	-	9	-	-	9	-	ns
	I_F = 15A	-	10	-	-	10	-	-	10	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}	See Fig. 7 & 8	-	-	20	-	-	20	-	-	20	mJ

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

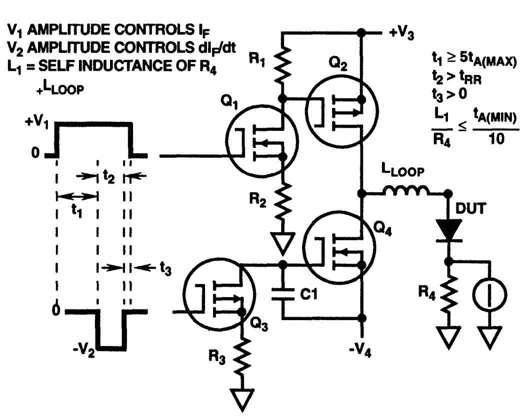


FIGURE 1. t_{RR} TEST CIRCUIT

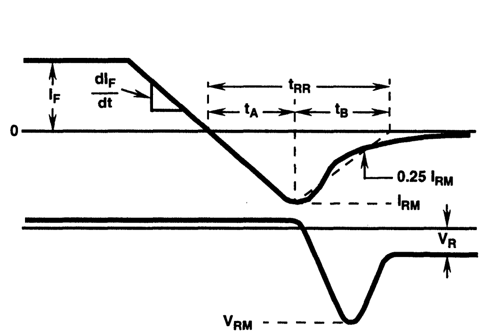


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

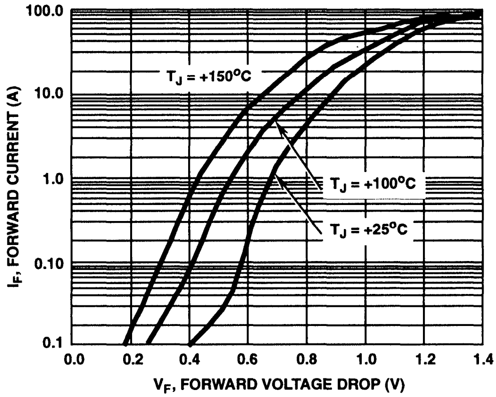


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

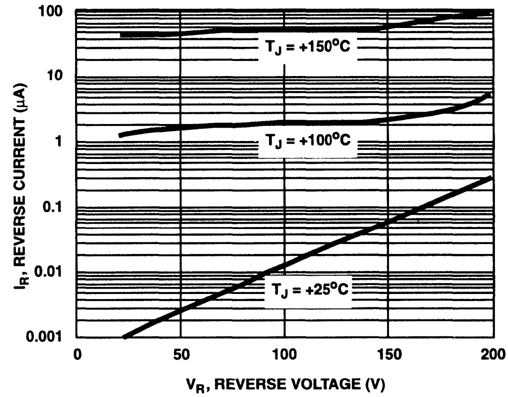


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

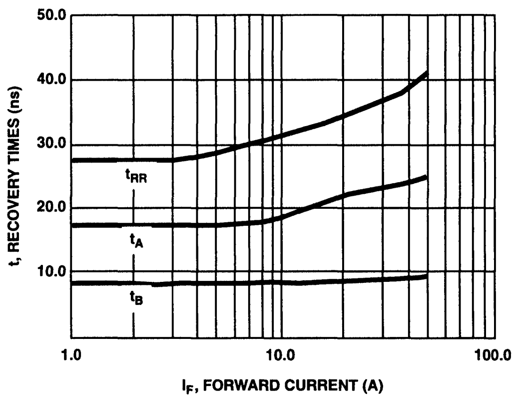


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

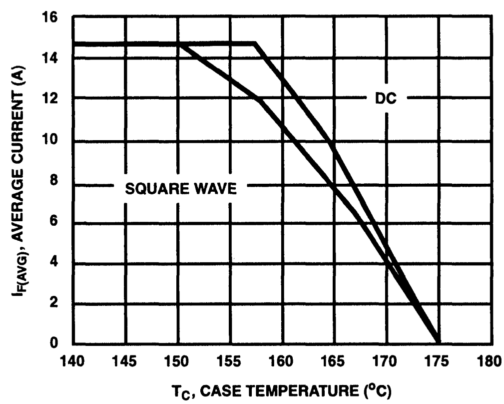


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

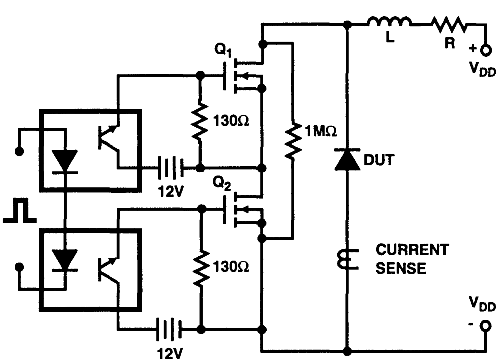


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

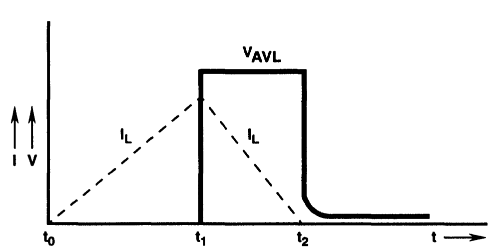


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2)\, LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

HARRIS SEMICONDUCTOR

MUR1540, MUR1550, MUR1560, RURP1540, RURP1550, RURP1560

April 1995

15A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

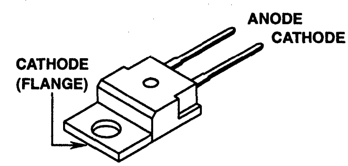
Description

MUR1540, MUR1550, MUR1560 and RURP1540, RURP1550, RURP1560 are ultrafast dual diodes (t_{RR} < 55ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

Package

JEDEC TO-220AC



Symbol

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR1540	TO-220AC	MUR1540
RURP1540	TO-220AC	RURP1540
MUR1550	TO-220AC	MUR1550
RURP1550	TO-220AC	RURP1550
MUR1560	TO-220AC	MUR1560
RURP1560	TO-220AC	RURP1560

NOTE: When ordering, use the entire part number

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MUR1540 RURP1540	MUR1550 RURP1550	MUR1560 RURP1560
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR1540, RURP1540			MUR1550, RURP1550			MUR1560, RURP1560			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +150°C	-	-	1.12	-	-	1.20	-	-	1.20	V
	I_F = 15A, T_C = +25°C	-	-	1.25	-	-	1.50	-	-	1.50	V
I_R at T_C = +150°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +25°C	V_R = 400V	-	-	100	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	100	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 15A	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 15A	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 15A	-	17	-	-	17	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}	See Fig. 7 & 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

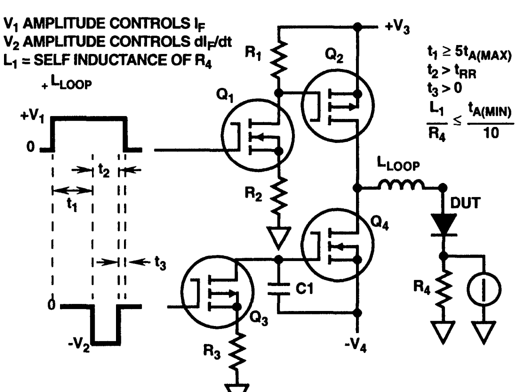


FIGURE 1. t_{RR} TEST CIRCUIT

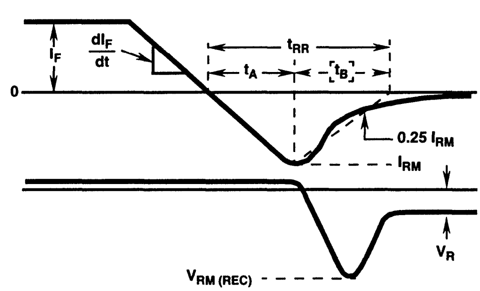


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

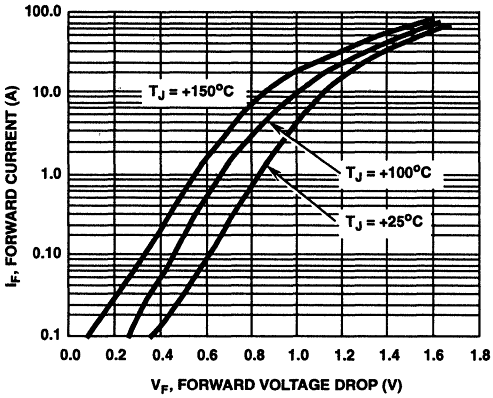


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

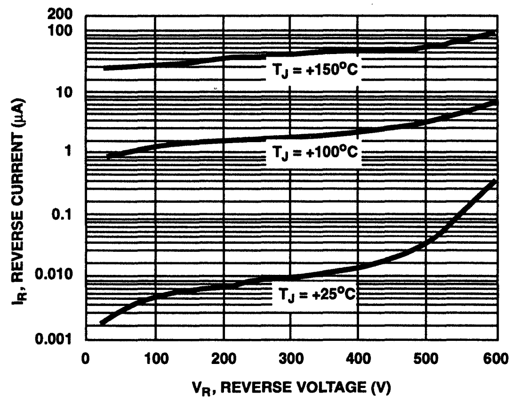


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

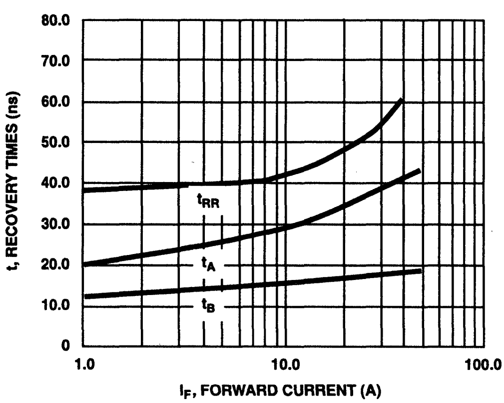


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

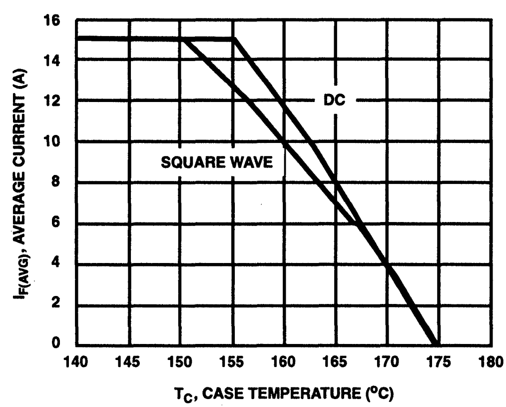


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

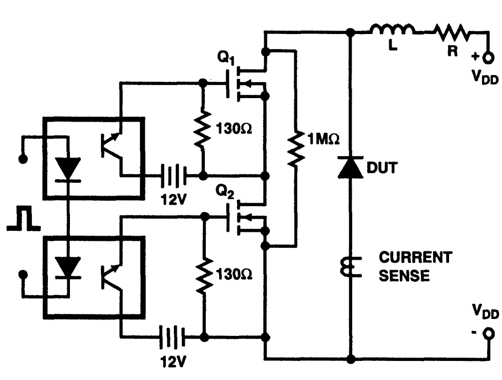


FIGURE 7. AVALANCHE ENERY TEST CIRCUIT

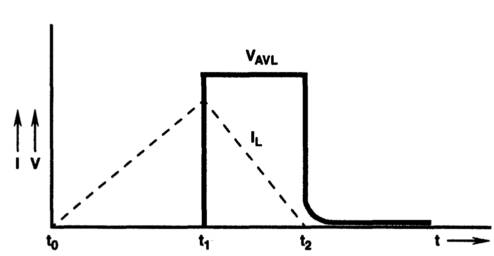


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2)\ LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

HARRIS SEMICONDUCTOR

RURD410, RURD415, RURD420, RURD410S, RURD415S, RURD420S

April 1995

4A, 100V - 200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <30ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

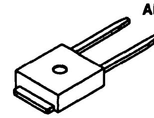
Description

RURD410, RURD415, RURD420, RURD410S, RURD415S, and RURD420S (TA49034) are ultrafast diodes with soft recovery characteristics (t_{RR} < 30ns). They have low forward voltage drop and are ion-implanted epitaxial planar construction.

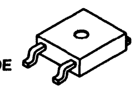
These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD410	TO-251	RUR410
RURD415	TO-251	RUR415
RURD420	TO-251	RUR420
RURD410S	TO-252	RUR410
RURD415S	TO-252	RUR415
RURD420S	TO-252	RUR420

NOTE: When ordering, use the entire part number.

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	RURD410 RURD410S	RURD415 RURD415S	RURD420 RURD420S	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	100	150	200	V
Working Peak Reverse Voltage . . . . V_{RWM}	100	150	200	V
DC Blocking Voltage . . . . V_R	100	150	200	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ (T_C = +159°C)	4	4	4	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	8	8	8	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	40	40	40	A
Maximum Power Dissipation . . . . P_D	30	30	30	W
Avalanche Energy (L = 40mH) . . . . E_{AVL}	10	10	10	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3614.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURD410 RURD410S			RURD415 RURD415S			RURD420 RURD420S			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 4A, T_C = +25^oC$	-	-	1.0	-	-	1.0	-	-	1.0	V
V_F	$I_F = 4A, T_C = +150^oC$	-	-	0.83	-	-	0.83	-	-	0.83	
I_R	$V_R = 100V, T_C = +25^oC$ $V_R = 150V, T_C = +25^oC$ $V_R = 200V, T_C = +25^oC$	- - -	- - -	100 - -	- - -	- - -	- 100 -	- - -	- - -	- - 100	μA
I_R	$V_R = 100V, T_C = +150^oC$ $V_R = 150V, T_C = +150^oC$ $V_R = 200V, T_C = +150^oC$	- - -	- - -	500 - -	- - -	- - -	- 500 -	- - -	- - -	- - 500	μA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	30	-	-	30	-	-	30	ns
	$I_F = 4A, dI_F/dt = 100A/\mu s$	-	-	35	-	-	35	-	-	35	
t_A	$I_F = 4A, dI_F/dt = 100A/\mu s$	-	11	-	-	11	-	-	11	-	
t_B	$I_F = 4A, dI_F/dt = 100A/\mu s$	-	9	-	-	9	-	-	9	-	
Q_{RR}	$I_F = 4A, dI_F/dt = 100A/\mu s$	-	12	-	-	12	-	-	12	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	15	-	-	15	-	-	15	-	pF
$R_{\theta JC}$		-	-	5	-	-	5	-	-	5	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 9 and 10).

pw = pulse width.

D = duty cycle.

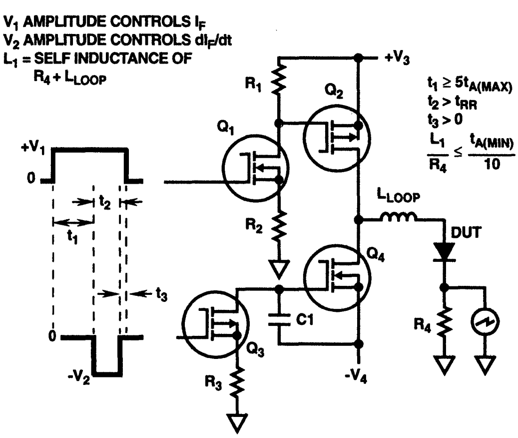


FIGURE 1. t_{RR} TEST CIRCUIT

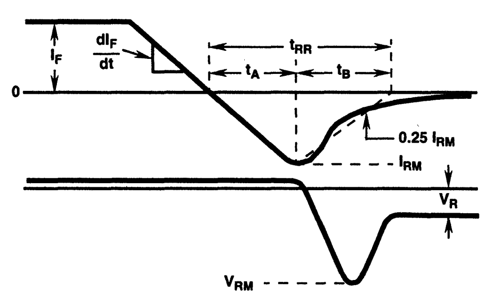


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

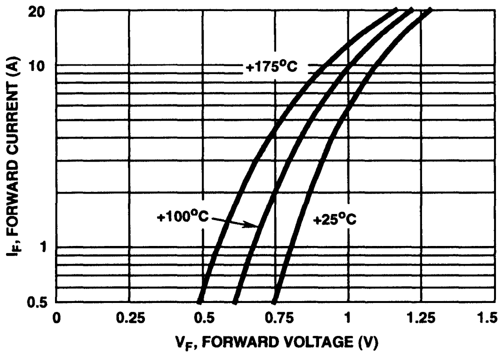


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

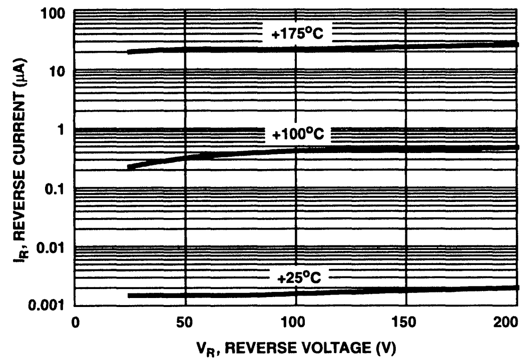


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

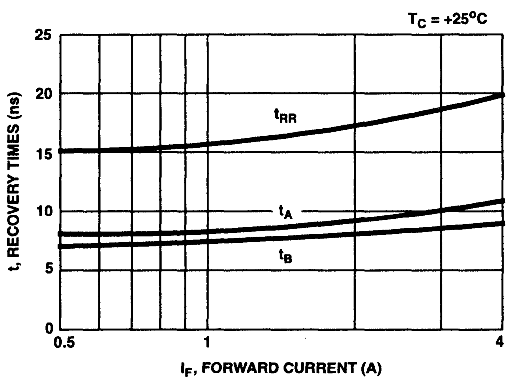


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

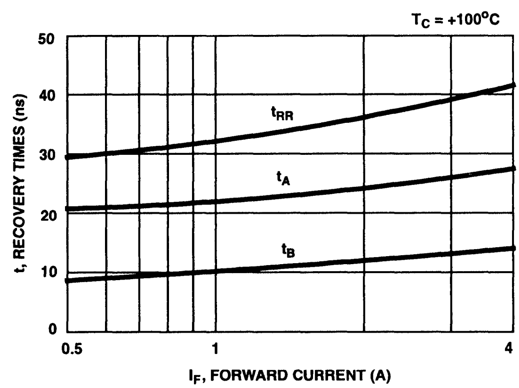


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

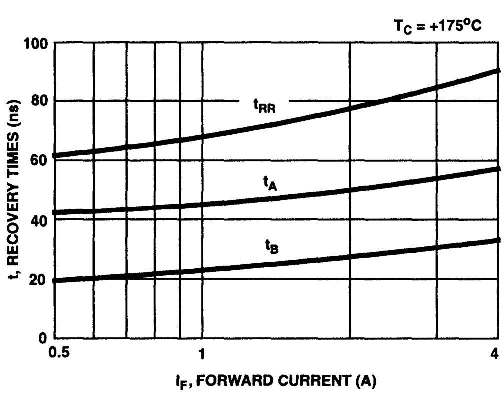


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

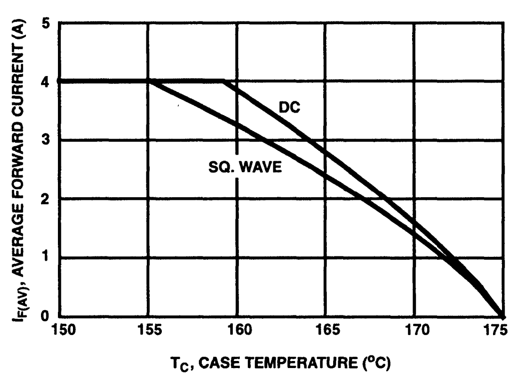


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

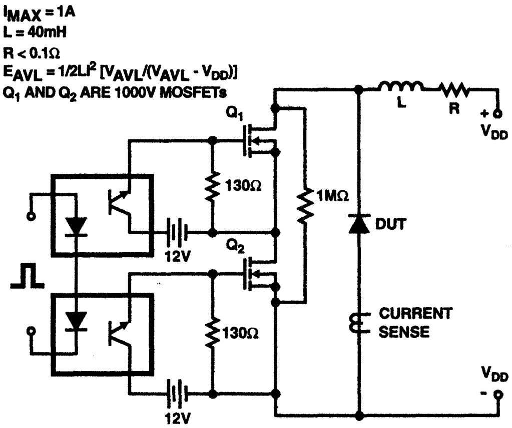


FIGURE 9. AVALANCHE ENERGY TEST CIRCUIT

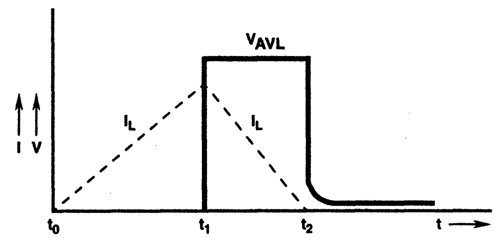


FIGURE 10. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURD440, RURD450, RURD460, RURD440S, RURD450S, RURD460S

April 1995

4A, 400V - 600V Ultrafast Diodes

Features

- **Ultrafast with Soft Recovery .... <55ns**
- **Operating Temperature .... +175°C**
- **Reverse Voltage Up To 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RURD440, RURD450, RURD460, RURD440S, RURD450S and RURD460S (TA49035) are ultrafast diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

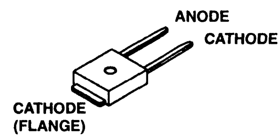
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD440	TO-251	RUR440
RURD450	TO-251	RUR450
RURD460	TO-251	RUR460
RURD440S	TO-252	RUR440
RURD450S	TO-252	RUR450
RURD460S	TO-252	RUR460

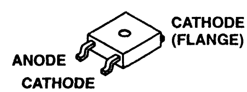
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURD440 RURD440S	RURD450 RURD450S	RURD460 RURD460S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +160°C)	$I_{F(AV)}$	4	4	4	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	8	8	8	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	40	40	40	A
Maximum Power Dissipation	P_D	50	50	50	W
Avalanche Energy (L = 40mH)	E_{AVL}	10	10	10	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURD440, RURD440S			RURD450, RURD450S			RURD460, RURD460S			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 4A, T_C = +25°C	-	-	1.5	-	-	1.5	-	-	1.5	V
V_F	I_F = 4A, T_C = +150°C	-	-	1.2	-	-	1.2	-	-	1.2	V
I_R	V_R = 400V, T_C = +25°C	-	-	100	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	100	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	55	-	-	55	-	-	55	ns
	I_F = 4A, dI_F/dt = 100A/μs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 4A, dI_F/dt = 100A/μs	-	32	-	-	32	-	-	32	-	ns
t_B	I_F = 4A, dI_F/dt = 100A/μs	-	15	-	-	15	-	-	15	-	ns
Q_{RR}	I_F = 4A, dI_F/dt = 100A/μs	-	50	-	-	50	-	-	50	-	nC
C_J	V_R = 10V, I_F = 0A	-	15	-	-	15	-	-	15	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 9 and 10).

pw = pulse width.

D = duty cycle.

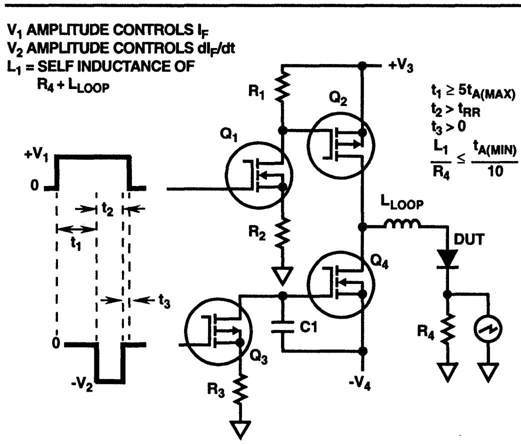


FIGURE 1. t_{RR} TEST CIRCUIT

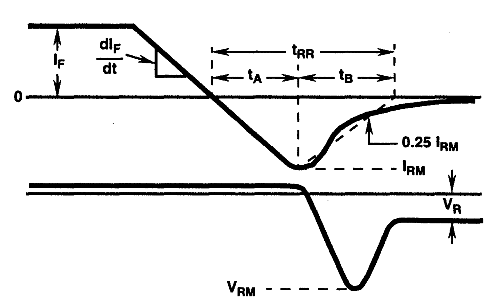


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

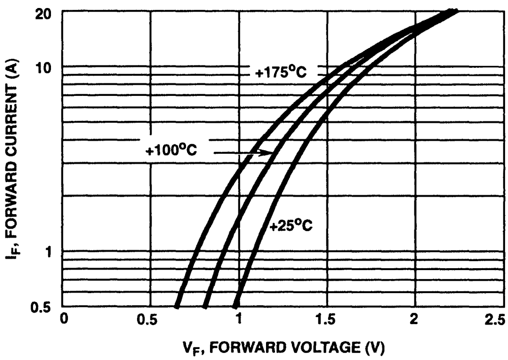


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

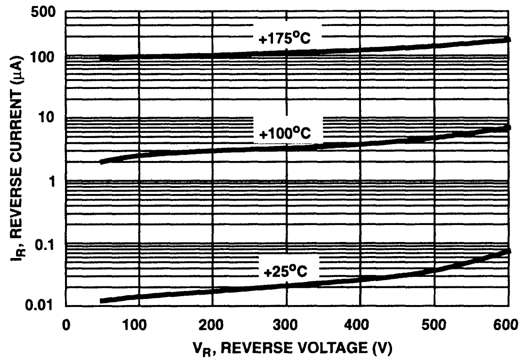


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

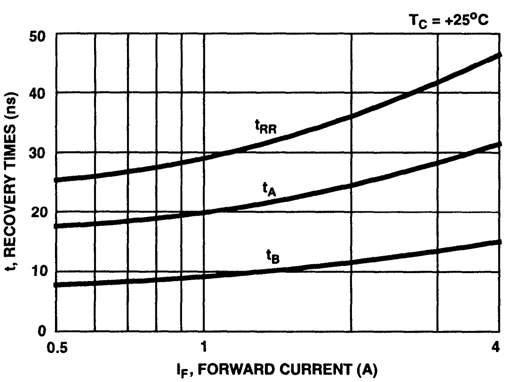


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

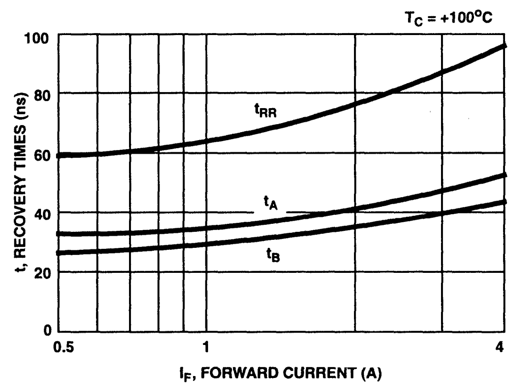


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

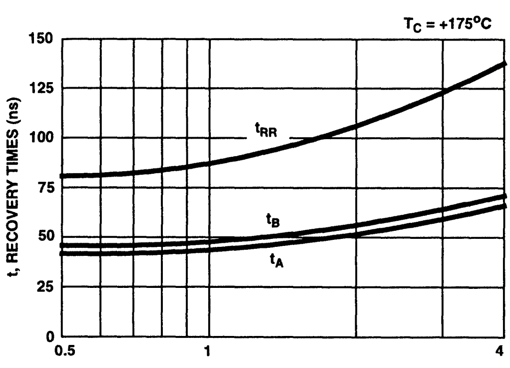


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

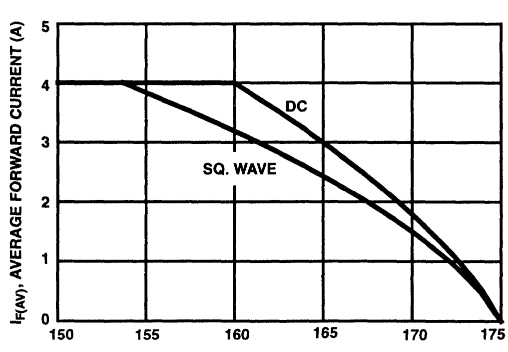


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

5
ULTRAFAST SINGLE DIODES

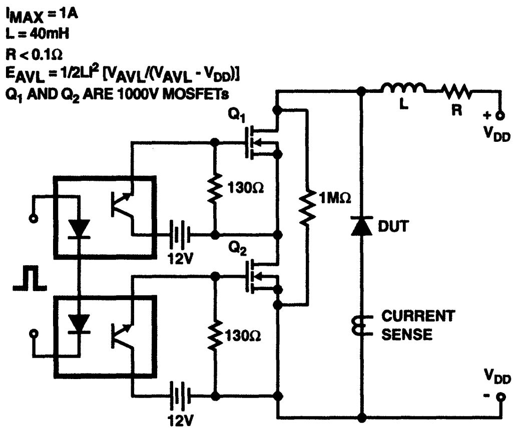


FIGURE 9. AVALANCHE ENERGY TEST CIRCUIT

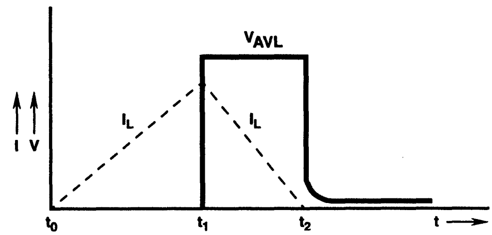


FIGURE 10. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS
SEMICONDUCTOR

RURD4120, RURD4120S

April 1995

4A, 1200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <70ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURD4120 and RURD4120S (TA49036) are ultrafast diodes with soft recovery characteristics (t_{RR} < 70ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

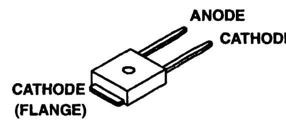
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD4120	TO-251	UR4120
RURD4120S	TO-252	UR4120

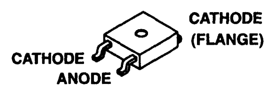
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252 variant in the tape and reel, i.e., RURD4120S9A.

Packages

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURD4120, RURD4120S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +152°C)	$I_{F(AV)}$	4	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	8	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	40	A
Maximum Power Dissipation	P_D	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	10	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURD4120, RURD4120S MIN	TYP	MAX	UNITS
V_F	I_F = 4A, T_C = +25°C	-	-	2.1	V
	I_F = 4A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	70	ns
	I_F = 4A, dI_F/dt = 200A/µs	-	-	90	ns
t_A	I_F = 4A, dI_F/dt = 200A/µs	-	40	-	ns
t_B	I_F = 4A, dI_F/dt = 200A/µs	-	28	-	ns
Q_{RR}	I_F = 4A, dI_F/dt = 200A/µs	-	335	-	nC
C_J	V_R = 10V, I_F = 0A	-	15	-	pF
$R_{\theta JC}$		-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery time.

C_J = Junction capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled Avalanche Energy, (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

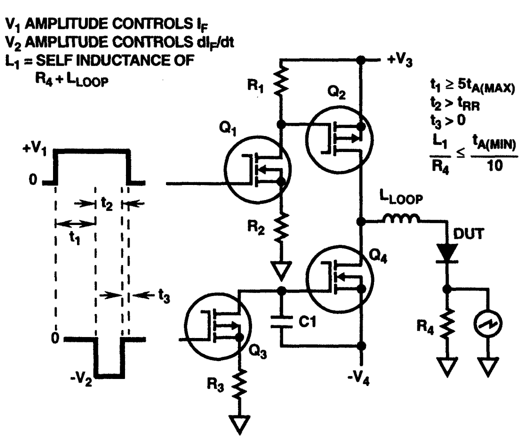


FIGURE 1. t_{RR} TEST CIRCUIT

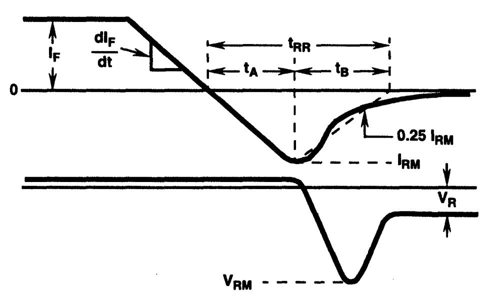


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

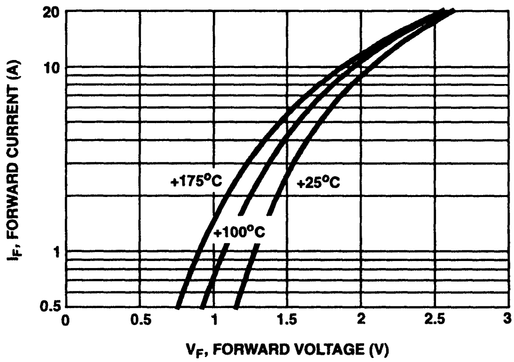


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

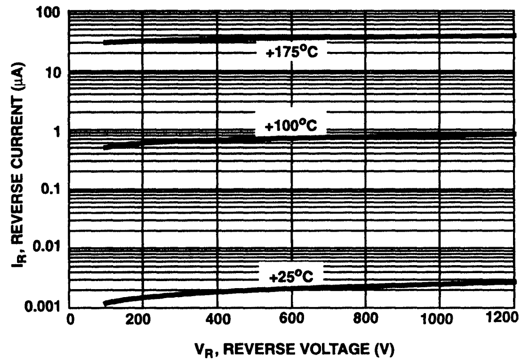


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

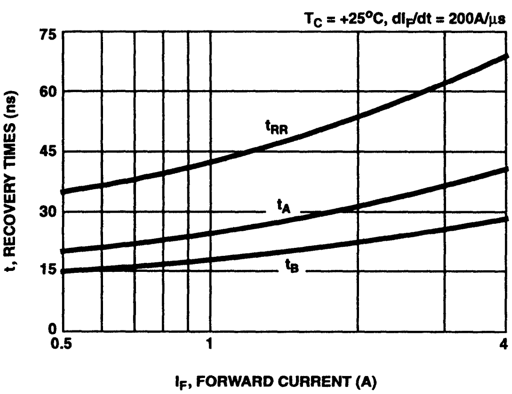


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

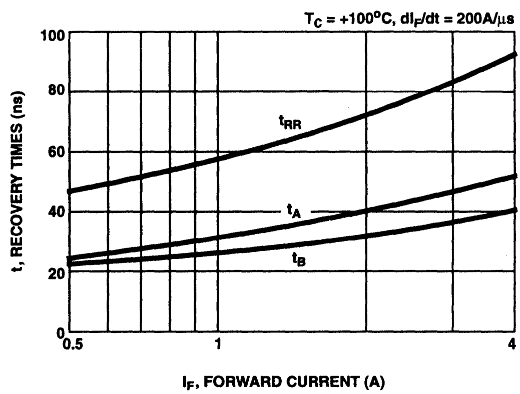


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

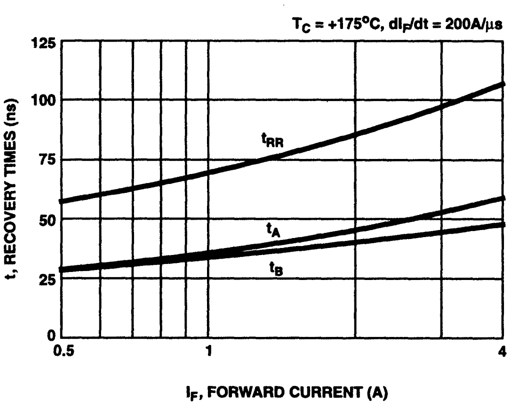


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

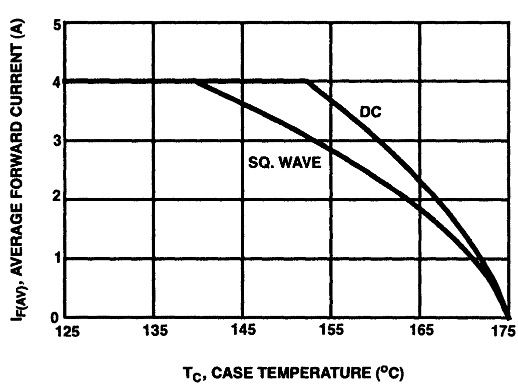


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

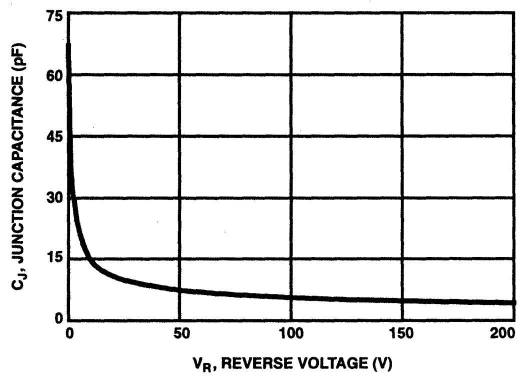


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

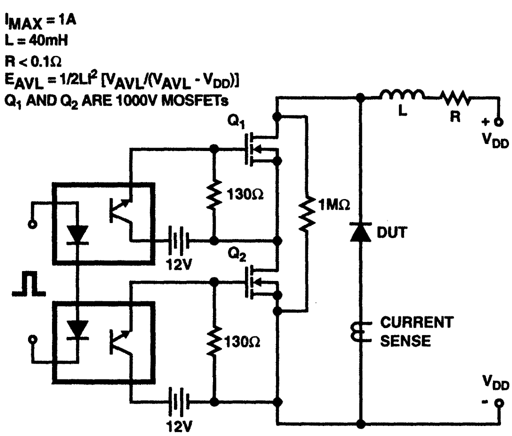


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

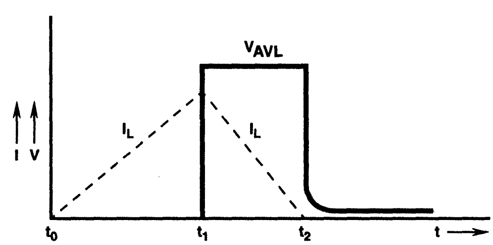


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURD610, RURD615, RURD620, RURD610S, RURD615S, RURD620S

April 1995

6A, 100V - 200V Ultrafast Diodes

Features

- **Ultrafast with Soft Recovery** .... <30ns
- **Operating Temperature** .... +175°C
- **Reverse Voltage Up To** 200V
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RURD610, RURD615, RURD620, RURD610S, RURD615S and RURD620S (TA49037) are ultrafast diodes with soft recovery characteristics (t_{RR} < 30ns). They have low forward voltage drop and are ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

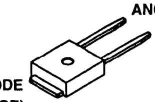
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD610	TO-251	RUR610
RURD615	TO-251	RUR615
RURD620	TO-251	RUR620
RURD610S	TO-252	RUR610
RURD615S	TO-252	RUR615
RURD620S	TO-252	RUR620

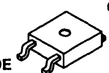
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252 variant in the tape and reel, i.e., RURD610S9A.

Packaging

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURD610 RURD610S	RURD615 RURD615S	RURD620 RURD620S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	100	150	200	V
Working Peak Reverse Voltage	V_{RWM}	100	150	200	V
DC Blocking Voltage	V_R	100	150	200	V
Average Rectified Forward Current (T_C = +160°C)	$I_{F(AV)}$	6	6	6	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	12	12	12	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	60	60	60	A
Maximum Power Dissipation	P_D	45	45	45	W
Avalanche Energy (L = 40mH)	E_{AVL}	10	10	10	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3640.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS RURD610 RURD610S MIN	TYP	MAX	RURD615 RURD615S MIN	TYP	MAX	RURD620 RURD620S MIN	TYP	MAX	UNITS
V_F	I_F = 6A, T_C = +25°C	-	-	1.0	-	-	1.0	-	-	1.0	V
	I_F = 6A, T_C = +150°C	-	-	0.83	-	-	0.83	-	-	0.83	V
I_R	V_R = 100V, T_C = +25°C	-	-	100	-	-	-	-	-	-	µA
	V_R = 150V, T_C = +25°C	-	-	-	-	-	100	-	-	-	µA
	V_R = 200V, T_C = +25°C	-	-	-	-	-	-	-	-	100	µA
I_R	V_R = 100V, T_C = +150°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V, T_C = +150°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V, T_C = +150°C	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	30	-	-	30	-	-	30	ns
	I_F = 6A, dI_F/dt = 100A/µs	-	-	35	-	-	35	-	-	35	ns
t_A	I_F = 6A, dI_F/dt= 100A/µs	-	16	-	-	16	-	-	16	-	ns
t_B	I_F = 6A, dI_F/dt = 100A/µs	-	7	-	-	7	-	-	7	-	ns
Q_{RR}	I_F = 6A, dI_F/dt = 100A/µs	-	15	-	-	15	-	-	15	-	nC
C_J	V_R = 10V, I_F = 0A	-	30	-	-	30	-	-	30	-	pF
$R_{\theta JC}$		-	-	3.5	-	-	3.5	-	-	3.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 9 and 10).
pw = pulse width.
D = duty cycle.

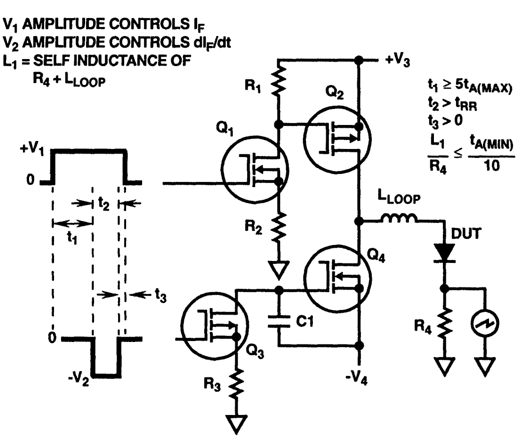


FIGURE 1. t_{RR} TEST CIRCUIT

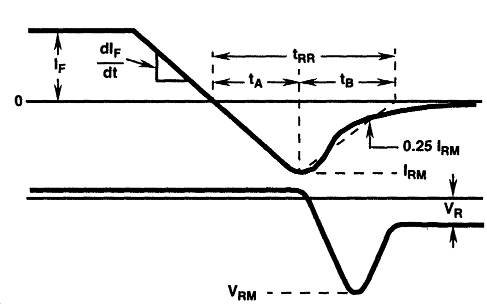


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

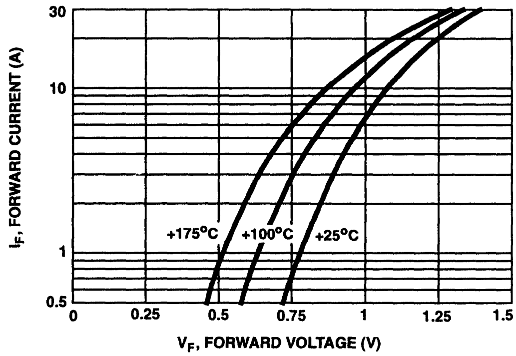


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

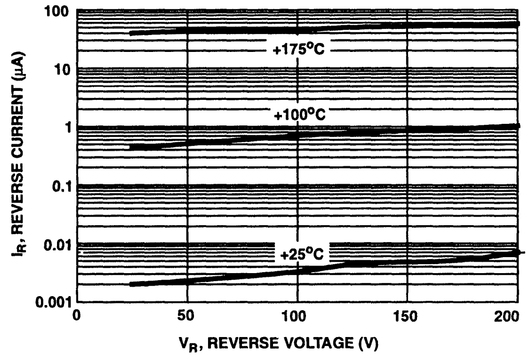


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

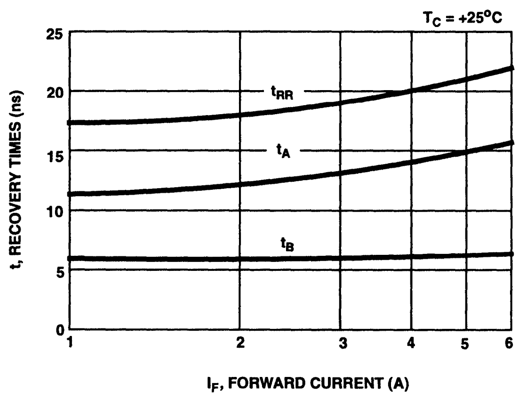


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

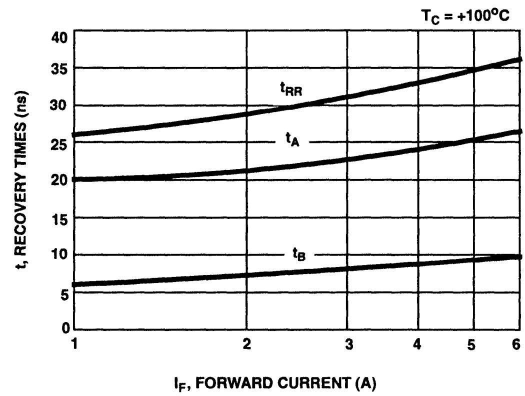


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

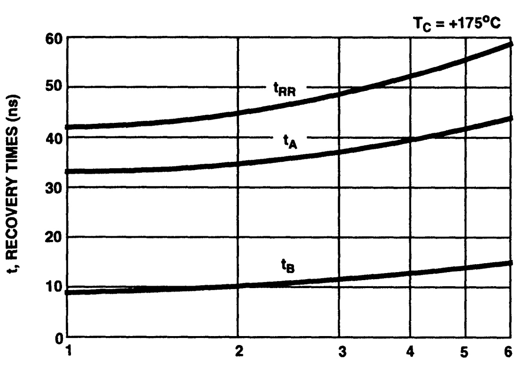


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

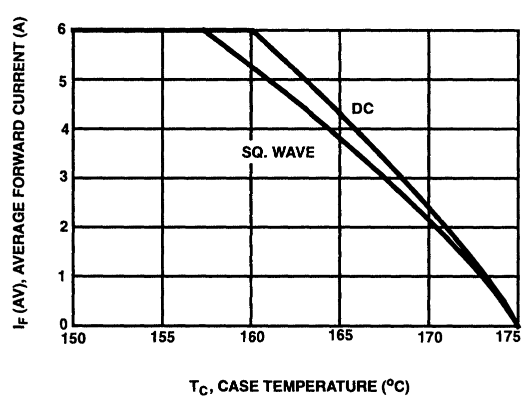


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

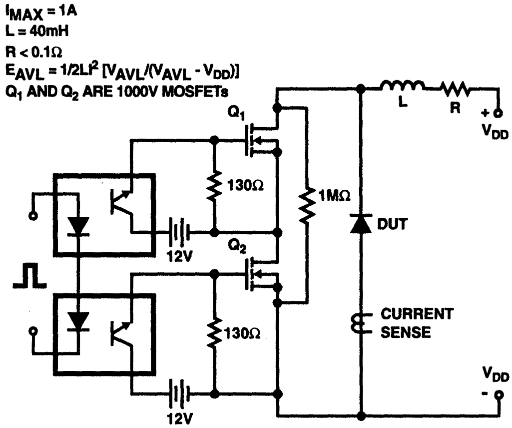


FIGURE 9. AVALANCHE ENERGY TEST CIRCUIT

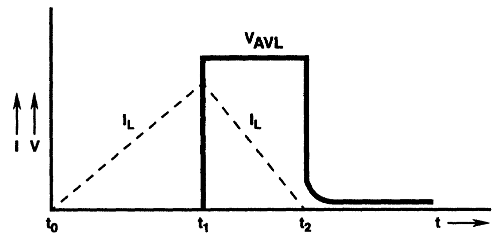


FIGURE 10. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURD640, RURD650, RURD660, RURD640S, RURD650S, RURD660S

April 1995

6A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURD640, RURD650, RURD660, RURD640S, RURD650S and RURD660S (TA49038) are ultrafast diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

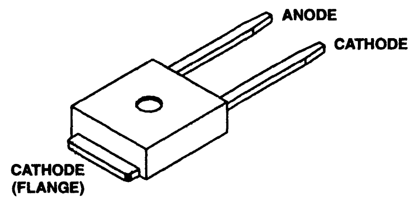
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD640	TO-251	RUR640
RURD650	TO-251	RUR650
RURD660	TO-251	RUR660
RURD640S	TO-252	RUR640
RURD650S	TO-252	RUR650
RURD660S	TO-252	RUR660

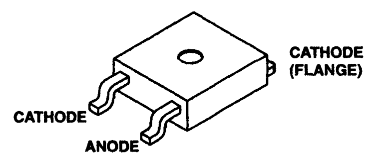
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252 variant in the tape and reel, i.e., RURD640S9A.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURD640 RURD640S	RURD650 RURD650S	RURD660 RURD660S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +155°C)	$I_{F(AV)}$	6	6	6	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	12	12	12	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	60	60	60	A
Maximum Power Dissipation	P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	10	10	10	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

5 ULTRAFAST SINGLE DIODES

File Number **3750.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURD640, RURD640S			RURD650, RURD650S			RURD660, RURD660S			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 6A, T_C = +25°C	-	-	1.5	-	-	1.5	-	-	1.5	V
	I_F = 6A, T_C = +150°C	-	-	1.2	-	-	1.2	-	-	1.2	V
I_R	V_R = 400V, T_C = +25°C	-	-	100	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	100	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	100	µA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	55	-	-	55	-	-	55	ns
	I_F = 6A, dI_F/dt = 200A/µs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 6A, dI_F/dt = 200A/µs	-	28	-	-	28	-	-	28	-	ns
t_B	I_F = 6A, dI_F/dt = 200A/µs	-	16	-	-	16	-	-	16	-	ns
Q_{RR}	I_F = 6A, dI_F/dt = 200A/µs	-	150	-	-	150	-	-	150	-	nC
C_J	V_R = 10V, I_F = 0A	-	25	-	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = Pulse width.
D = Duty cycle.

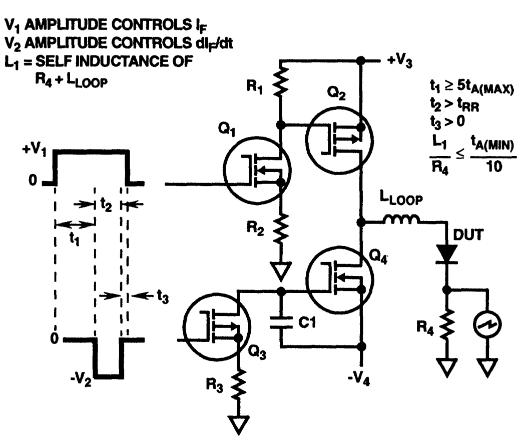


FIGURE 1. t_{RR} TEST CIRCUIT

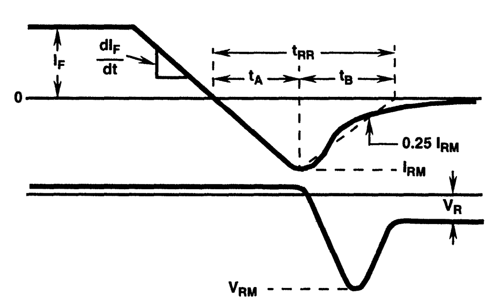


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

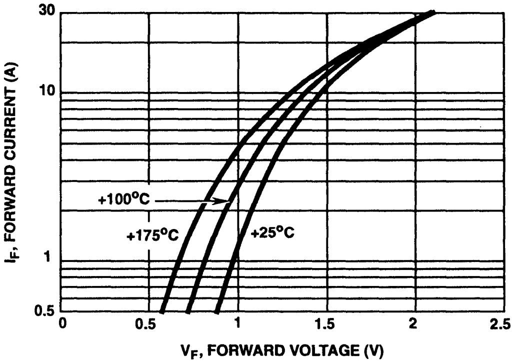


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

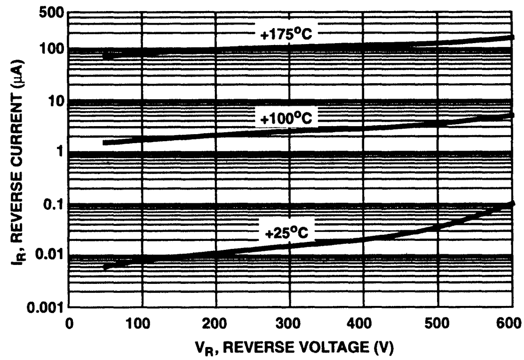


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

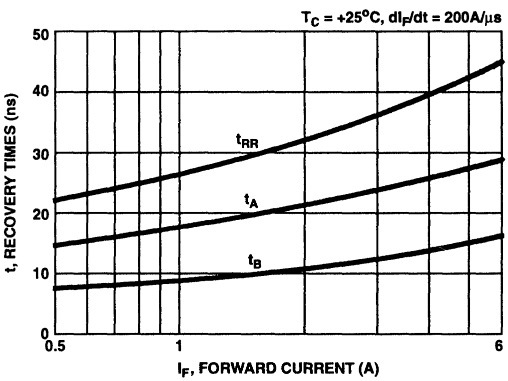


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

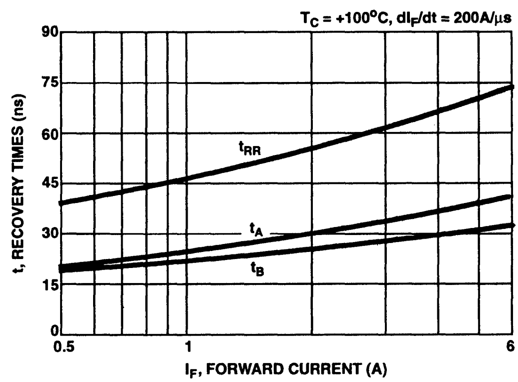


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

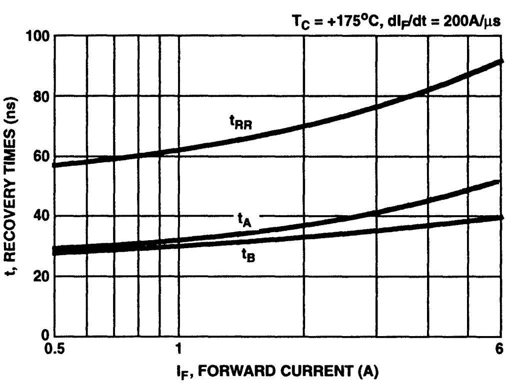


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

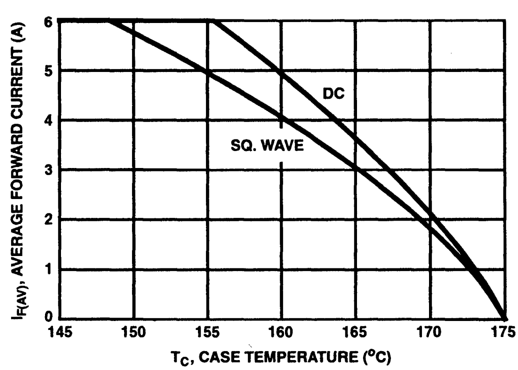


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

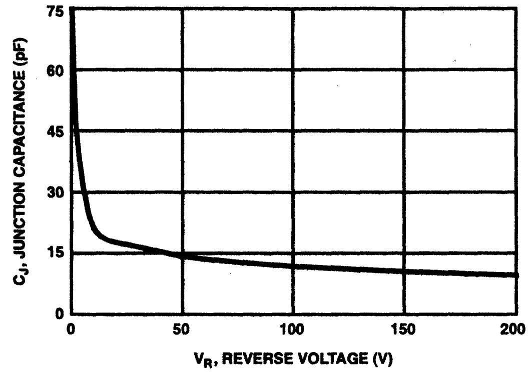


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

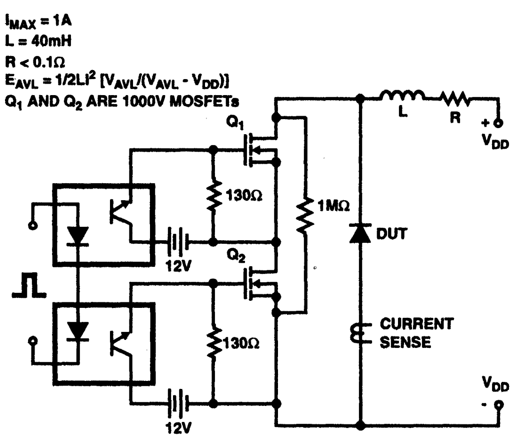


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

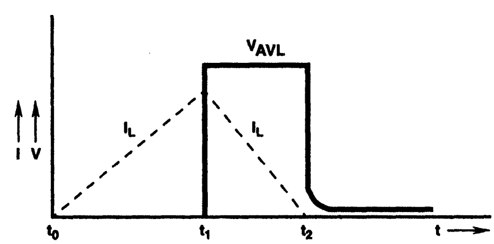


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURD6120, RURD6120S

April 1995

6A, 1200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <70ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURD6120 and RURD6120S (TA49039) are ultrafast diodes with soft recovery characteristics (t_{RR} < 70ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

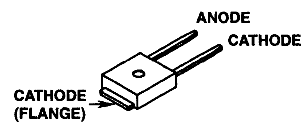
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURD6120	TO-251	UR6120
RURD6120S	TO-252	UR6120

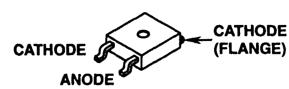
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252 variant in the tape and reel, i.e., RURD6120S9A.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURD6120 RURD6120S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 140°C)	$I_{F(AV)}$	6	A
Repetitive Peak Surge Current (Square Wave, 200kHz)	I_{FSM}	12	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	60	A
Maximum Power Dissipation	P_D	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	10	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number 3962.1

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURD6120 RURD6120S MIN	TYP	MAX	UNITS
V_F	I_F = 6A, T_C = +25°C	-	-	2.1	V
	I_F = 6A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	70	ns
	I_F = 6A, dI_F/dt = 200A/µs	-	-	90	ns
t_A	I_F = 6A, dI_F/dt = 200A/µs	-	45	-	ns
t_B	I_F = 6A, dI_F/dt = 200A/µs	-	30	-	ns
Q_{RR}	I_F = 6A, dI_F/dt = 200A/µs	-	400	-	nC
C_J	V_R = 10V, I_F = 0A	-	22	-	pF
$R_{\theta JC}$		-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

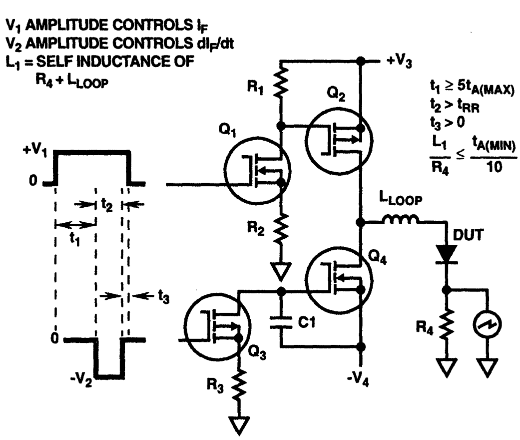


FIGURE 1. t_{RR} TEST CIRCUIT

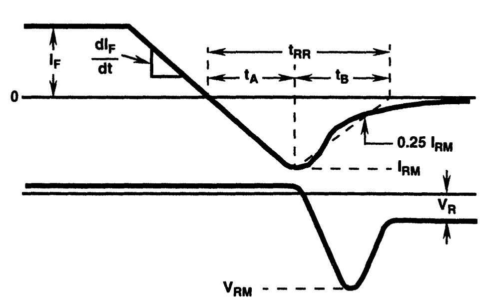


FIGURE 2. t_{RR} TEST CIRCUIT

Typical Performance Curves

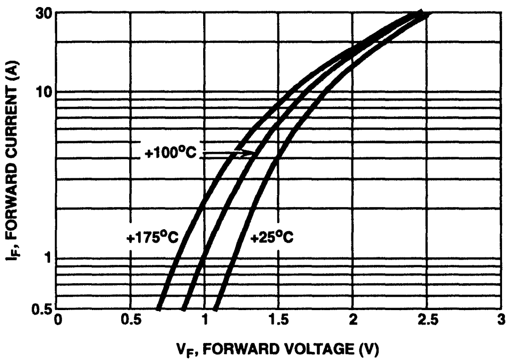


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

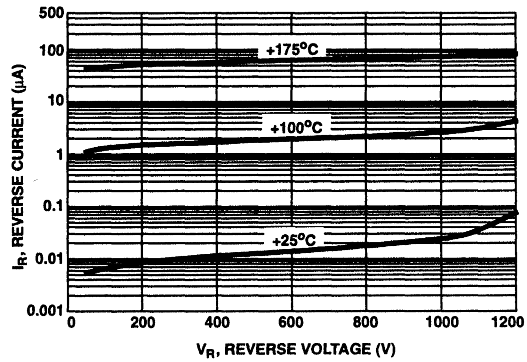


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

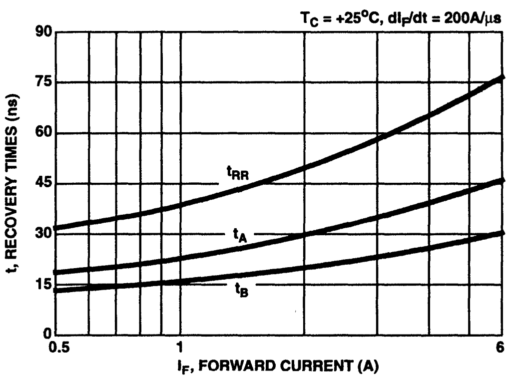


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

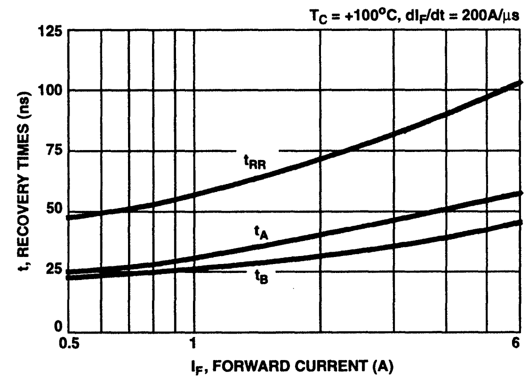


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

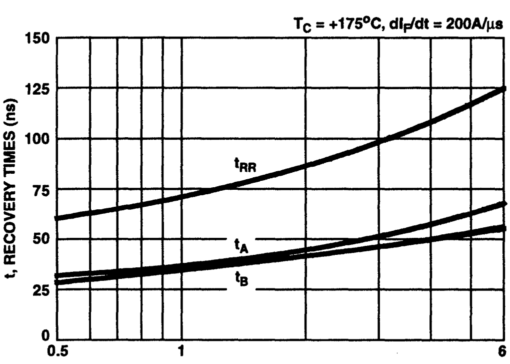


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

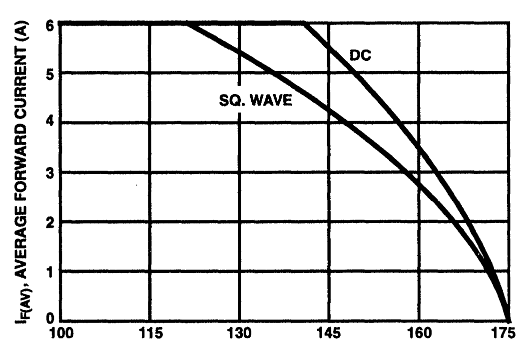


FIGURE 8. CURRENT DERATING CURVE

5

ULTRAFAST SINGLE DIODES

Typical Performance Curves (Continued)

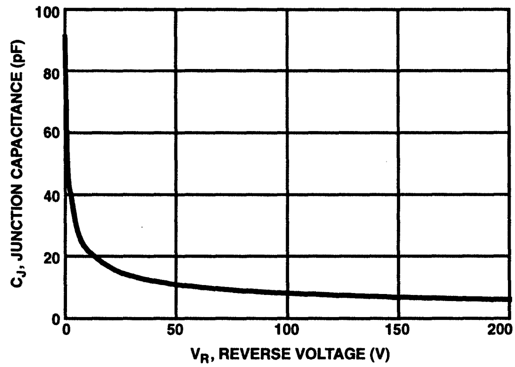


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

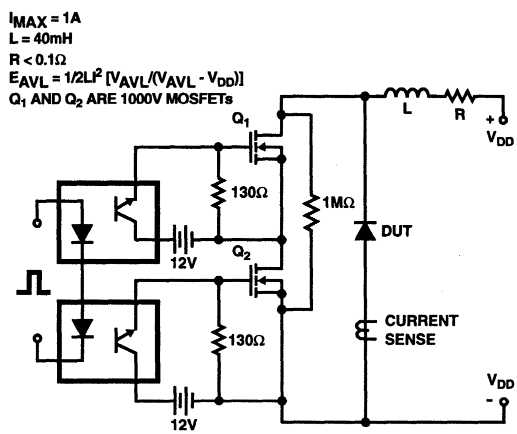


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

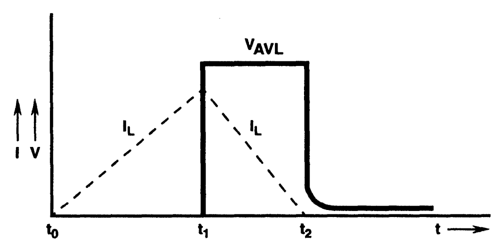


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RURG3010, RURG3015, RURG3020

HARRIS SEMICONDUCTOR

April 1995

30A, 100V - 200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <45ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3010, RURG3015 and RURG3020 are ultrafast diodes with soft recovery characteristics (t_{RR} < 45ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

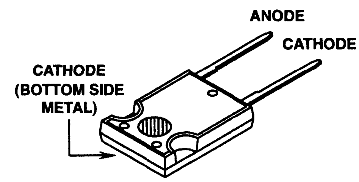
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3010	TO-247	RURG3010
RURG3015	TO-247	RURG3015
RURG3020	TO-247	RURG3020

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG3010	RURG3015	RURG3020	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	100	150	200	V
Working Peak Reverse Voltage	V_{RWM}	100	150	200	V
DC Blocking Voltage	V_R	100	150	200	V
Average Rectified Forward Current (T_C = +145°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number 3277.2

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURG3010			RURG3015			RURG3020			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A, T_C = +25^oC$	-	-	1.0	-	-	1.0	-	-	1.0	V
V_F	$I_F = 30A, T_C = +150^oC$	-	-	0.85	-	-	0.85	-	-	0.85	V
I_R	$V_R = 100V, T_C = +25^oC$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 150V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 200V, T_C = +25^oC$	-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 100V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 150V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 200V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	μA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	45	-	-	45	-	-	45	ns
	$I_F = 30A$, $dI_F/dt = 100A/\mu s$	-	-	50	-	-	50	-	-	50	ns
t_A	$I_F = 30A$, $dI_F/dt= 100A/\mu s$	-	20	-	-	20	-	-	20	-	ns
t_B	$I_F = 30A$, $dI_F/dt = 100A/\mu s$	-	15	-	-	15	-	-	15	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

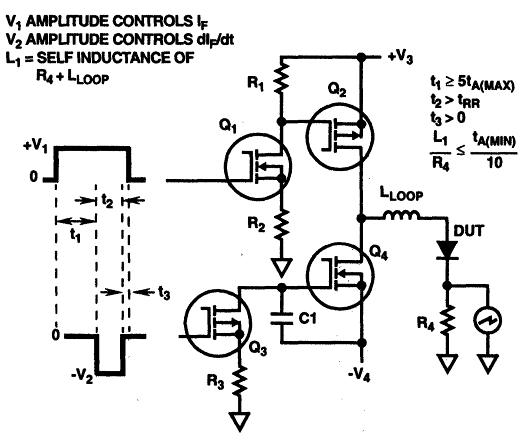


FIGURE 1. t_{RR} TEST CIRCUIT

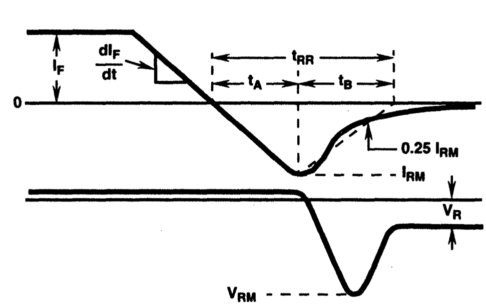


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

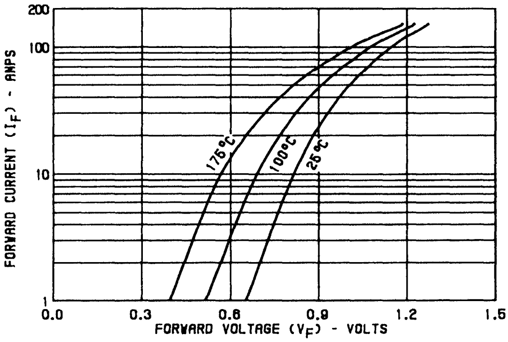


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

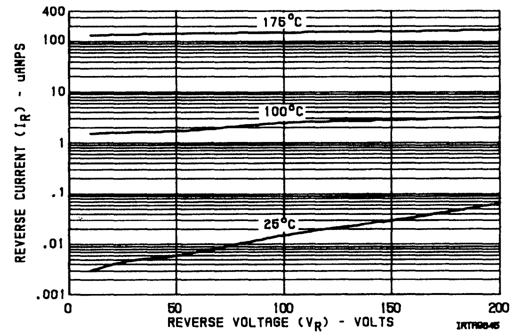


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

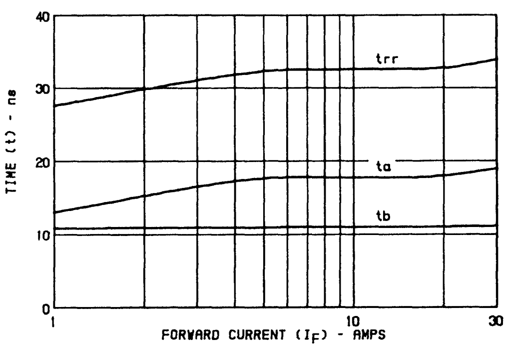


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

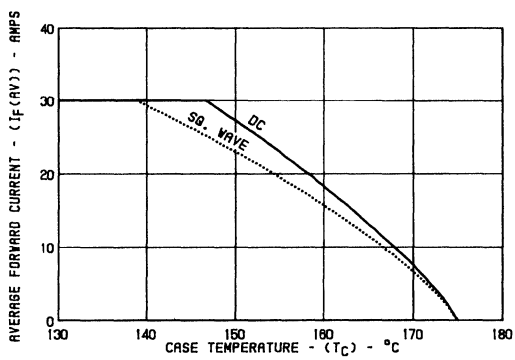


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

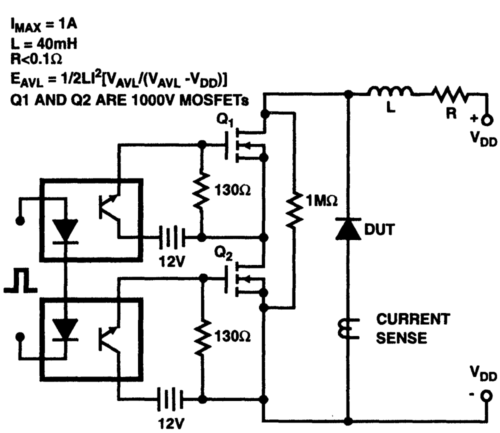


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

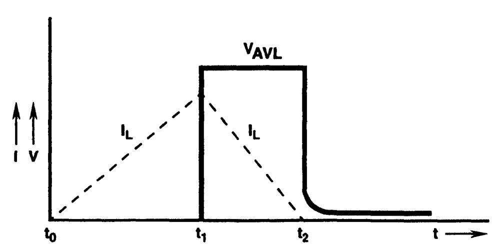


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG3040, RURG3050, RURG3060

April 1995

30A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <55ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3040, RURG3050 and RURG3060 are ultrafast diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

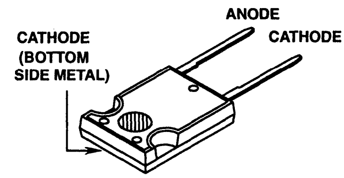
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3040	TO-247	RURG3040
RURG3050	TO-247	RURG3050
RURG3060	TO-247	RURG3060

NOTE: When ordering, use the entire part number

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG3040	RURG3050	RURG3060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +145°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURG3040			RURG3050			RURG3060			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	1.5	-	-	1.5	-	-	1.5	V
V_F	I_F = 30A, T_C = +150°C	-	-	1.3	-	-	1.3	-	-	1.3	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = +150°C	-	-	1	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	1	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	55	-	-	55	-	-	55	ns
	I_F = 30A, dI_F/dt = 100A/µs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 30A, dI_F/dt= 100A/µs	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

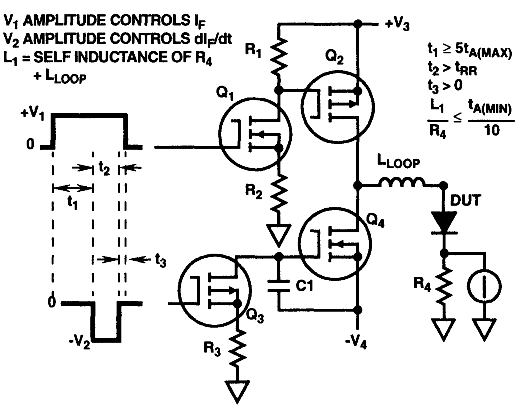


FIGURE 1. t_{RR} TEST CIRCUIT

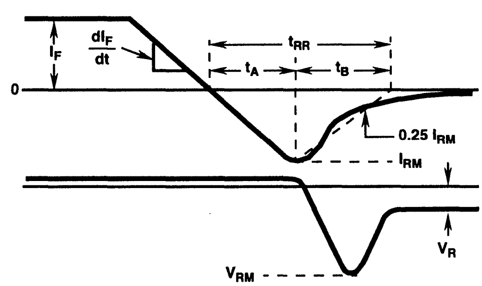


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

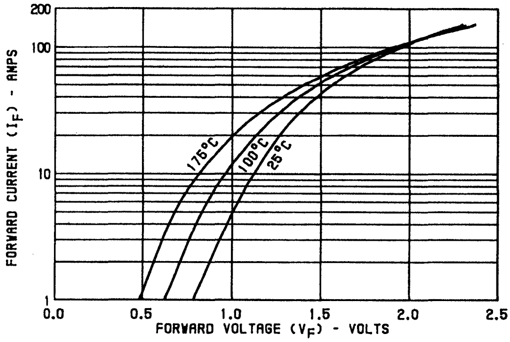


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

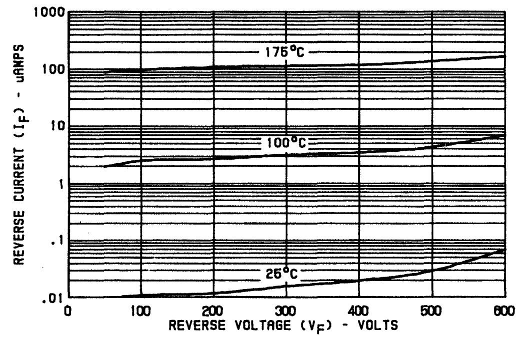


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

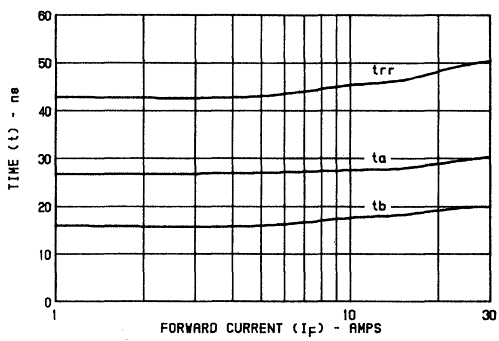


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

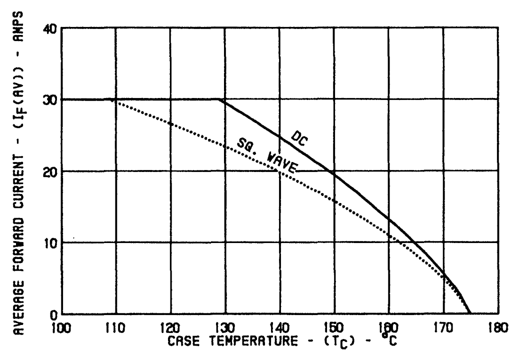


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

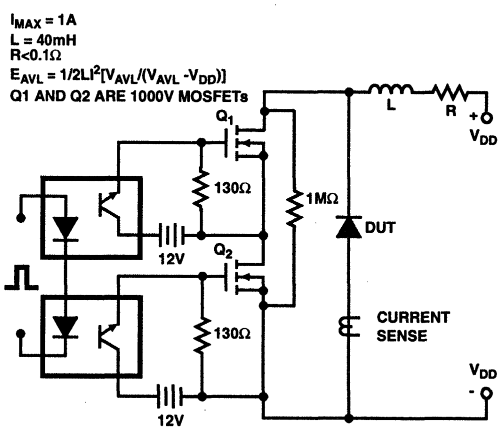


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

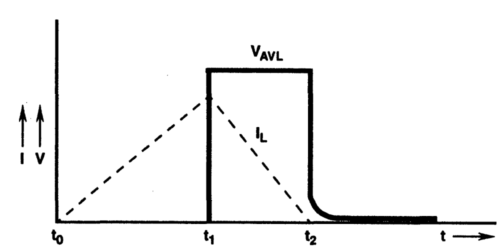


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG3070, RURG3080, RURG3090, RURG30100

April 1995

30A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery....................<110ns
- Operating Temperature........................+175°C
- Reverse Voltage Up To..........................1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3070, RURG3080, RURG3090 and RURG30100 (TA9904) are ultrafast diodes with soft recovery characteristics (t_{RR} < 110ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

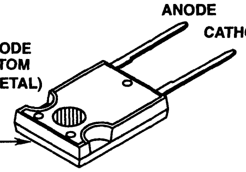
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3070	TO-247	RURG3070
RURG3080	TO-247	RURG3080
RURG3090	TO-247	RURG3090
RURG30100	TO-247	RURG30100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG3070	RURG3080	RURG3090	RURG30100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +117°C)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	60	60	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	300	300	300	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Avalanche Energy	E_{AVL}	30	30	30	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURG3070			RURG3080			RURG3090			RURG30100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	1.8	-	-	1.8	-	-	1.8	-	-	1.8	V
V_F	I_F = 30A, T_C = +150°C	-	-	1.6	-	-	1.6	-	-	1.6	-	-	1.6	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R =800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	1	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	1	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	1	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	110	-	-	110	-	-	110	-	-	110	ns
	I_F = 30A, dI_F/dt = 100A/μs	-	-	150	-	-	150	-	-	150	-	-	150	ns
t_A	I_F = 30A, dI_F/dt = 100A/μs	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/μs	-	45	-	-	45	-	-	45	-	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

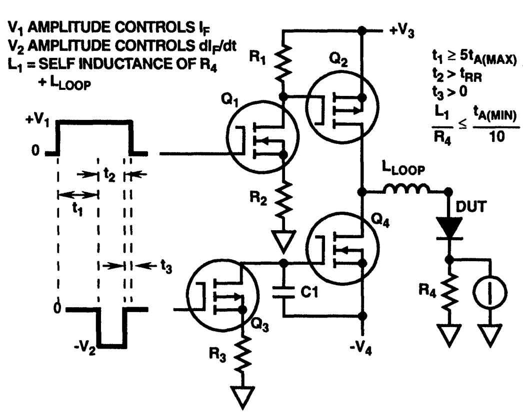


FIGURE 1. t_{RR} TEST CIRCUIT

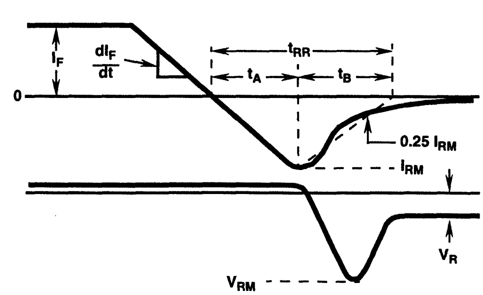


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

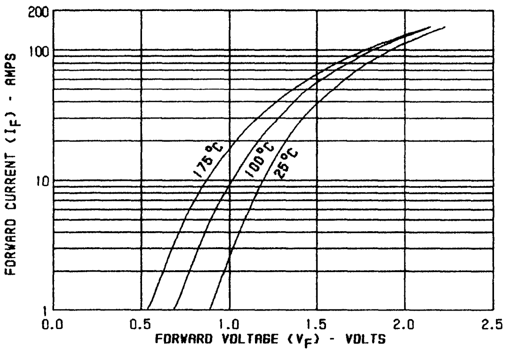


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

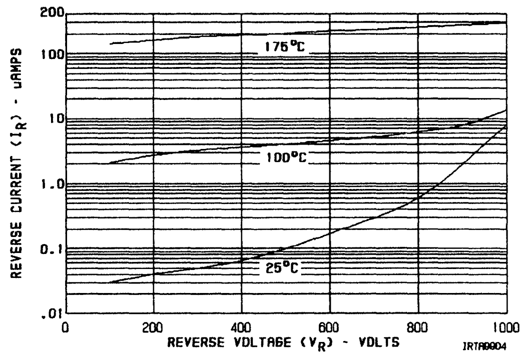


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

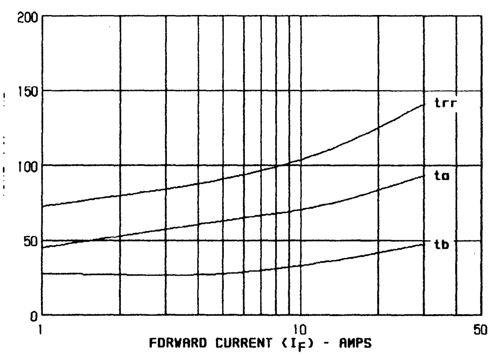


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

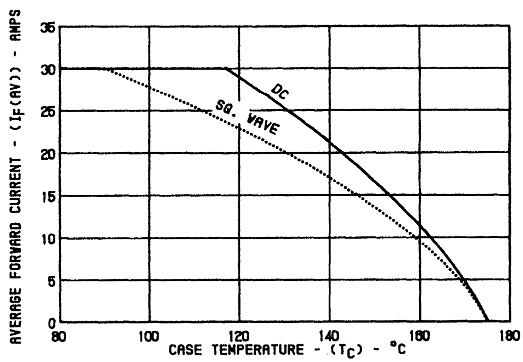


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

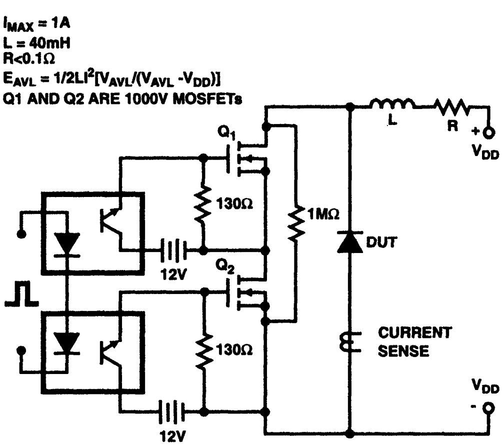


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

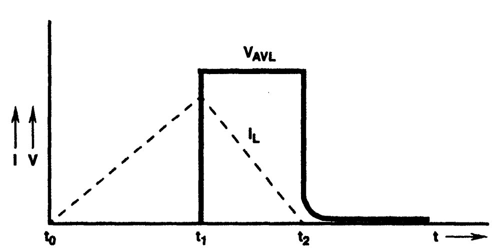


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

5
ULTRAFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

RURG30120

April 1995

30A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . <110ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURG30120 (49031) is an ultrafast diode with soft recovery characteristic (t_{RR} < 110ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

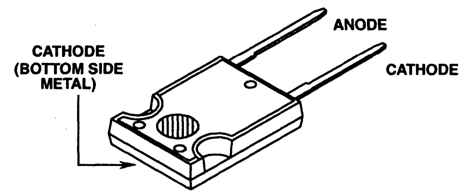
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG30120	TO-247	RURG30120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG30120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +110°C)	$I_{F(AV)}$	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	A
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3399.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	2.1	V
V_F	I_F = 30A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	500	µA
I_R	V_R = 1200V, T_C = +150°C	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	110	ns
	I_F = 30A, dI_F/dt = 100A/µs	-	-	150	ns
t_A	I_F = 30A, dI_F/dt= 100A/µs	-	90	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

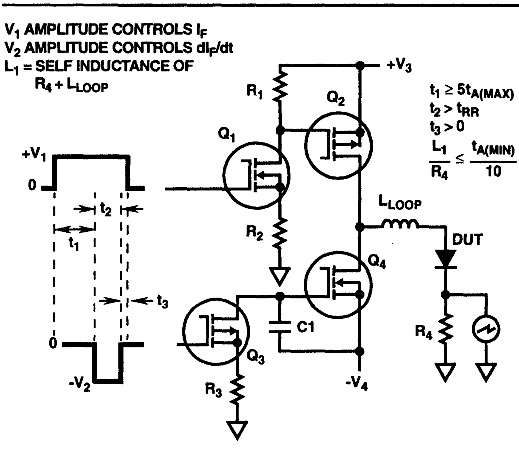


FIGURE 1. t_{RR} TEST CIRCUIT

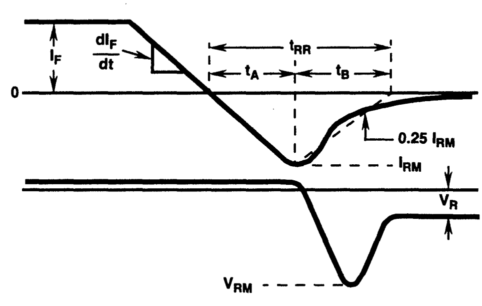


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

5

ULTRAFAST SINGLE DIODES

Typical Performance Curves

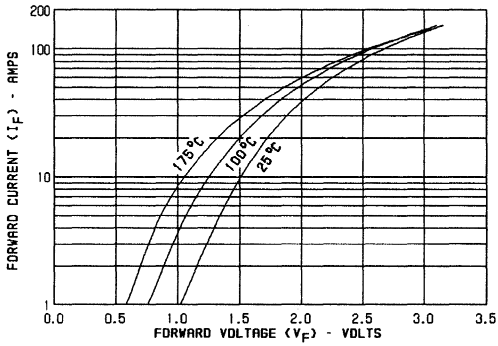


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

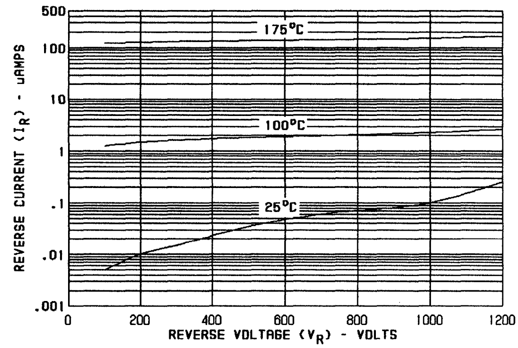


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

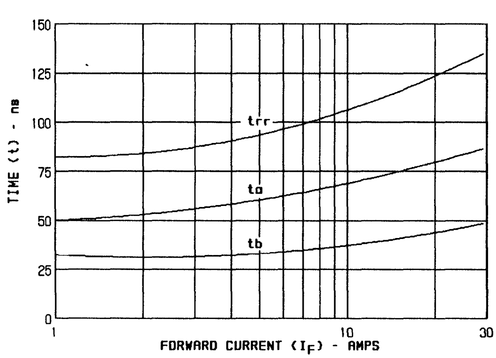


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

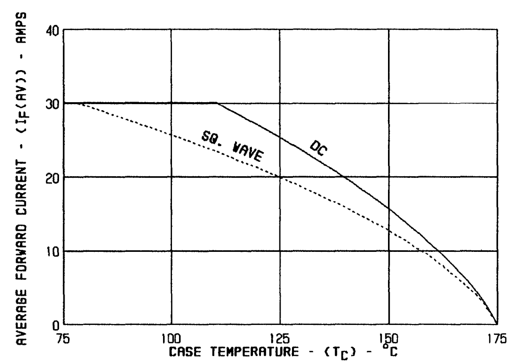


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

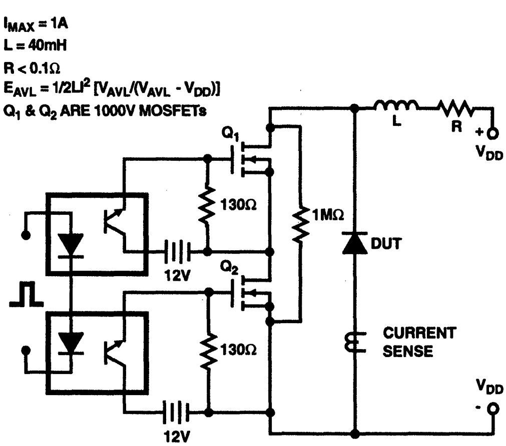


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

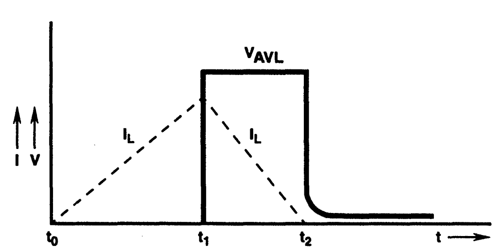


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG5040, RURG5050, RURG5060

April 1995

50A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery..................... <65ns
- Operating Temperature.......................... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG5040, RURG5050 and RURG5060 (TA9909) are ultrafast diodes with soft recovery characteristics (t_{RR} < 65ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

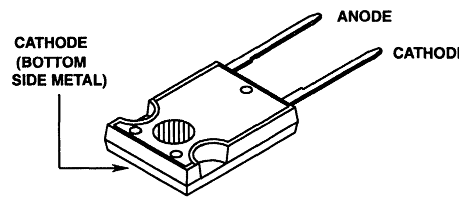
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG5040	TO-247	RURG5040
RURG5050	TO-247	RURG5050
RURG5060	TO-247	RURG5060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG5040	RURG5050	RURG5060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +102°C)	$I_{F(AV)}$	50	50	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	100	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	A
Maximum Power Dissipation	P_D	150	150	150	W
Avalanche Energy	E_{AVL}	40	40	40	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3211.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURG5040			RURG5050			RURG5060			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 50A, T_C = +25°C	-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	I_F = 50A, T_C = +150°C	-	-	1.4	-	-	1.4	-	-	1.4	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = 150°C	-	-	1.5	-	-	-	-	-	-	mA
	V_R = 500V, T_C = 150°C	-	-	-	-	-	1.5	-	-	-	mA
	V_R = 600V, T_C = 150°C	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	65	-	-	65	-	-	65	ns
	I_F = 50A, dI_F/dt = 100A/µs	-	-	75	-	-	75	-	-	75	ns
t_A	I_F = 50A, dI_F/dt= 100A/µs	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 50A, dI_F/dt = 100A/µs	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1	-	-	1	-	-	1	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

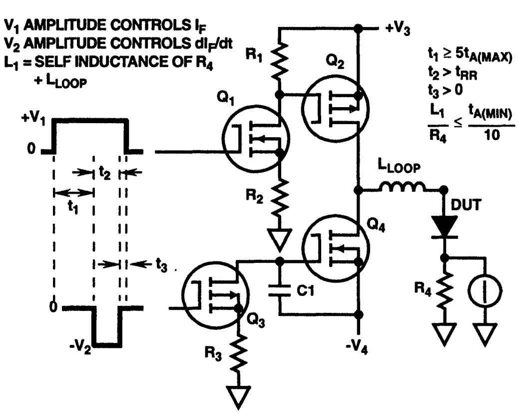


FIGURE 1. t_{RR} TEST CIRCUIT

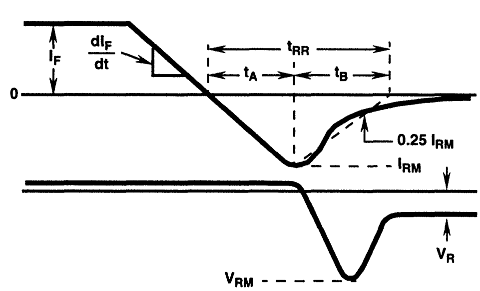


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

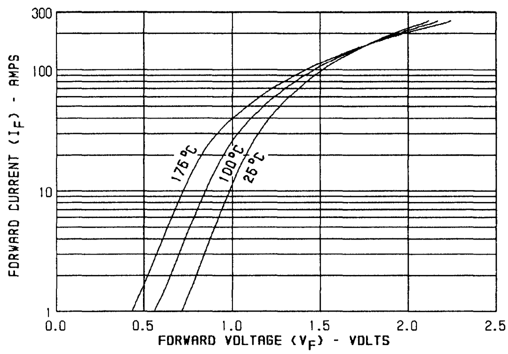


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

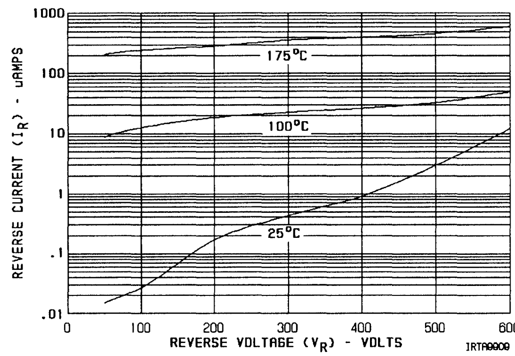


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

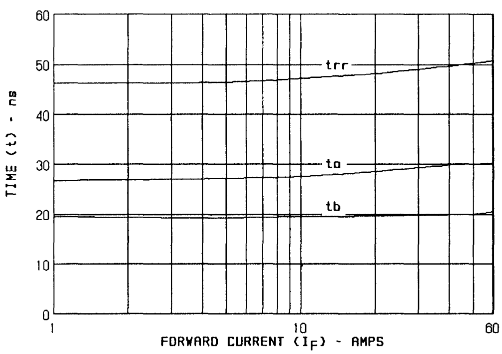


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

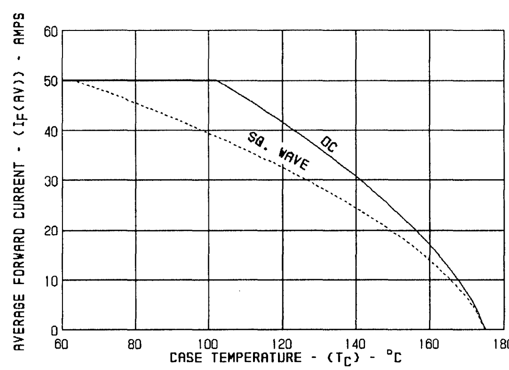


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

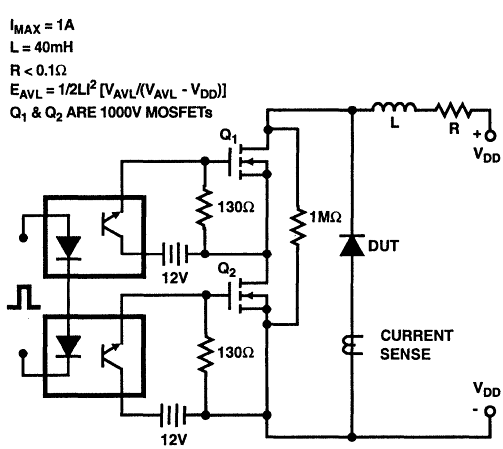


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

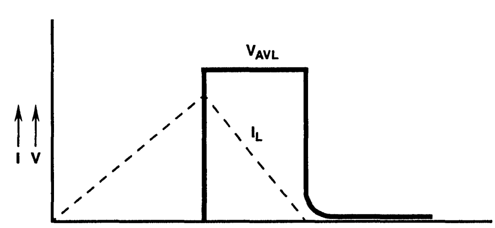


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

5
ULTRAFAST SINGLE DIODES

RURG5070, RURG5080, RURG5090, RURG50100

HARRIS SEMICONDUCTOR

April 1995

50A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <125ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG5070, RURG5080, RURG5090 and RURG50100 are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

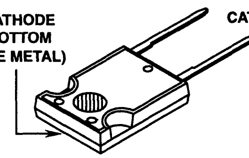
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG5070	TO-247	RURG5070
RURG5080	TO-247	RURG5080
RURG5090	TO-247	RURG5090
RURG50100	TO-247	RURG50100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG5070	RURG5080	RURG5090	RURG50100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +85°C)	$I_{F(AV)}$	50	50	50	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	100	100	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	500	A
Maximum Power Dissipation	P_D	150	150	150	150	W
Avalanche Energy	E_{AVL}	40	40	40	40	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURG5070			RURG5080			RURG5090			RURG50100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 50A, T_C = +25^oC$	-	-	1.9	-	-	1.9	-	-	1.9	-	-	1.9	V
V_F	$I_F = 50A, T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 700V, T_C = +25^oC$	-	-	500	-	-	-	-	-	-	-	-	-	µA
	$V_R = 800V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	-	-	-	µA
	$V_R = 900V, T_C = +25^oC$	-	-	-	-	-	-	-	-	500	-	-	-	µA
	$V_R = 1000V, T_C = +25^oC$	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 700V, T_C = +150^oC$	-	-	1.5	-	-	-	-	-	-	-	-	-	mA
	$V_R = 800V, T_C = +150^oC$	-	-	-	-	-	1.5	-	-	-	-	-	-	mA
	$V_R = 900V, T_C = +150^oC$	-	-	-	-	-	-	-	-	1.5	-	-	-	mA
	$V_R = 1000V, T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	125	-	-	125	-	-	125	-	-	125	ns
	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	-	200	-	-	200	-	-	200	-	-	200	ns
t_A	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	110	-	-	110	-	-	110	-	-	110	-	ns
t_B	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	65	-	-	65	-	-	65	-	-	65	-	ns
$R_{\theta JC}$		-	-	1.0	-	-	1.0	-	-	1.0	-	-	1.0	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

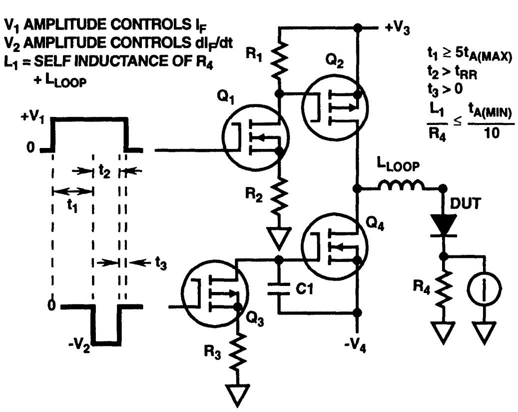


FIGURE 1. t_{RR} TEST CIRCUIT

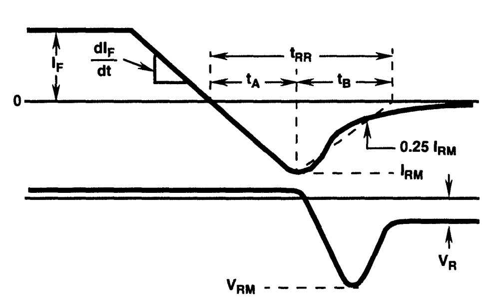


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

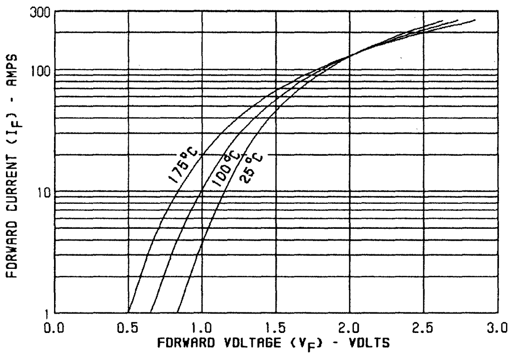


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

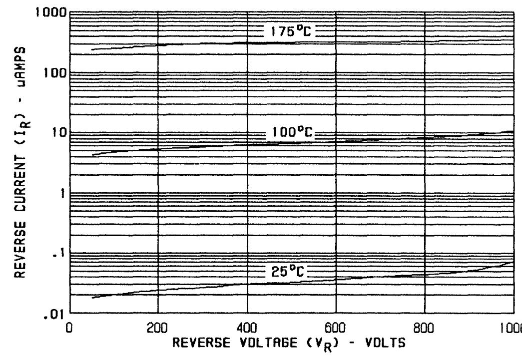


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

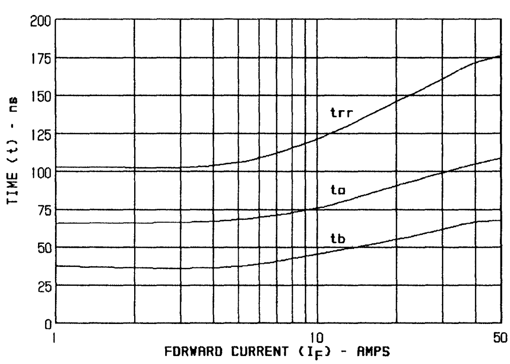


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

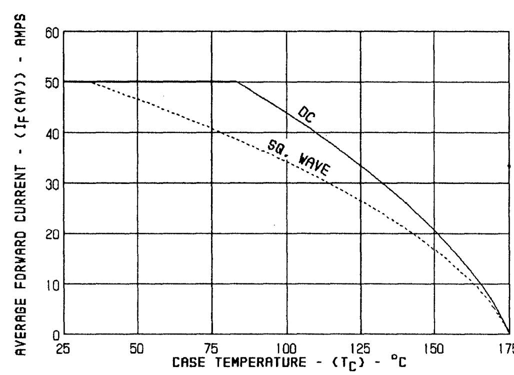


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 & Q_2 ARE 1000V MOSFETs

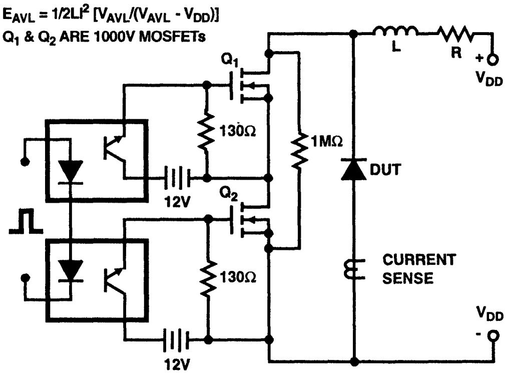


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

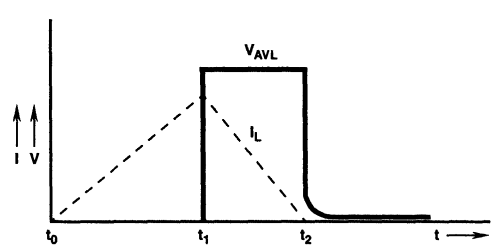


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG50120

April 1995

50A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery................<125ns
- Operating Temperature....................+175°C
- Reverse Voltage..........................1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURG50120 (TA49099) are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

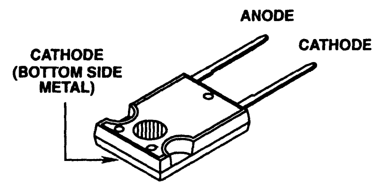
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG50120	TO-247	RURG50120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG50120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +85°C)	$I_{F(AV)}$	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	170	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3740.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS MIN	TYP	MAX	UNITS
V_F	$I_F = 50A$, $T_C = +25^oC$	-	-	2.1	V
	$I_F = 50A$, $T_C = +150^oC$	-	-	1.9	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	500	µA
	$V_R = 1200V$, $T_C = +150^oC$	-	-	2.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	125	ns
	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	-	200	ns
t_A	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	95	-	ns
t_B	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	70	-	ns
Q_{RR}	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	800	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	160	-	pF
$R_{\theta JC}$		-	-	0.9	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

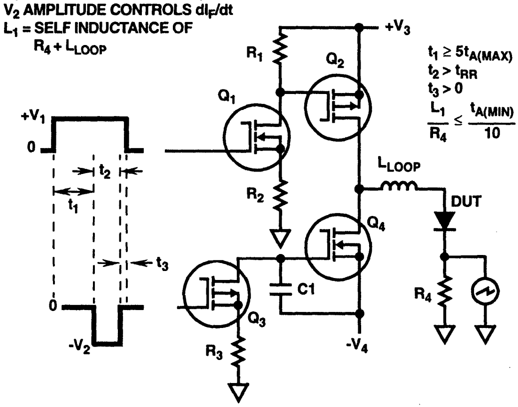


FIGURE 1. t_{RR} TEST CIRCUIT

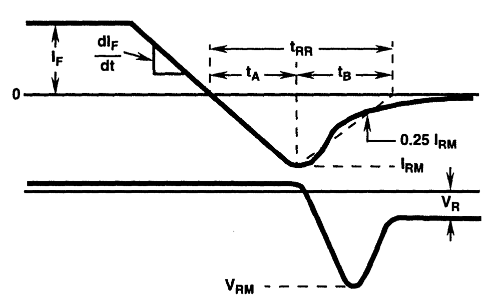


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

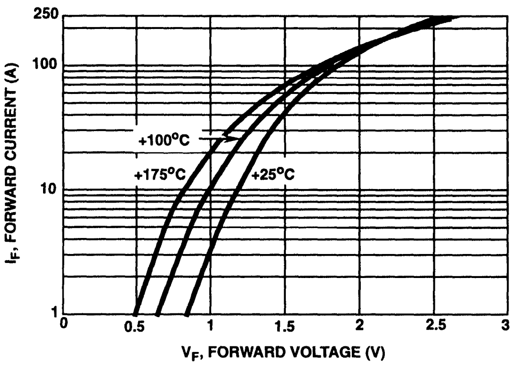


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

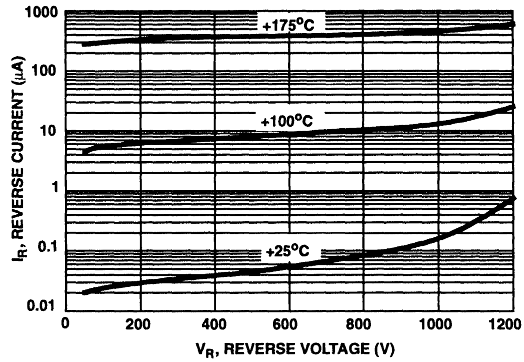


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

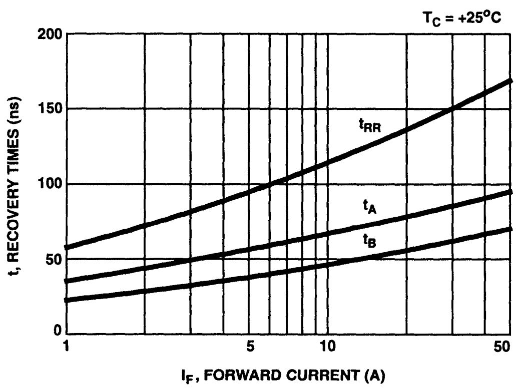


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

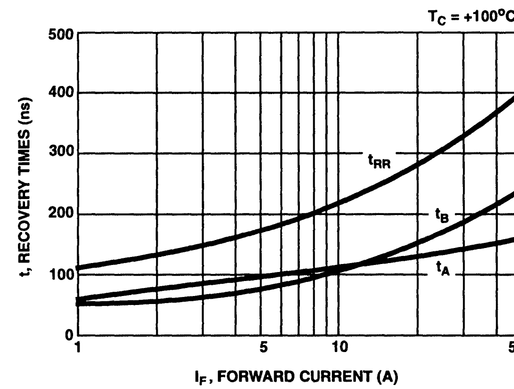


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

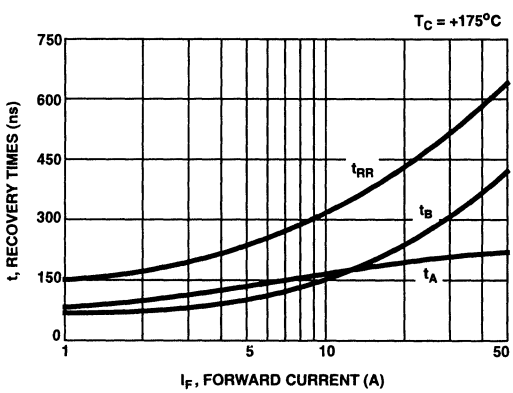


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

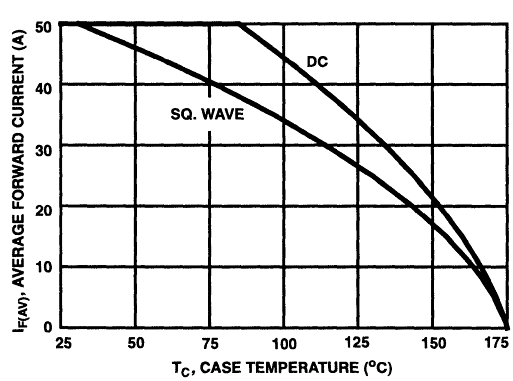


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

5

ULTRAFAST SINGLE DIODES

Typical Performance Curves (Continued)

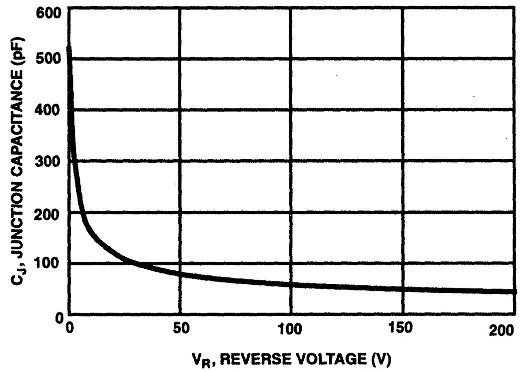


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

$I_{MAX} = 1A$
$L = 40mH$
$R < 0.1\Omega$
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

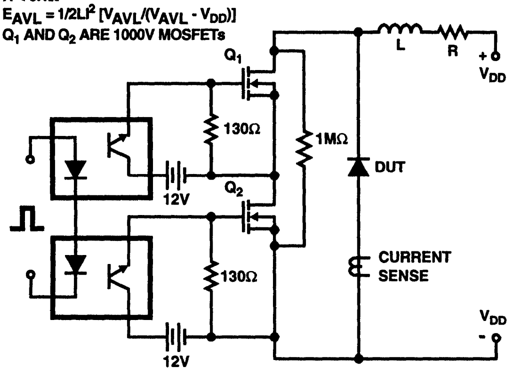


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

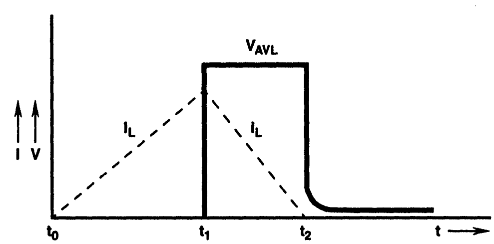


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG75120

April 1995

75A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . <125ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURG75120 (TA49032) is an ultrafast diode with soft recovery characteristics (t_{RR} < 125ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

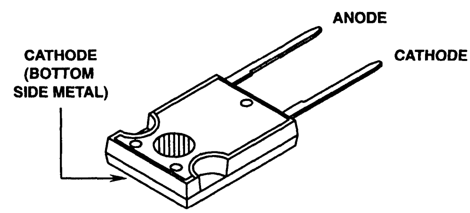
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG75120	TO-247	RURG75120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG75120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +54.75°C)	$I_{F(AV)}$	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	190	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3412.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 75A		-	-	2.1	V
V_F	I_F = 75A	T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V		-	-	500	µA
I_R	V_R = 1200V	T_C = +150°C	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs		-	-	125	ns
t_{RR}	I_F = 75A, dI_F/dt = 100A/µs		-	-	200	ns
t_A	I_F = 75A, dI_F/dt = 100A/µs		-	90	-	ns
t_B	I_F = 75A, dI_F/dt = 100A/µs		-	65	-	ns
$R_{\theta JC}$			-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

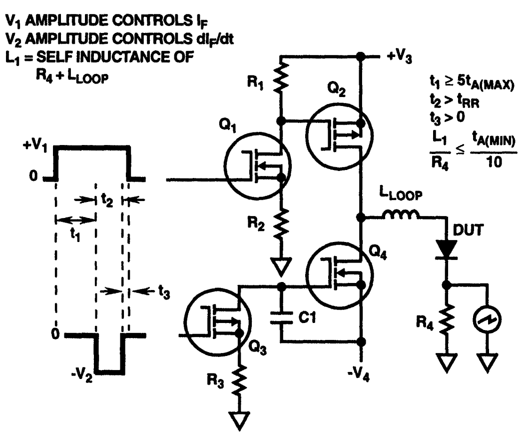


FIGURE 1. t_{RR} TEST CIRCUIT

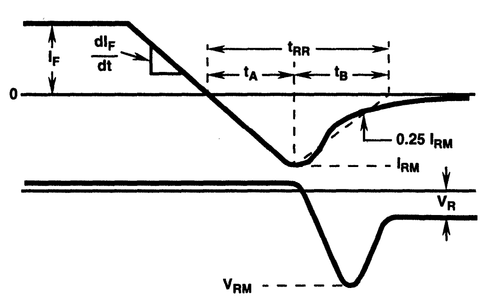


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

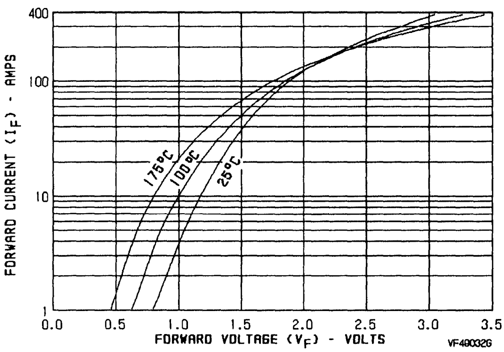


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

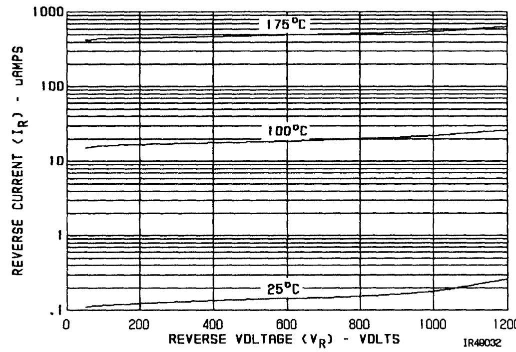


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

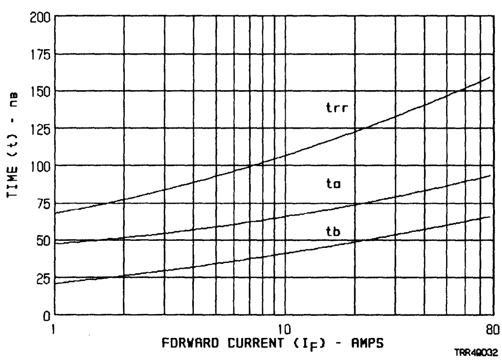


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

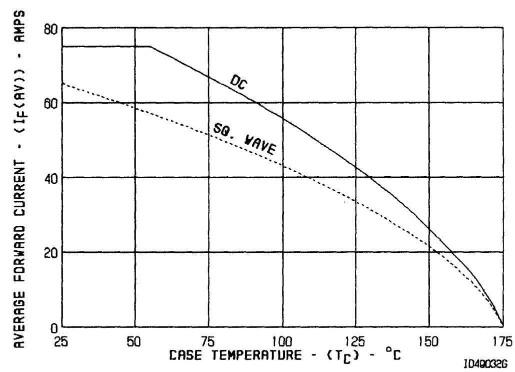


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

$I_{MAX} = 1A$
$L = 40mH$
$R < 0.1\Omega$
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

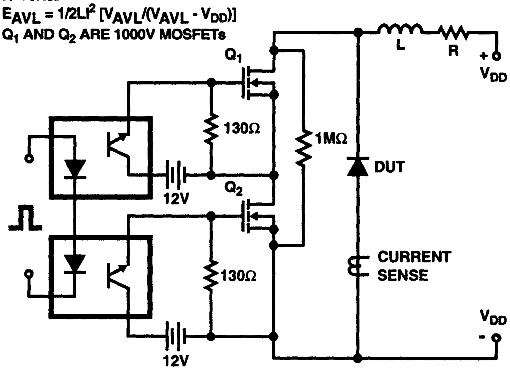


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

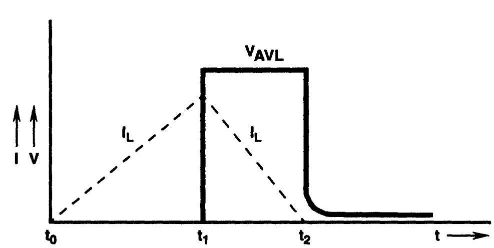


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

5
ULTRAFAST SINGLE DIODES

RURG8040, RURG8050, RURG8060

HARRIS SEMICONDUCTOR

April 1995

80A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <75ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG8040, RURG8050 and RURG8060 (TA9886) are ultrafast diodes with soft recovery characteristics (t_{RR} < 75ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

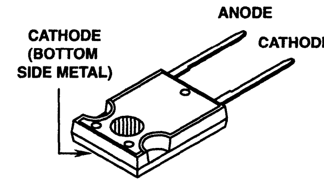
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG8040	TO-247	RURG8040
RURG8050	TO-247	RURG8050
RURG8060	TO-247	RURG8060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG8040	RURG8050	RURG8060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +72°C)	$I_{F(AV)}$	80	80	80	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	160	160	160	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	800	800	800	A
Maximum Power Dissipation	P_D	180	180	180	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3388.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURG8040			RURG8050			RURG8060			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 80A, T_C = +25°C	-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	I_F = 80A, T_C = +150°C	-	-	1.4	-	-	1.4	-	-	1.4	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 400V, T_C = +150°C	-	-	2.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	2.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	75	-	-	75	-	-	75	ns
	I_F = 80A, dI_F/dt = 100A/μs	-	-	85	-	-	85	-	-	85	ns
t_A	I_F = 80A, dI_F/dt= 100A/μs	-	40	-	-	40	-	-	40	-	ns
t_B	I_F = 80A, dI_F/dt = 100A/μs	-	25	-	-	25	-	-	25	-	ns
$R_{\theta JC}$		-	-	0.83	-	-	0.83	-	-	0.83	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

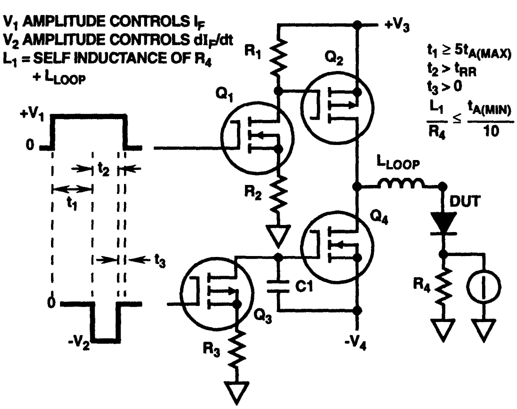


FIGURE 1. t_{RR} TEST CIRCUIT

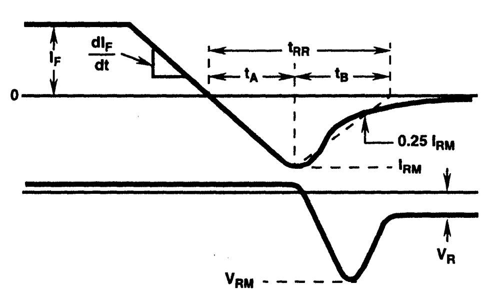


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

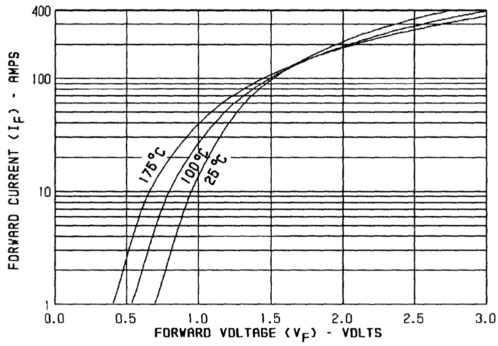


FIGURE 3. TYPICAL FORWARD CURRENT vs. FORWARD VOLTAGE DROP

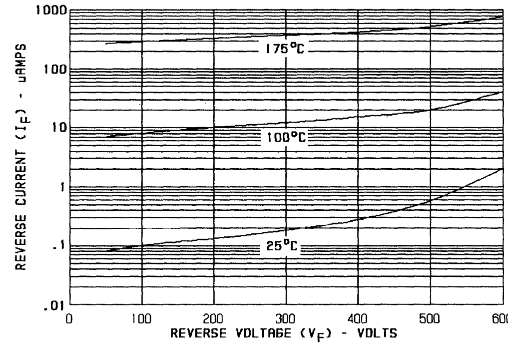


FIGURE 4. TYPICAL REVERSE CURRENT vs. VOLTAGE

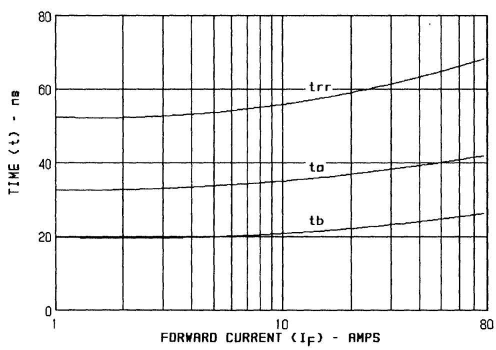


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs. FORWARD CURRENT

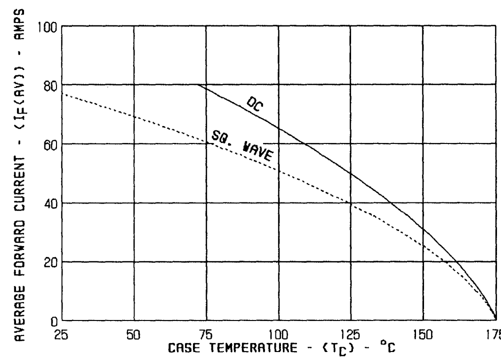


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

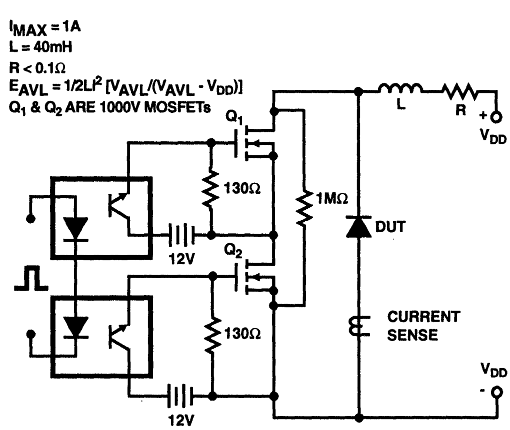


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

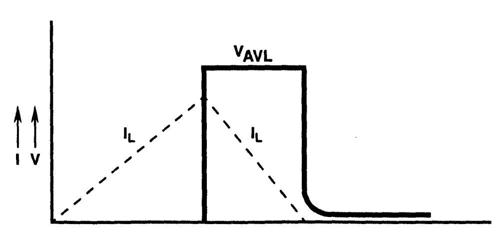


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG8070, RURG8080, RURG8090, RURG80100

April 1995

80A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <125ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG8070, RURG8080, RURG8090 and RURG80100 are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

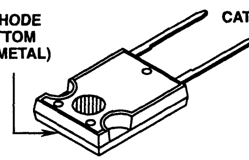
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG8070	TO-247	RURG8070
RURG8080	TO-247	RURG8080
RURG8090	TO-247	RURG8090
RURG80100	TO-247	RURG80100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG8070	RURG8080	RURG8090	RURG80100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +53°C)	$I_{F(AV)}$	80	80	80	80	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	160	160	160	160	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	500	A
Maximum Power Dissipation	P_D	180	180	180	180	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURG8070			RURG8080			RURG8090			RURG80100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 80A, T_C = +25°C	-	-	1.9	-	-	1.9	-	-	1.9	-	-	1.9	V
V_F	I_F = 80A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R =800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	2	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	2	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	2	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	125	-	-	125	-	-	125	-	-	125	ns
	I_F = 80A, dI_F/dt = 100A/μs	-	-	200	-	-	200	-	-	200	-	-	200	ns
t_A	I_F = 80A, dI_F/dt = 100A/μs	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	I_F = 80A, dI_F/dt = 100A/μs	-	65	-	-	65	-	-	65	-	-	65	-	ns
$R_{\theta JC}$		-	-	0.83	-	-	0.83	-	-	0.83	-	-	0.83	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

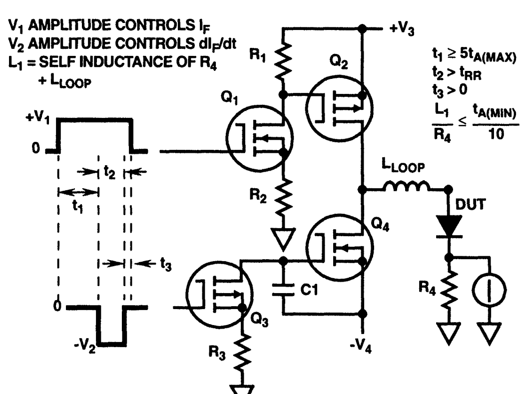


FIGURE 1. t_{RR} TEST CIRCUIT

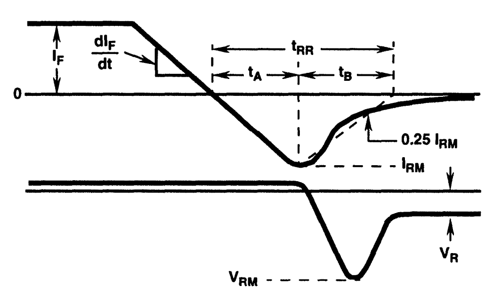


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

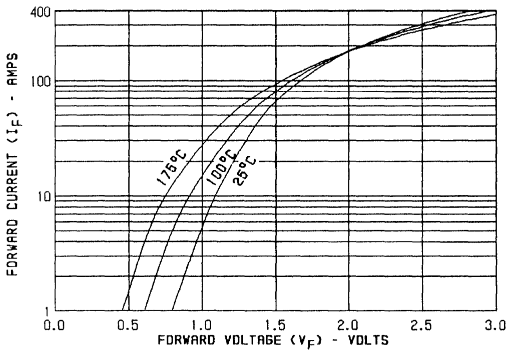


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

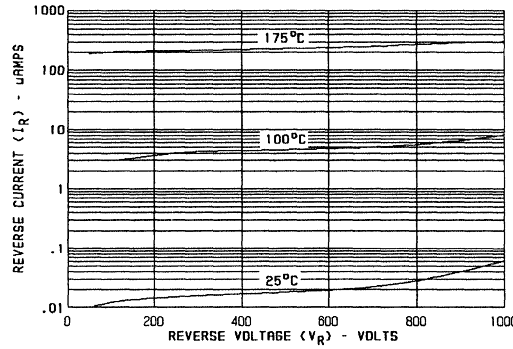


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

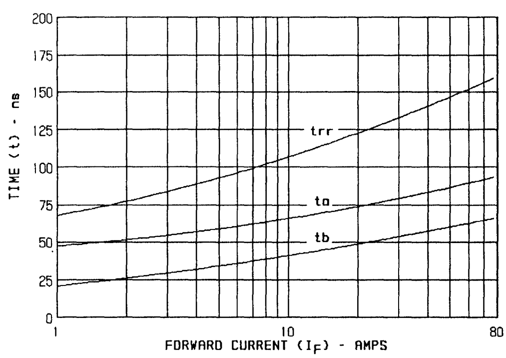


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

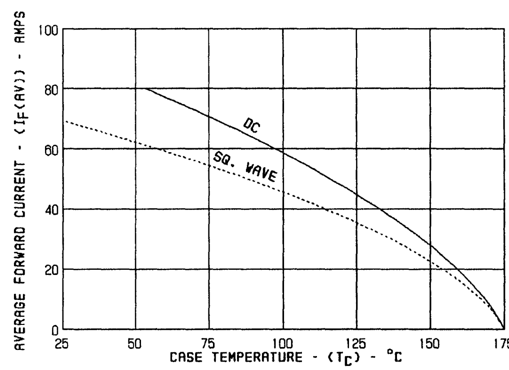


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

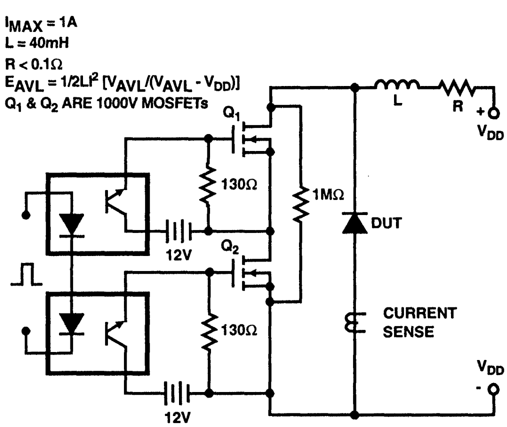


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

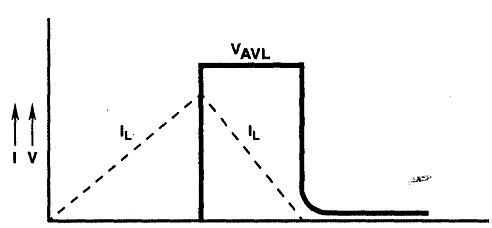


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURP8120

April 1995

8A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery................<100ns
- Operating Temperature....................+175°C
- Reverse Voltage...........................1200V
- Avalanche Energy Rated
- Planar Construction s

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURP8120 (TA49095) are ultrafast diodes with soft recovery characteristics (t_{RR} < 100ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

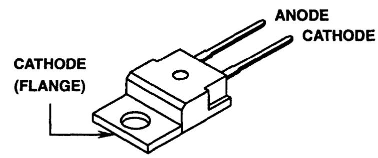
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP8120	TO-220AC	RURP8120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP8120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +144°C)	$I_{F(AV)}$	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	A
Maximum Power Dissipation	P_D	75	W
Avalanche Energy (See Figure 10 and Figure 11)	E_{AVL}	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3661.2**

Electrical Specifications
T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 8A, T_C = +25°C	-	-	2.1	V
	I_F = 8A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	100	ns
	I_F = 8A, dI_F/dt = 100A/µs	-	-	110	ns
t_A	I_F = 8A, dI_F/dt = 100A/µs	-	60	-	ns
t_B	I_F = 8A, dI_F/dt = 100A/µs	-	40	-	ns
Q_{RR}	I_F = 8A, dI_F/dt = 100A/µs	-	380	-	nC
C_J	V_R = 10V, I_F = 0A	-	25	-	pF
$R_{\theta JC}$		-	-	2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
Q_{RR} = Reverse Recovery Charge.
C_J = Junction Capacitance.
pw = pulse width.
D = duty cycle.

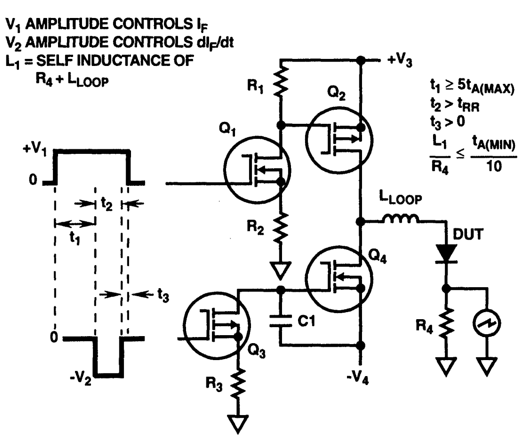


FIGURE 1. t_{RR} TEST CIRCUIT

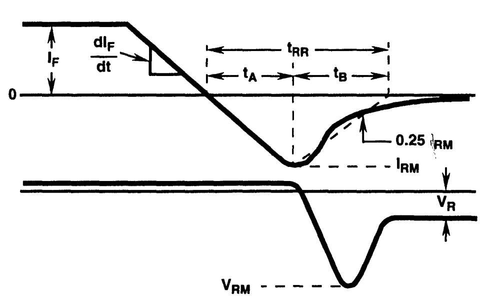


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

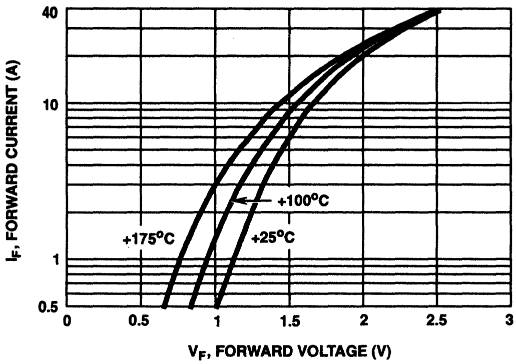


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

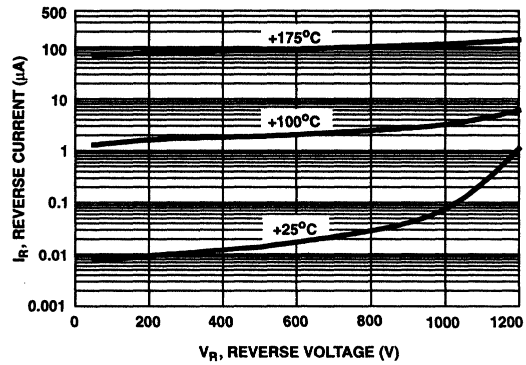


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

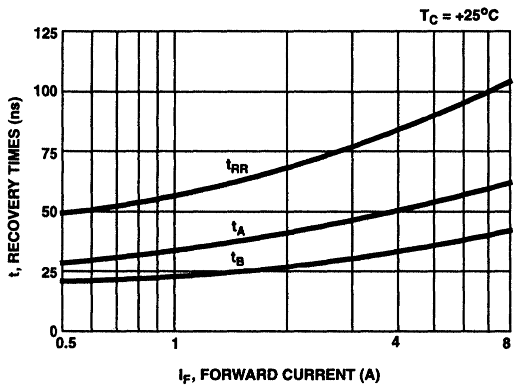


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

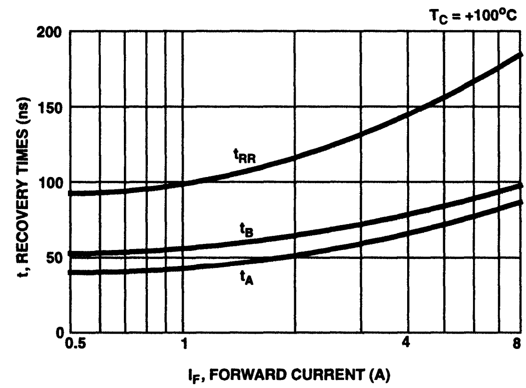


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

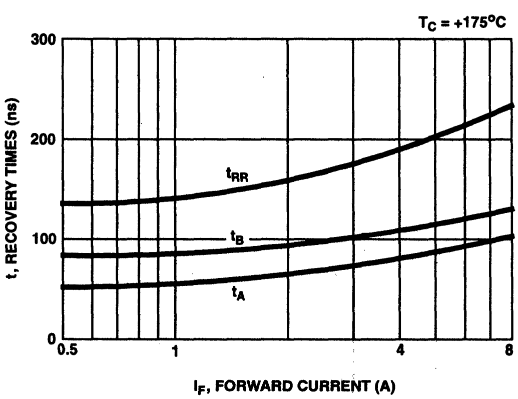


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

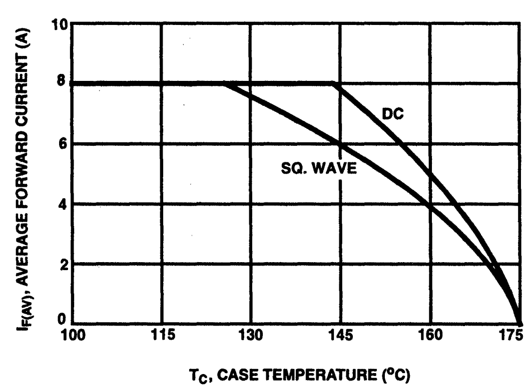


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

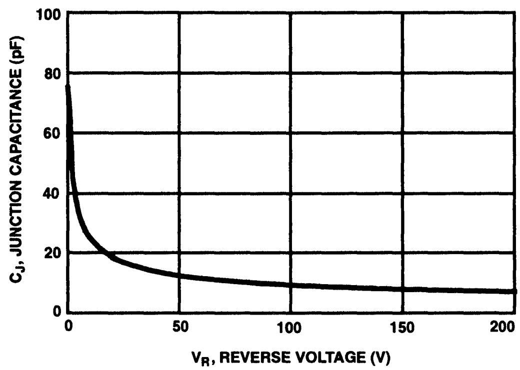


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

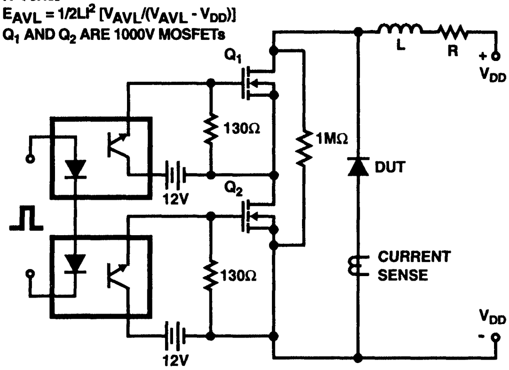


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

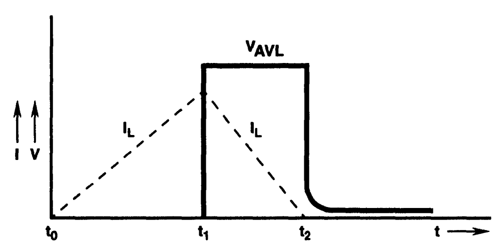


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

5
ULTRAFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

RURP1570, RURP1580, RURP1590, RURP15100

April 1995

15A, 700V - 1000V Ultrafast Diodes

Features

- **Ultrafast with Soft Recovery Characteristic (t_{RR} < 100ns)**
- **+175°C Rated Junction Temperature**
- **Reverse Voltage Up to 1000V**
- **Avalanche Energy Rated**

Applications

- **Switching Power Supply**
- **Power Switching Circuits**
- **General Purpose**

Description

RURP1570, RURP1580, RURP1590, RURP15100 are ultrafast diodes with soft recovery characteristics (t_{RR} < 100ns). They have a low forward voltage drop and are silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as freewheel/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

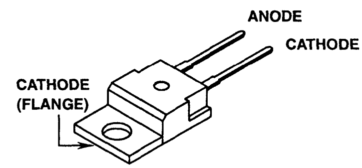
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP1570	TO-220AC	RURP1570
RURP1580	TO-220AC	RURP1580
RURP1590	TO-220AC	RURP1590
RURP15100	TO-220AC	RURP15100

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP1570	RURP1580	RURP1590	RURP15100
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current (Total Device Forward Current At Rated V_R And T_C = +150°C)	$I_{F(AV)}$	15A	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, Square Wave 20kHz)	I_{FRM}	30A	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge Applied At Rated Load Condition Halfwave 1 Phase 60Hz)	I_{FSM}	200A	200A	200A	200A
Maximum Power Dissipation	P_D	100W	100W	100W	100W
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

File Number **2878.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURP1570			RURP1580			RURP1590			RURP15100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	I_F = 15A T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at T_C = +150°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +25°C	V_R = 700V	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	100	-	-	100	-	-	100	-	-	100	ns
	I_F = 15A	-	-	125	-	-	125	-	-	125	-	-	125	ns
t_A	I_F = 15A	-	75	-	-	75	-	-	75	-	-	75	-	ns
t_B	I_F = 15A	-	40	-	-	40	-	-	40	-	-	40	-	ns
$R_{θJC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}		-	-	20	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{θJC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

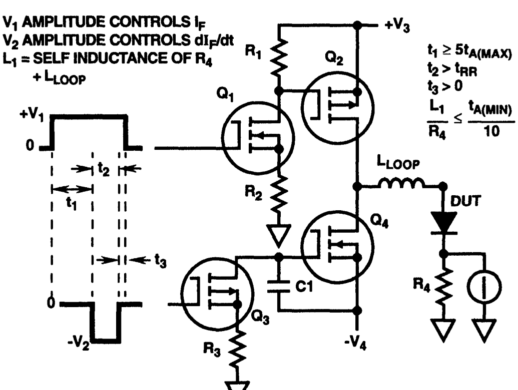


FIGURE 1. t_{RR} TEST CIRCUIT

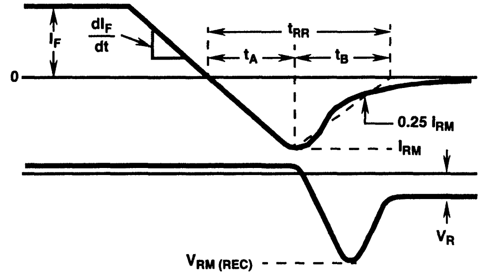


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

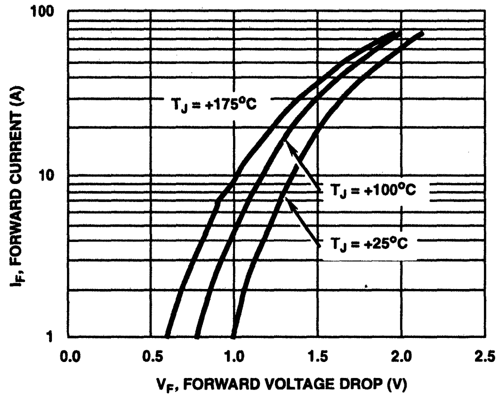


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

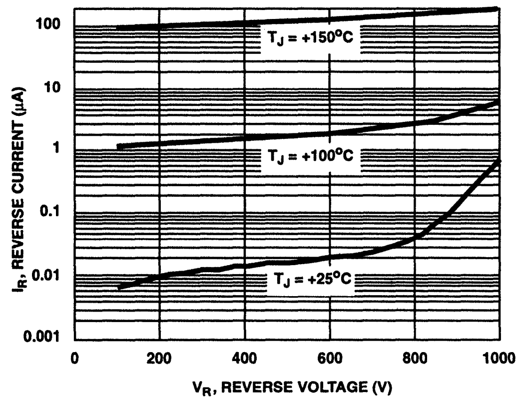


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

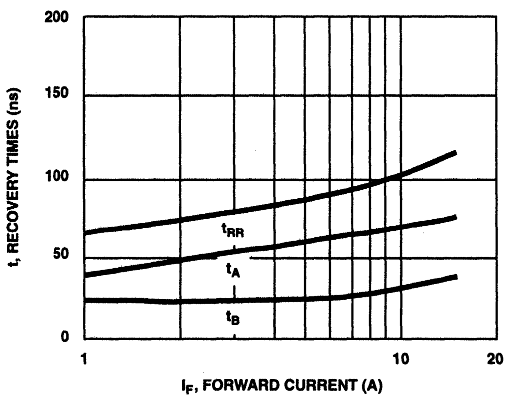


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

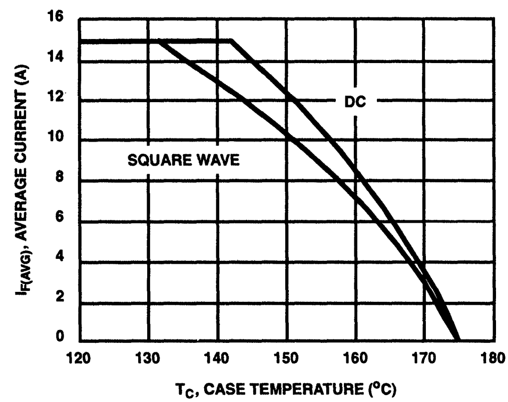


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

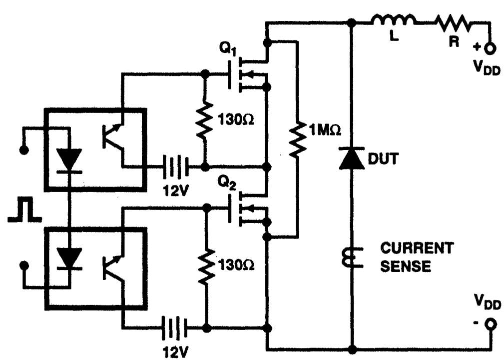


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

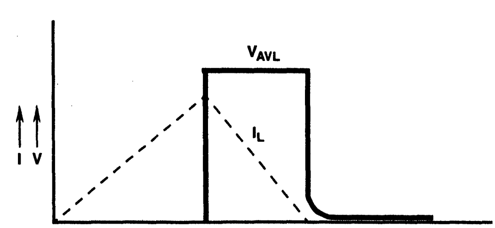


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (1/2) LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$
Q1 AND Q2 ARE 1000V MOSFETs

HARRIS SEMICONDUCTOR

RURP15120

April 1995

15A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . <100ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURP15120 (TA49097) are ultrafast diodes with soft recovery characteristics (t_{RR} < 100ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

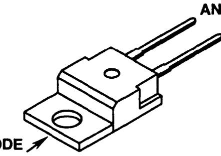
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP15120	TO-220AC	RUR15120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP15120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	A
Maximum Power Dissipation	P_D	100	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 15A, T_C = +25°C	-	-	2.1	V
	I_F = 15A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	100	ns
	I_F = 15A, dI_F/dt = 100A/µs	-	-	130	ns
t_A	I_F = 15A, dI_F/dt = 100A/µs	-	65	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/µs	-	40	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/µs	-	400	-	nC
C_J	V_R = 10V, I_F = 0A	-	56	-	pF
$R_{\theta JC}$		-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
Q_{RR} = Reverse recovery charge.
C_J = Junction capacitance.
pw = pulse width.
D = duty cycle.

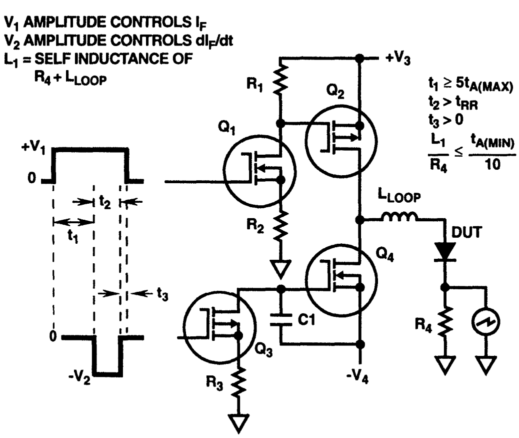


FIGURE 1. t_{RR} TEST CIRCUIT

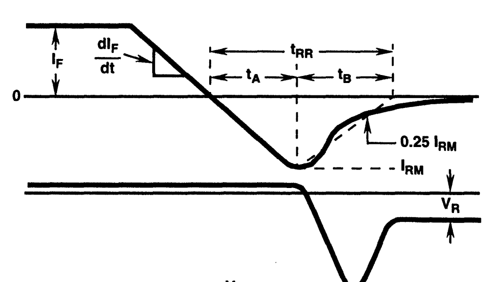


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

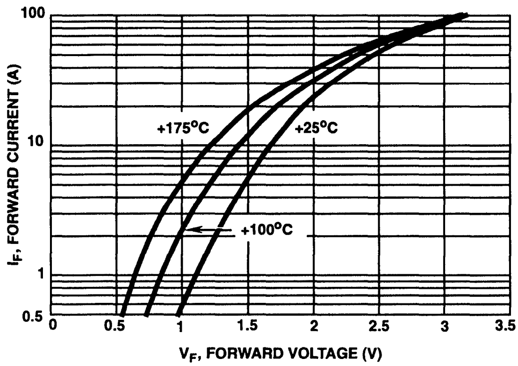


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

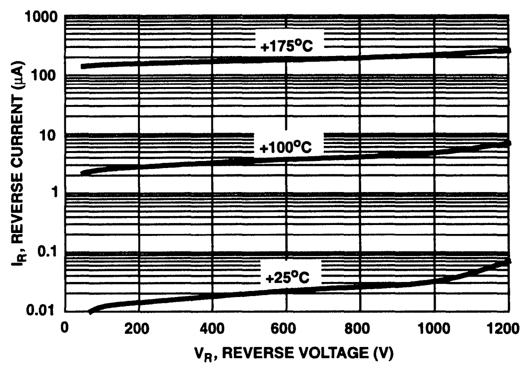


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

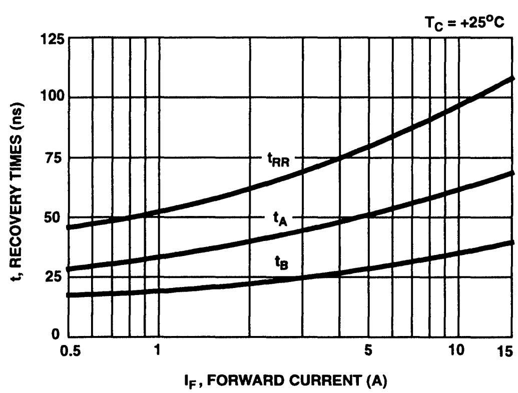


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

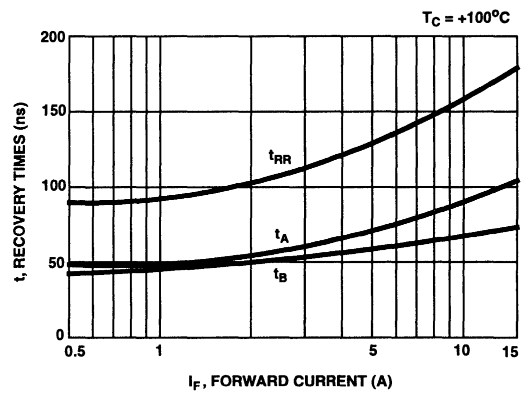


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

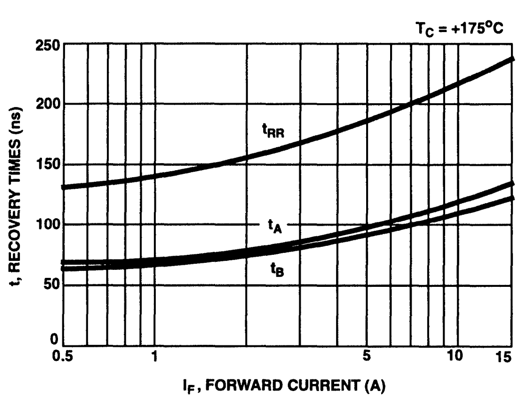


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

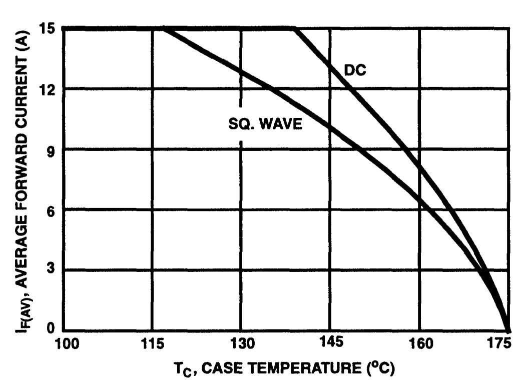


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

5

ULTRAFAST SINGLE DIODES

Typical Performance Curves (Continued)

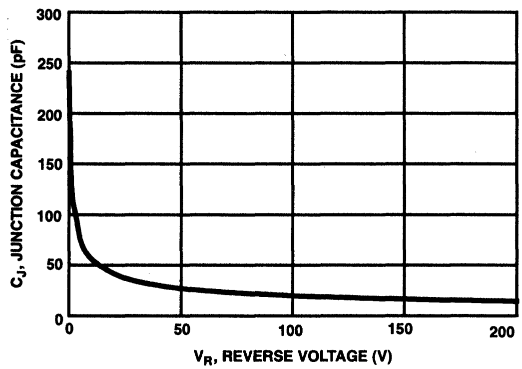


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

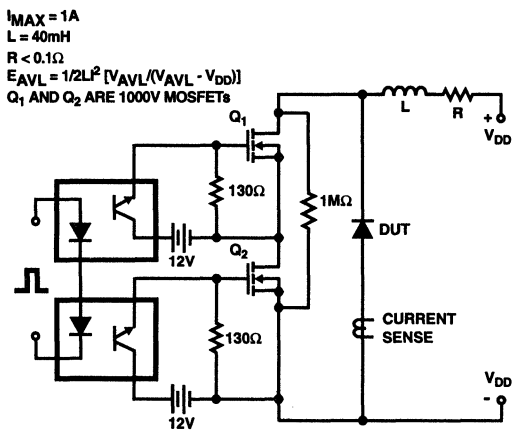


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

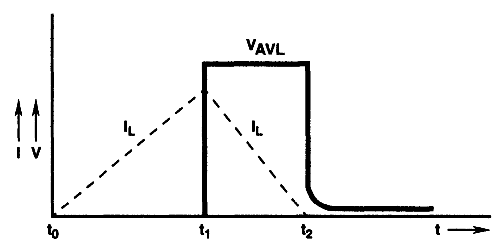


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURP3010, RURP3015, RURP3020

April 1995

30A, 100V - 200V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 45ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

RURP3010, RURP3015, RURP3020 are ultrafast diodes (t_{RR} < 45ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

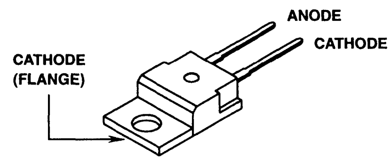
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP3010	TO-220AC	RURP3010
RURP3015	TO-220AC	RURP3015
RURP3020	TO-220AC	RURP3020

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP3010	RURP3015	RURP3020
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total Device Forward Current At Rated V_R and T_C = +150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, Square Wave 20kHZ)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge Applied At Rated Load Condition Halfwave 1 Phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURP3010			RURP3015			RURP3020			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
	I_F = 30A T_C = +25°C	-	-	1.00	-	-	1.00	-	-	1.00	V
I_R at T_C = +150°C	V_R = 100V	-	-	1.0	-	-	-	-	-	-	mA
	V_R = 150V	-	-	-	-	-	1.0	-	-	-	mA
	V_R = 200V	-	-	-	-	-	-	-	-	1.0	mA
I_R at T_C = +25	V_R = 100V	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A	-	-	45	-	-	45	-	-	45	ns
	I_F = 30A	-	-	50	-	-	50	-	-	50	ns
t_A	I_F = 1A	-	24	-	-	24	-	-	24	-	ns
	I_F = 30A	-	28	-	-	28	-	-	28	-	ns
t_B	I_F = 1A	-	17	-	-	17	-	-	17	-	ns
	I_F = 30A	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W
E_{AVL}	See Figures 7 and 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

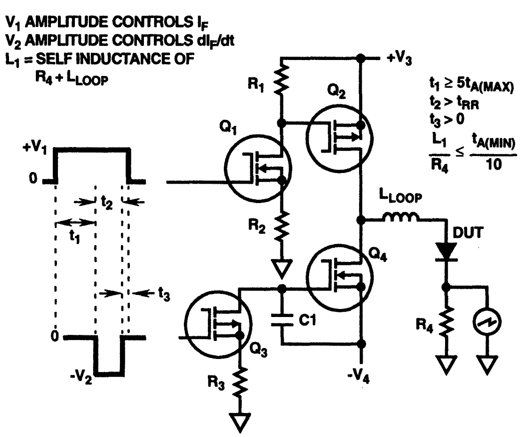


FIGURE 1. t_{RR} TEST CIRCUIT

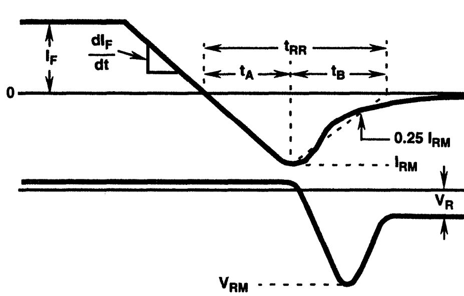


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

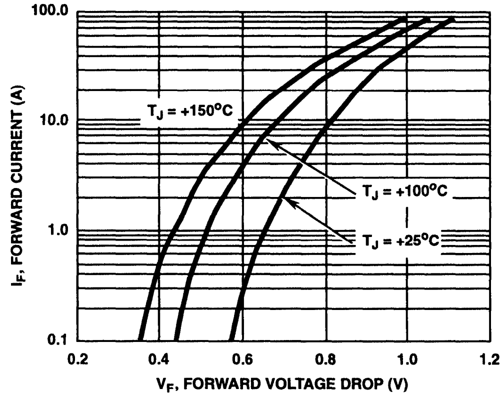


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

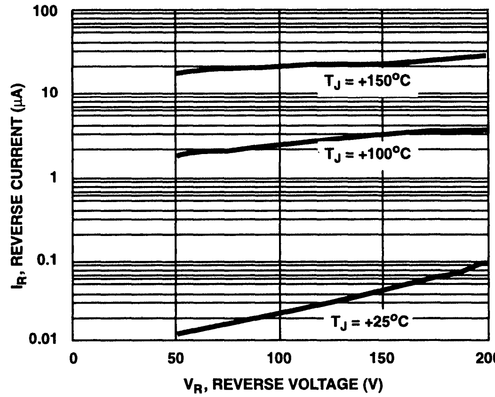


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

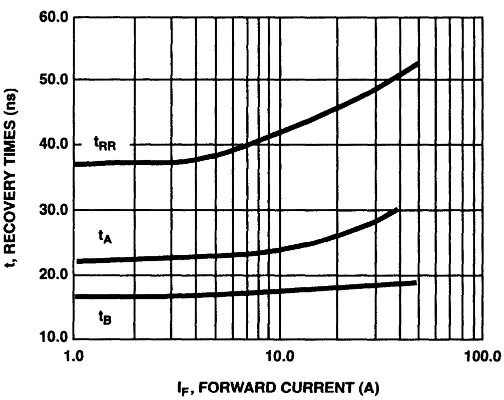


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

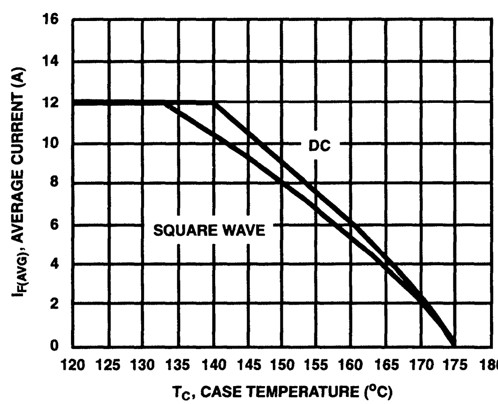


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

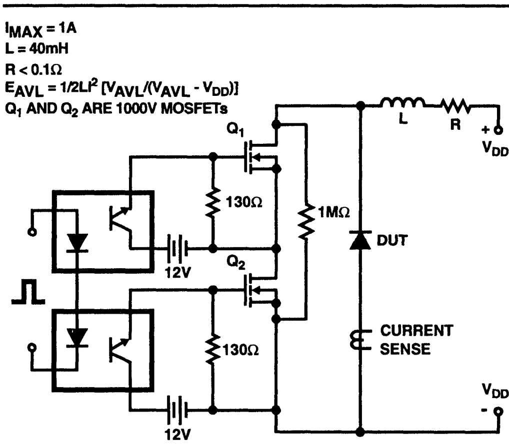


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

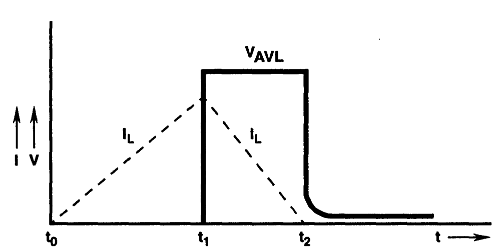


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (1/2) LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

5

ULTRAFAST SINGLE DIODES

RURP3040, RURP3050, RURP3060

HARRIS SEMICONDUCTOR

April 1995

30A, 400V - 600V Ultrafast Diodes

Features

- **Ultrafast with Soft Recovery Characteristic (t_{RR} < 55ns)**
- **+175°C Rated Junction Temperature**
- **Reverse Voltage Up to 600V**
- **Avalanche Energy Rated**

Applications

- **Switching Power Supply**
- **Power Switching Circuits**
- **General Purpose**

Description

RURP3010, RURP3015, RURP3020 are ultrafast diodes (t_{RR} < 55ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

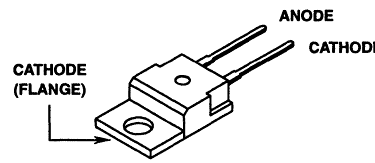
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP3040	TO-220AC	RURP3040
RURP3050	TO-220AC	RURP3050
RURP3060	TO-220AC	RURP3060

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP3040	RURP3050	RURP3060
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

File Number **2776.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS RURP3040 MIN			RURP3050 MIN			RURP3060 MIN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.30	-	-	1.30	-	-	1.30	V
	I_F = 30A, T_C = +25°C	-	-	1.50	-	-	1.50	-	-	1.50	V
I_R at T_C = +150°C	V_R = 400V	-	-	1	-	-	-	-	-	-	mA
	V_R = 500V	-	-	-	-	-	1	-	-	-	mA
	V_R = 600V	-	-	-	-	-	-	-	-	1	mA
I_R at T_C = +25°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 30A	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 30A	-	38	-	-	38	-	-	38	-	ns
t_B	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 30A	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W
E_{AVL}	See Figure 7 and 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

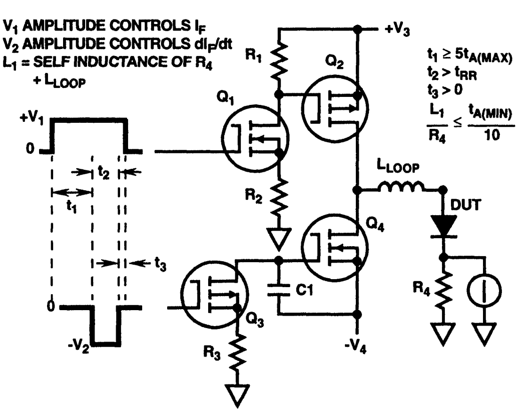


FIGURE 1. t_{RR} TEST CIRCUIT

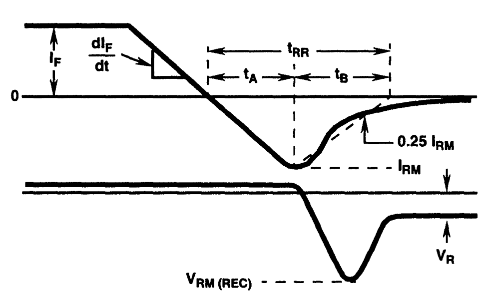


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

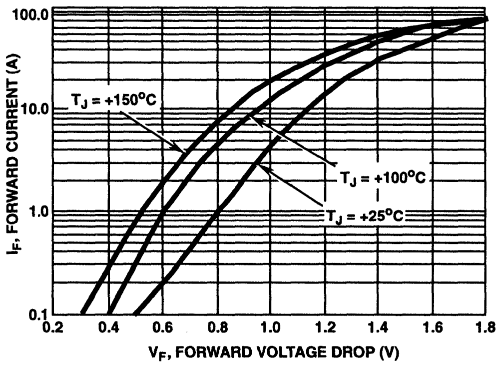


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

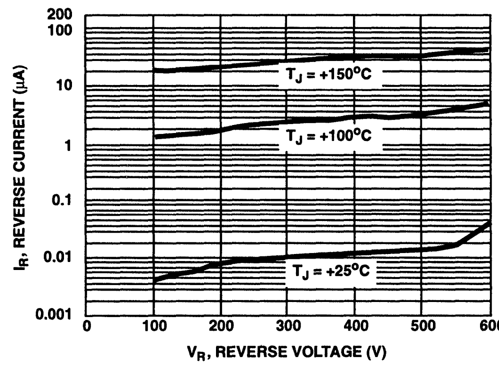


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

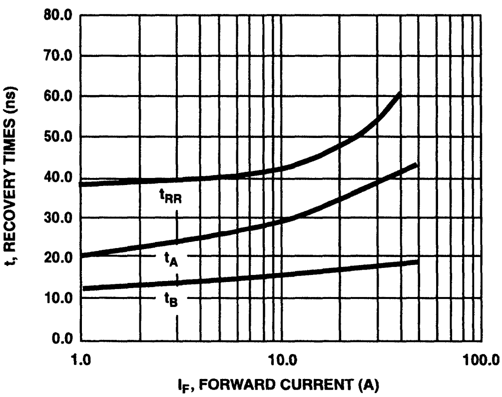


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

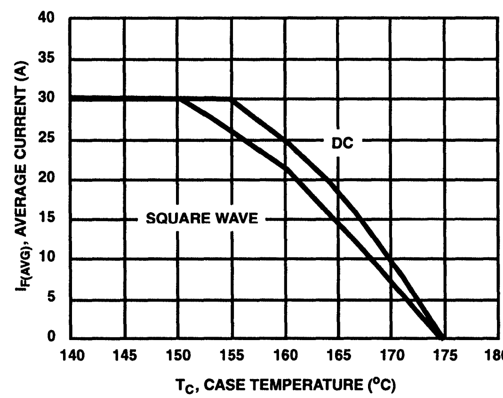


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

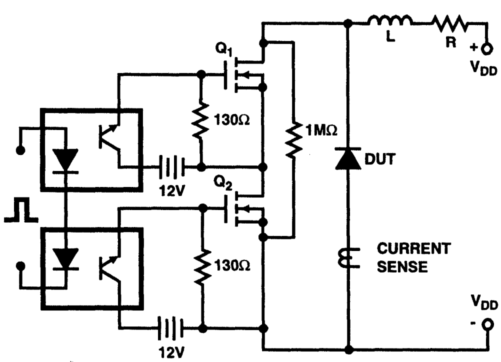


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

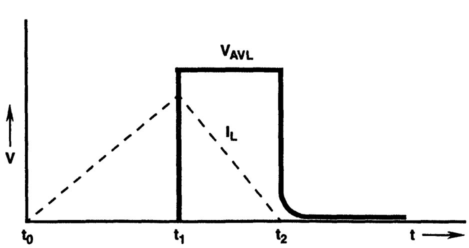


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2)\ LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

HARRIS SEMICONDUCTOR

RURP3070, RURP3080, RURP3090, RURP30100

April 1995

30A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 110ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

RURP3070, RURP3080, RURP3090, RURP30100 are ultrafast diodes with soft recovery characteristics (t_{RR} < 110ns). They have a low forward voltage drop and are silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as flywheel/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

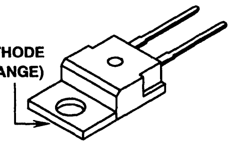
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP3070	TO-220AC	RURP3070
RURP3080	TO-220AC	RURP3080
RURP3090	TO-220AC	RURP3090
RURP30100	TO-220AC	RUR30100

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP3070	RURP3080	RURP3090	RURP30100
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current (T_C = +121°C)	$I_{F(AV)}$	30A	30A	30A	30A
Peak Forward Repetitive Current (Square wave 20kHz)	I_{FRM}	60A	60A	60A	60A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	300A	300A	300A	300A
Maximum Power Dissipation	P_D	125W	125W	125W	125W
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

		LIMITS												
	TEST	RURP3070			RURP3080			RURP3090			RURP30100			
SYMBOL	CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 30A T_C = +150°C	-	-	1.60	-	-	1.60	-	-	1.60	-	-	1.60	V
	I_F = 30A T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at T_C = +150°C	V_R = 700V	-	-	1	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V	-	-	-	-	-	1	-	-	-	-	-	-	mA
	V_R = 900V	-	-	-	-	-	-	-	-	1	-	-	-	mA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	1	mA
I_R at T_C = +25°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A	-	-	110	-	-	110	-	-	110	-	-	110	ns
	I_F = 30A	-	-	150	-	-	150	-	-	150	-	-	150	ns
t_A	I_F = 30A	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	I_F = 30A	-	45	-	-	45	-	-	45	-	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	-	-	1.2	°C/W
E_{AVL}		-	-	20	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

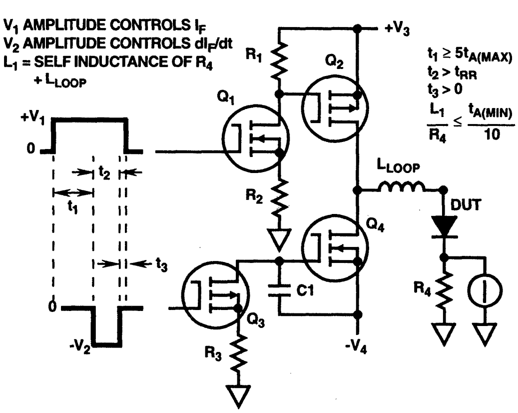


FIGURE 1. t_{RR} TEST CIRCUIT

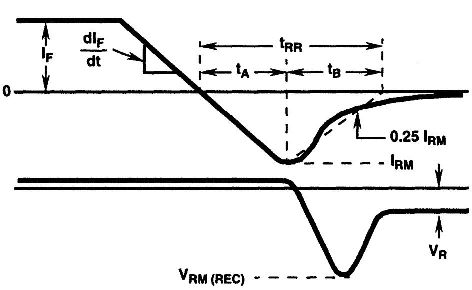


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

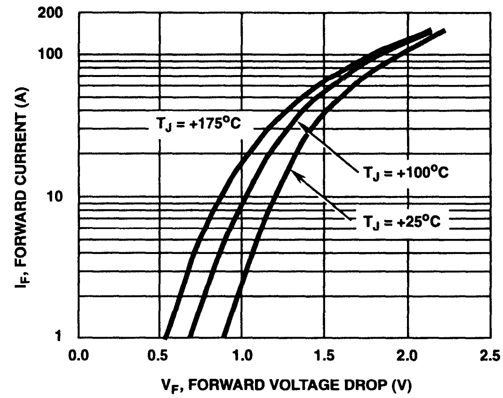


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

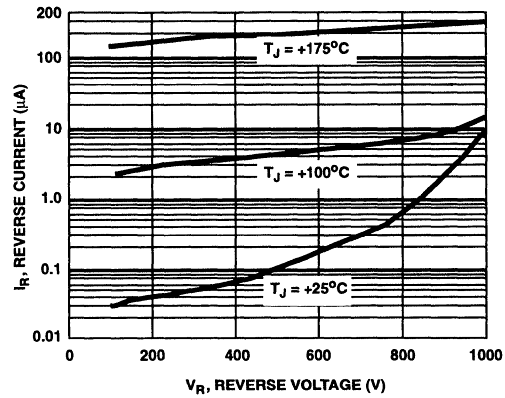


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

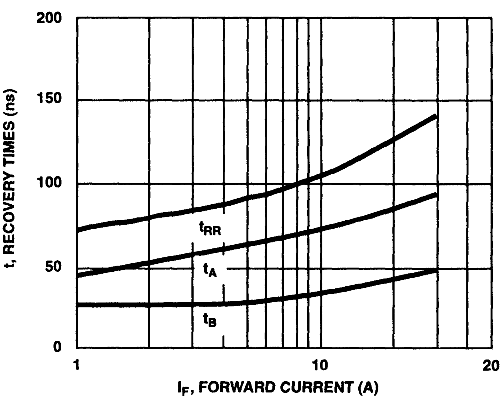


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

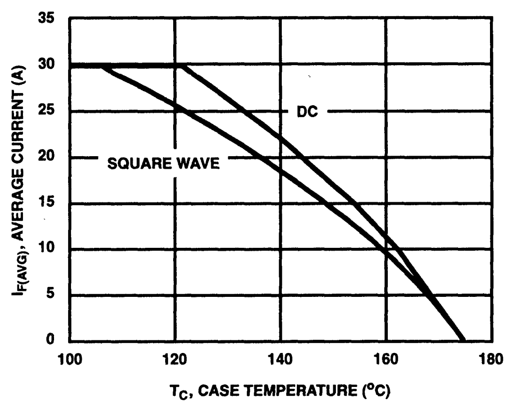


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

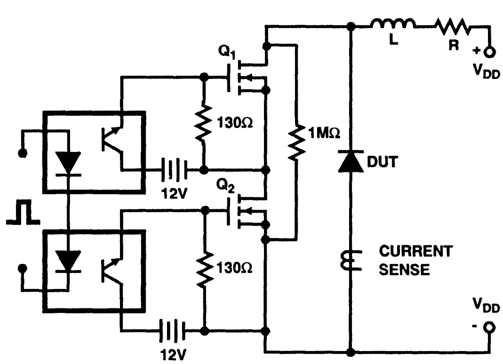


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

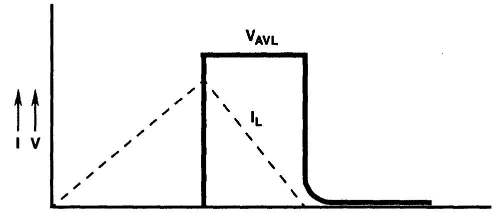


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2) LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$
Q1 AND Q2 ARE 1000V MOSFETs

HARRIS SEMICONDUCTOR

RURP30120

April 1995

30A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . <110ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURP30120 (49031) is an ultrafast diode with soft recovery characteristic (t_{RR} < 110ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

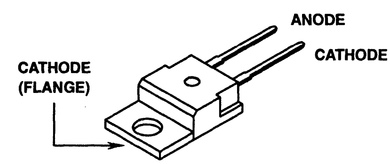
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP30120	TO-220AC	RUR30120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURP30120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +110°C)	$I_{F(AV)}$	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	A
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3397.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	2.1	V
V_F	I_F = 30A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	500	µA
I_R	V_R = 1200V, T_C = +150°C	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	110	ns
	I_F = 30A, dI_F/dt = 100A/µs	-	-	150	ns
t_A	I_F = 30A, dI_F/dt = 100A/µs	-	90	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

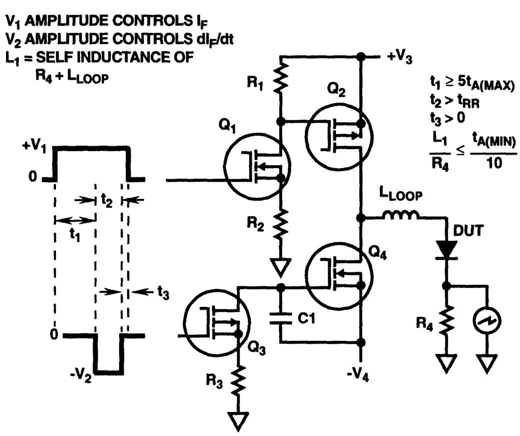


FIGURE 1. t_{RR} TEST CIRCUIT

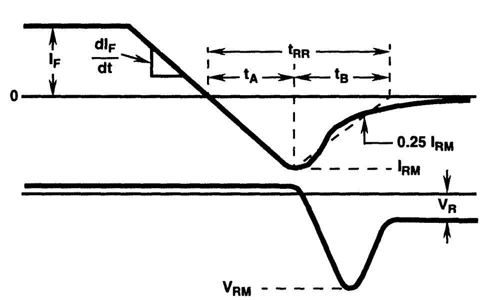


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

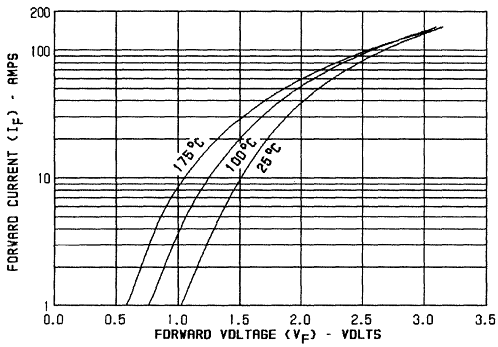


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

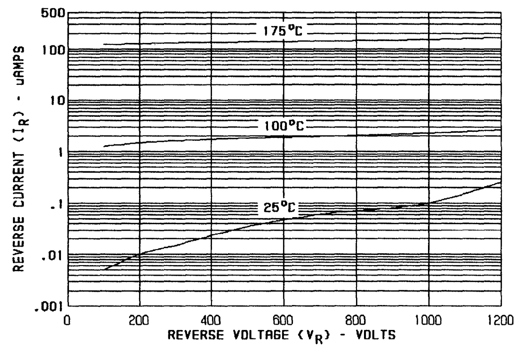


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

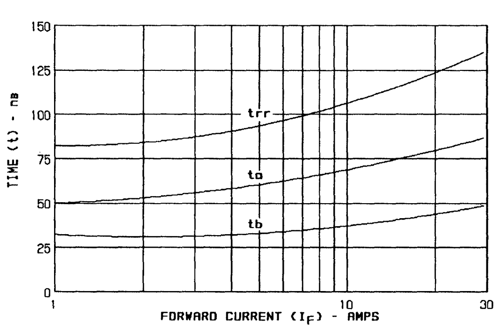


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

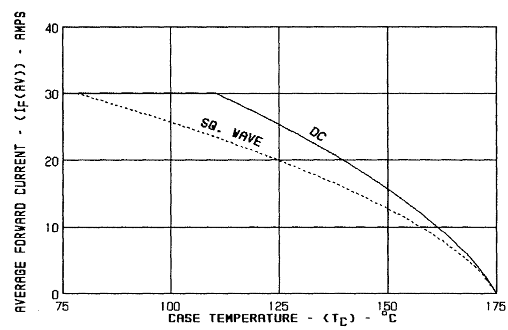


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

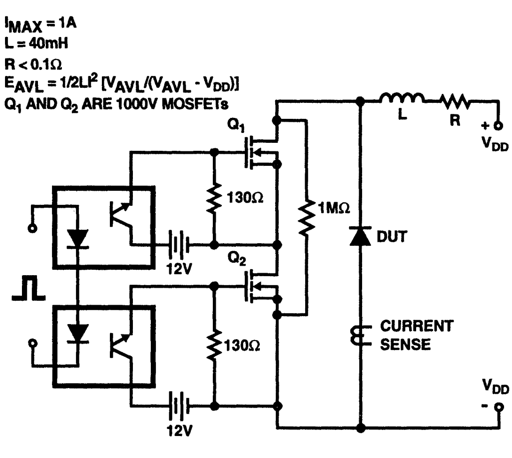


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

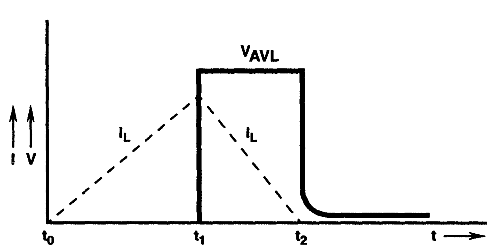


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU5040, RURU5050, RURU5060

April 1995

50A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <65ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU5040, RURU5050 and RURU5060 (TA9909) are ultrafast diodes with soft recovery characteristics (t_{RR} < 65ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

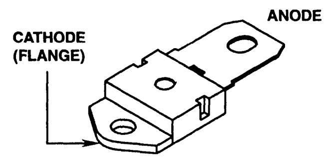
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU5040	TO-218	RURU5040
RURU5050	TO-218	RURU5050
RURU5060	TO-218	RURU5060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU5040	RURU5050	RURU5060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +102°C)	$I_{F(AV)}$	50	50	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	100	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	A
Maximum Power Dissipation	P_D	150	150	150	W
Avalanche Energy	E_{AVL}	40	40	40	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

5 ULTRAFAST SINGLE DIODES

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURU5040			RURU5050			RURU5060			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 50A, T_C = +25^oC$	-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	$I_F = 50A, T_C = +150^oC$	-	-	1.4	-	-	1.4	-	-	1.4	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	1.5	-	-	-	-	-	-	mA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	1.5	-	-	-	mA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	65	-	-	65	-	-	65	ns
	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	-	75	-	-	75	-	-	75	ns
t_A	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	30	-	-	30	-	-	30	-	ns
t_B	$I_F = 50A, dI_F/dt = 100A/\mu s$	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1	-	-	1	-	-	1	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

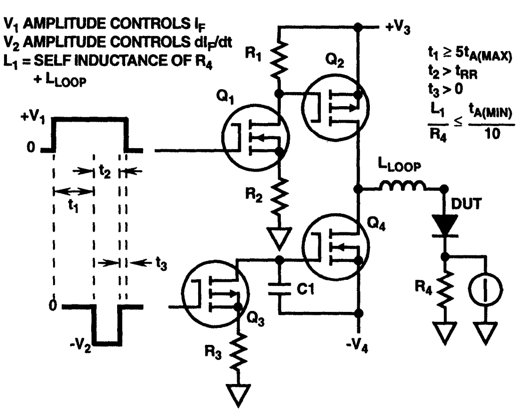


FIGURE 1. t_{RR} TEST CIRCUIT

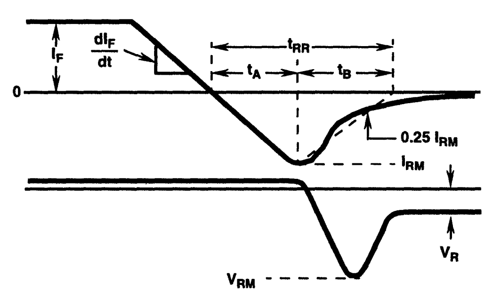


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

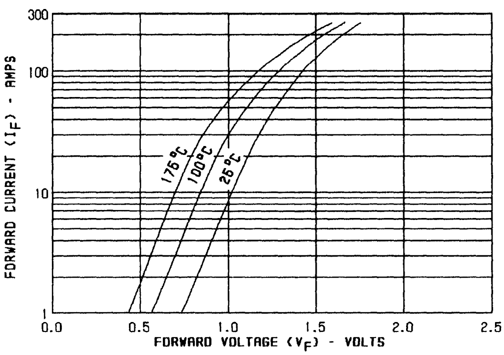


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

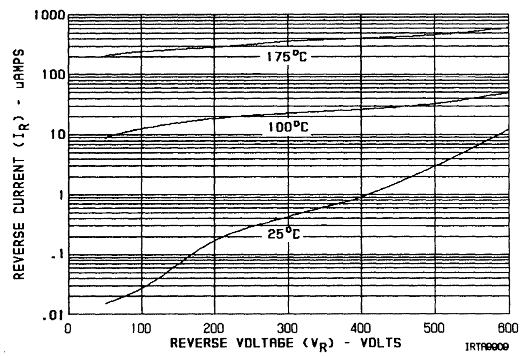


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

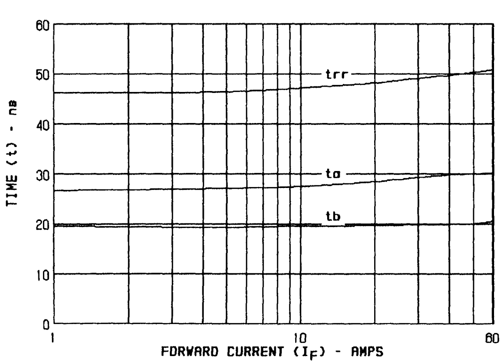


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

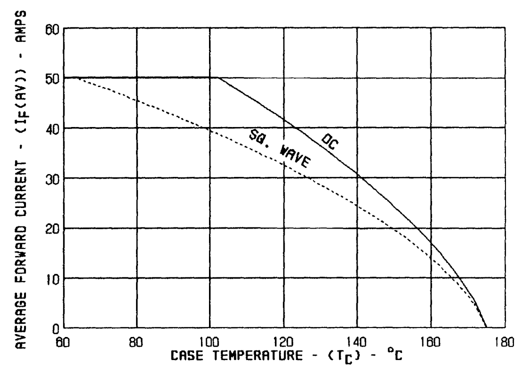


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

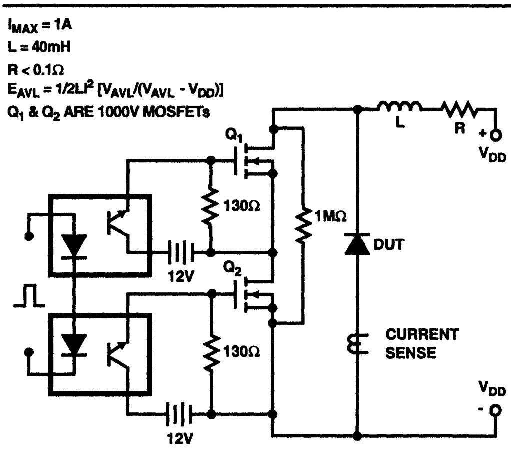


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

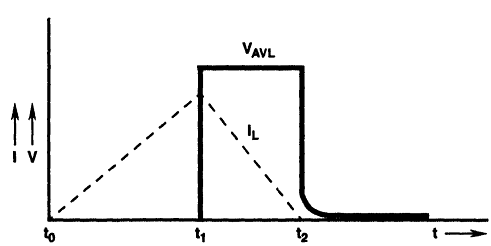


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU5070, RURU5080, RURU5090, RURU50100

April 1995

50A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <125ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU5070, RURU5080, RURU5090 and RURU50100 (TA9910) are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

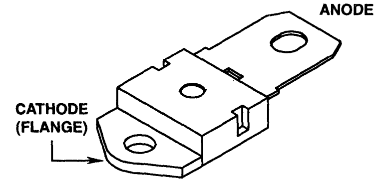
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU5070	TO-218	RURU5070
RURU5080	TO-218	RURU5080
RURU5090	TO-218	RURU5090
RURU50100	TO-218	RURU50100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU5070	RURU5080	RURU5090	RURU50100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +88.6°C)	$I_{F(AV)}$	50	50	50	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	100	100	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	500	A
Maximum Power Dissipation	P_D	150	150	150	150	W
Avalanche Energy (L = 40mH)	E_{AVL}	40	40	40	40	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3376.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		LIMITS												
		RURU5070			RURU5080			RURU5090			RURU50100			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 50A	-	-	1.9	-	-	1.9	-	-	1.9	-	-	1.9	V
V_F	I_F = 50A, T_C = 150°C	-	-	1.7	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 700V, T_C = 150°C	-	-	1.5	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = 150°C	-	-	-	-	-	1.5	-	-	-	-	-	-	mA
	V_R = 900V, T_C = 150°C	-	-	-	-	-	-	-	-	1.5	-	-	-	mA
	V_R = 1000V, T_C = 150°C	-	-	-	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	125	-	-	125	-	-	125	-	-	125	ns
	I_F = 50A, dI_F/dt = 100A/µs	-	-	200	-	-	200	-	-	200	-	-	200	ns
t_A	I_F = 50A, dI_F/dt = 100A/µs	-	110	-	-	110	-	-	110	-	-	110	-	ns
t_B	I_F = 50A, dI_F/dt = 100A/µs	-	65	-	-	65	-	-	65	-	-	65	-	ns
$R_{\theta JC}$		-	-	1.0	-	-	1.0	-	-	1.0	-	-	1.0	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

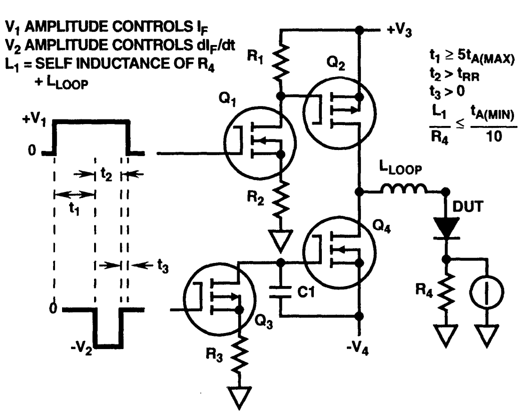


FIGURE 1. t_{RR} TEST CIRCUIT

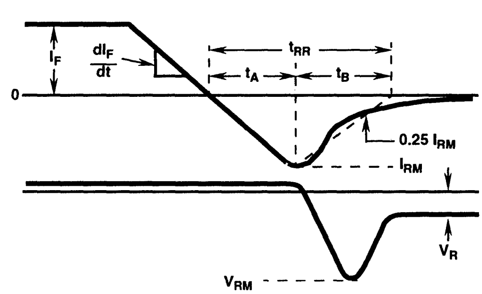


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

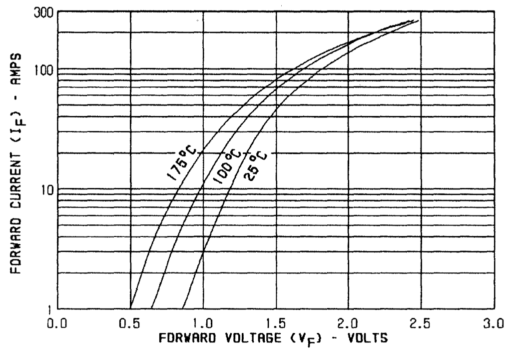


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

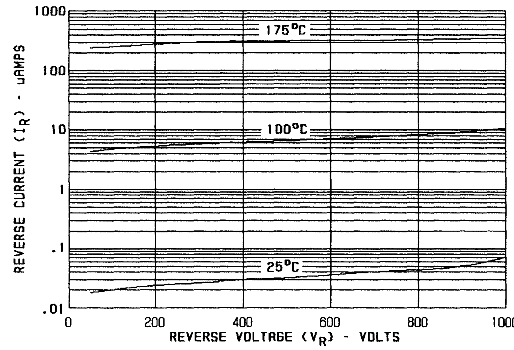


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

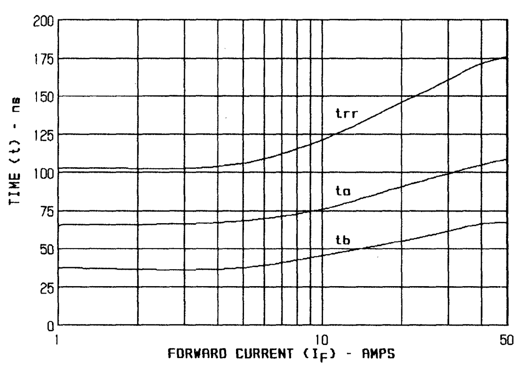


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

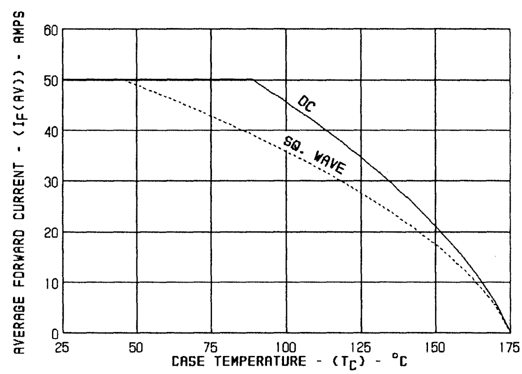


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

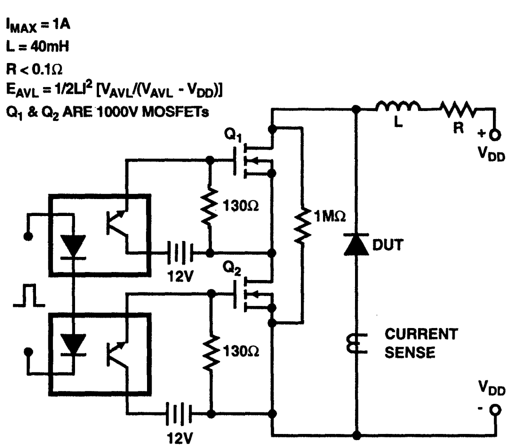


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

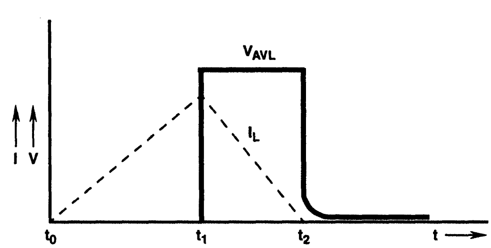


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU50120

April 1995

50A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . < 125ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURU50120 (TA49099) are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

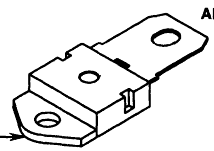
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU50120	TO-218	RURU50120

NOTE: When ordering, use the entire part number.

Package

SINGLE LEAD JEDEC STYLE TO-218



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU50120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +85°C)	$I_{F(AV)}$	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	170	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3741.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 50A, T_C = +25°C	-	-	2.1	V
	I_F = 50A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	500	μA
	V_R = 1200V, T_C = +150°C	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	125	ns
	I_F = 50A, dI_F/dt = 100A/μs	-	-	200	ns
t_A	I_F = 50A, dI_F/dt = 100A/μs	-	95	-	ns
t_B	I_F = 50A, dI_F/dt = 100A/μs	-	70	-	ns
Q_{RR}	I_F = 50A, dI_F/dt = 100A/μs	-	800	-	nC
C_J	V_R = 10V, I_F = 0A	-	160	-	pF
$R_{\theta JC}$		-	-	0.9	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

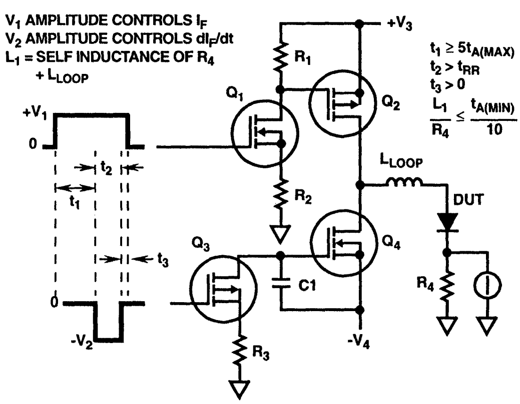


FIGURE 1. t_{RR} TEST CIRCUIT

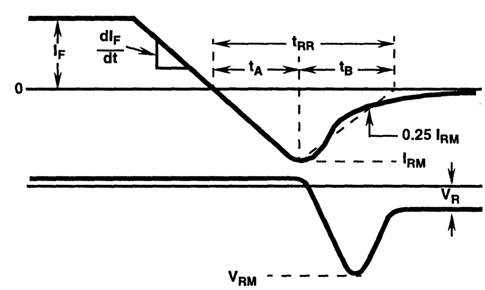


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

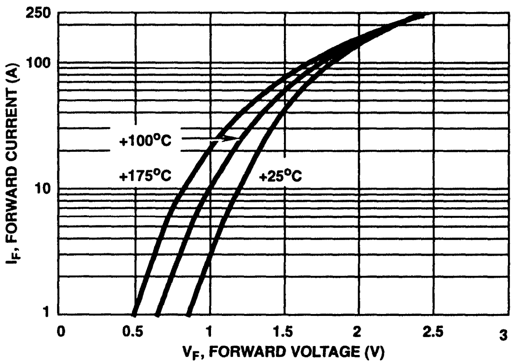


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

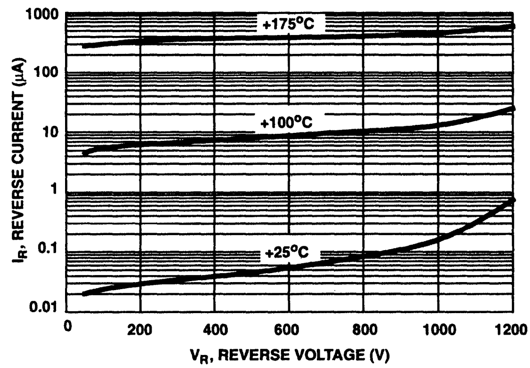


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

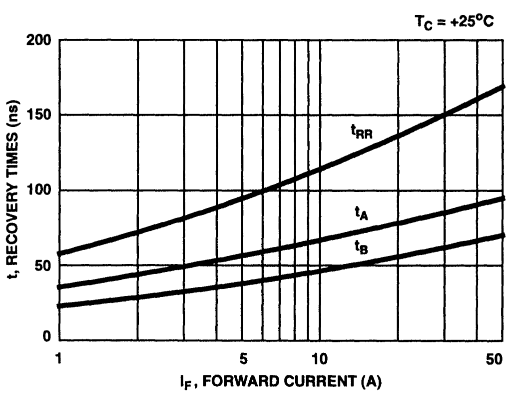


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

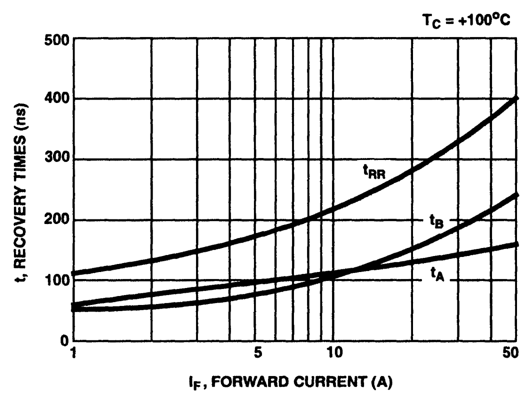


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

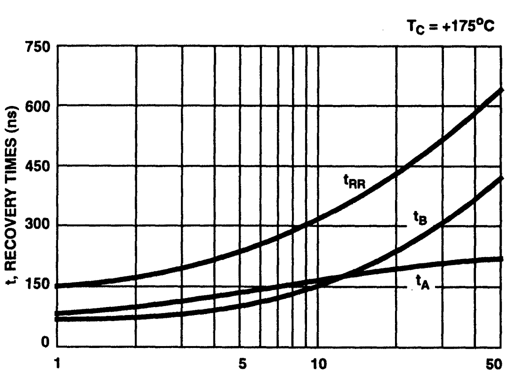


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

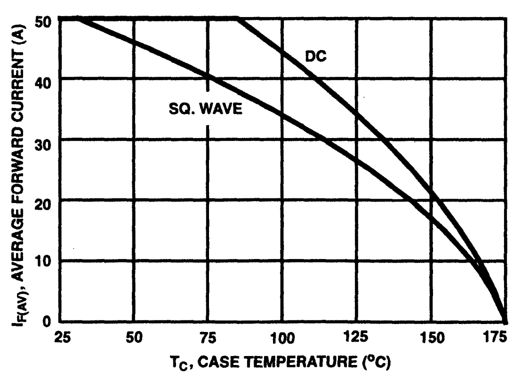


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

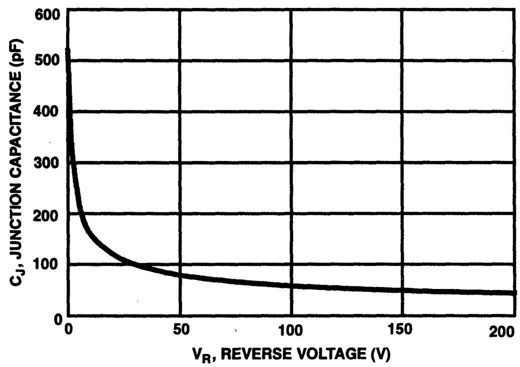


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

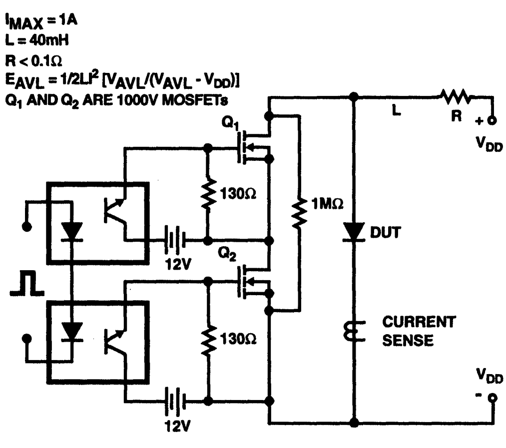


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

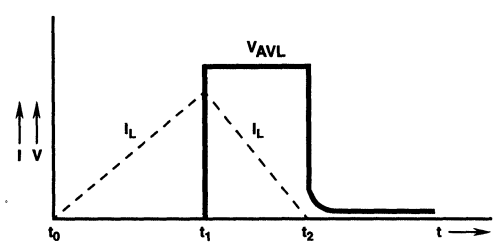


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU75120

April 1995

75A, 1200V Ultrafast Diode

Features

- Ultrafast with Soft Recovery . . . . <125ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURU75120 (TA49032) is an ultrafast diode with soft recovery characteristics (t_{RR} < 125ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

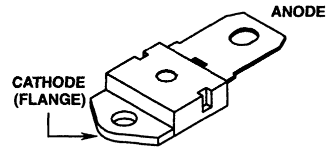
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU75120	TO-218	RURU75120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings $T_C = +25^oC$

		RURU75120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current ($T_C = +56.75^oC$)	$I_{F(AV)}$	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	190	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 75A		-	-	2.1	V
V_F	I_F = 75A	T_C = +150°C	-	-	1.9	
I_R	V_R = 1200V		-	-	500	μA
I_R	V_R = 1200V	T_C = +150°C	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	125	ns
t_{RR}	I_F = 75A, dI_F/dt = 100A/μs		-	-	200	
t_A	I_F = 75A, dI_F/dt = 100A/μs		-	90	-	
t_B	I_F = 75A, dI_F/dt = 100A/μs		-	65	-	
$R_{\theta JC}$			-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

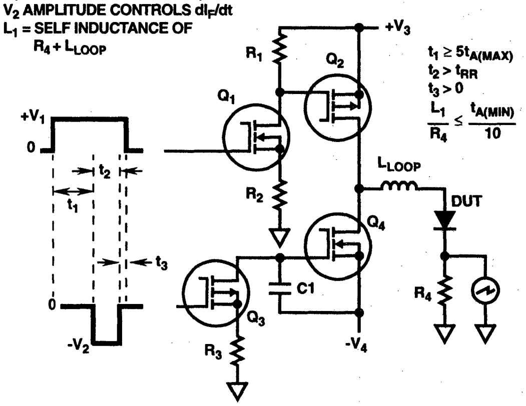


FIGURE 1. t_{RR} TEST CIRCUIT

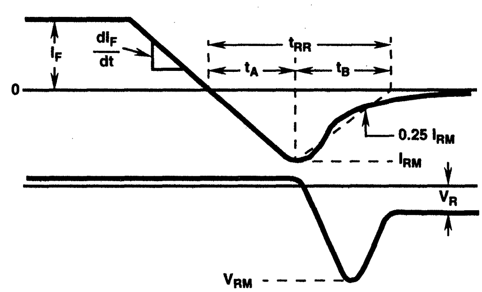


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

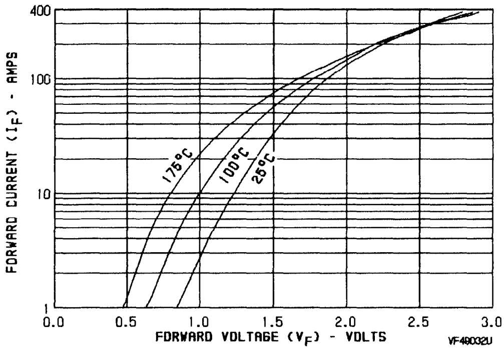


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

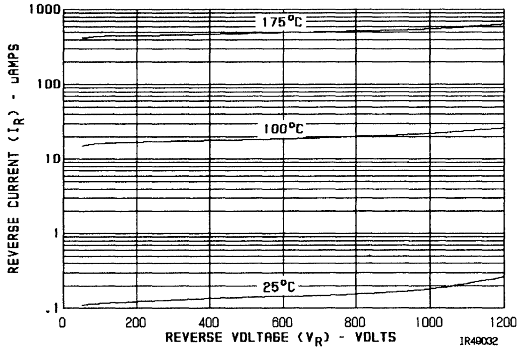


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

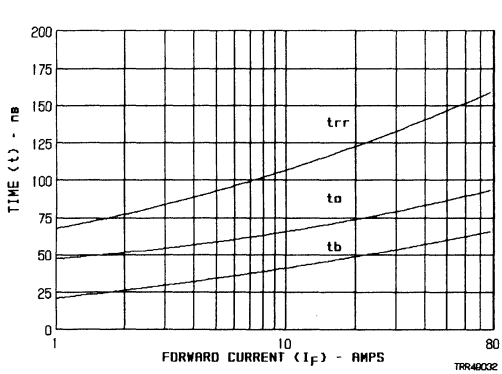


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

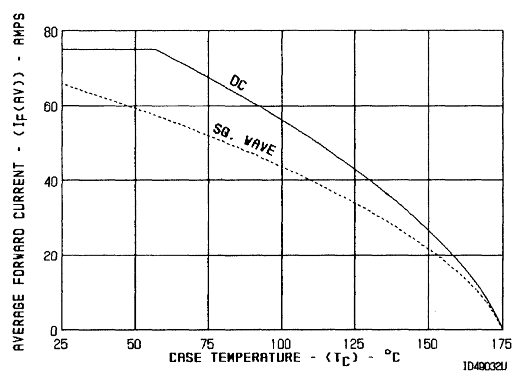


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

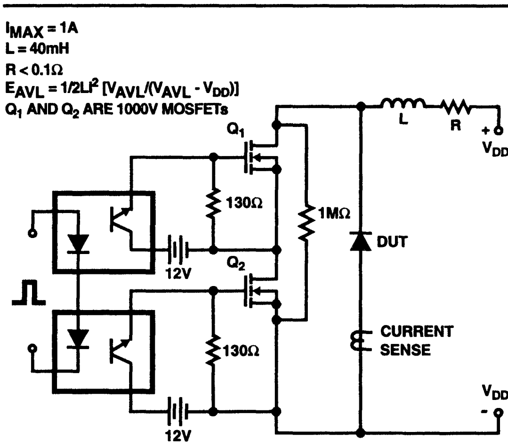


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

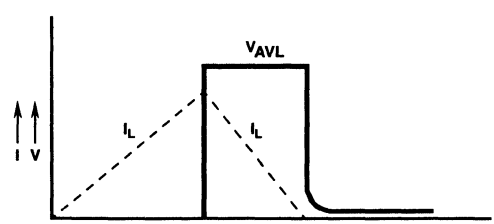


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU8040, RURU8050, RURU8060

April 1995

80A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <75ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU8040, RURU8050 and RURU8060 (TA9886) are ultrafast diodes with soft recovery characteristics (t_{RR} < 75ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

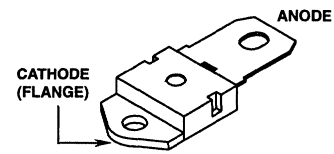
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU8040	TO-218	RURU8040
RURU8050	TO-218	RURU8050
RURU8060	TO-218	RURU8060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU8040	RURU8050	RURU8060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +84°C)	$I_{F(AV)}$	80	80	80	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	160	160	160	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	800	800	800	A
Maximum Power Dissipation	P_D	180	180	180	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3380.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURU8040 MIN	RURU8040 TYP	RURU8040 MAX	RURU8050 MIN	RURU8050 TYP	RURU8050 MAX	RURU8060 MIN	RURU8060 TYP	RURU8060 MAX	UNITS
V_F	I_F = 80A, T_C = +25°C	-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	I_F = 80A, T_C = +150°C	-	-	1.4	-	-	1.4	-	-	1.4	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 400V, T_C = +150°C	-	-	2.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	2.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	75	-	-	75	-	-	75	ns
	I_F = 80A, dI_F/dt = 100A/μs	-	-	85	-	-	85	-	-	85	ns
t_A	I_F = 80A, dI_F/dt = 100A/μs	-	40	-	-	40	-	-	40	-	ns
t_B	I_F = 80A, dI_F/dt = 100A/μs	-	25	-	-	25	-	-	25	-	ns
$R_{\theta JC}$		-	-	0.83	-	-	0.83	-	-	0.83	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

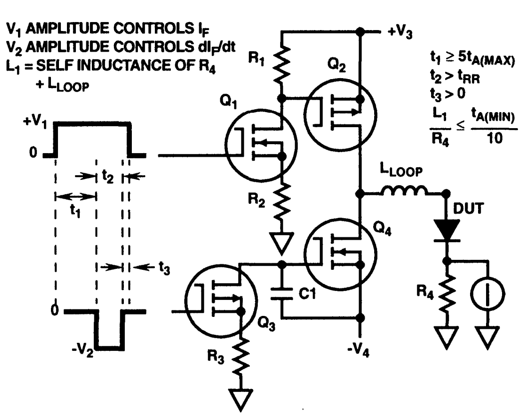


FIGURE 1. t_{RR} TEST CIRCUIT

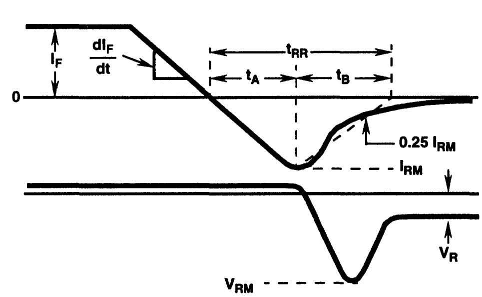


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

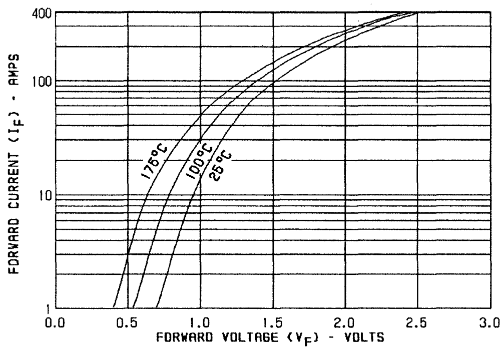


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

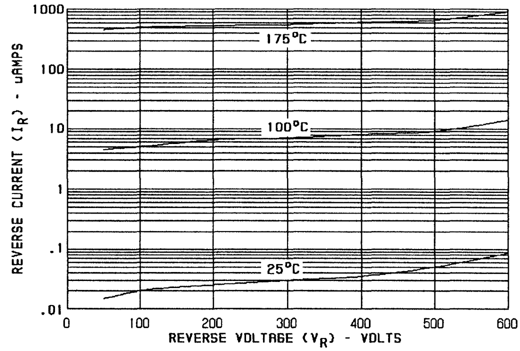


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

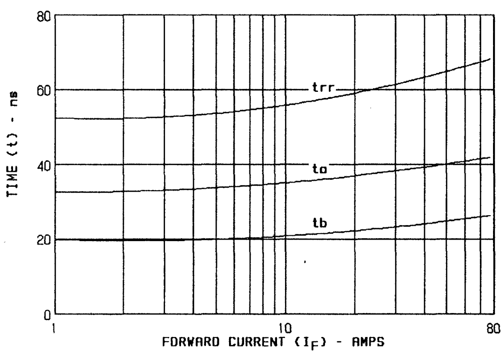


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

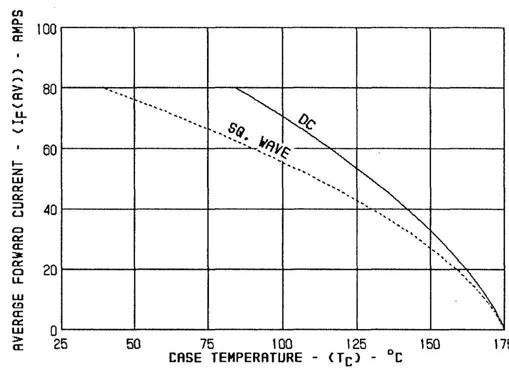


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

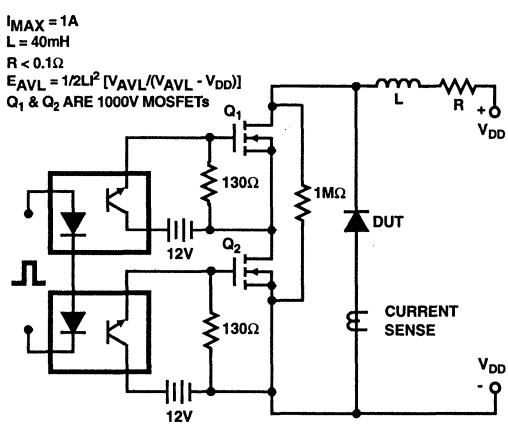


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

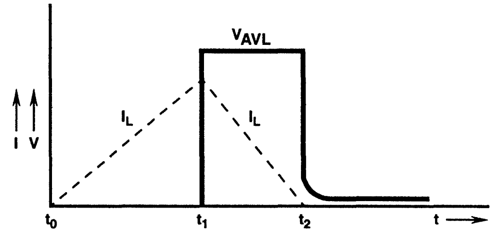


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU8070, RURU8080, RURU8090, RURU80100

April 1995

80A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <125ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU8070, RURU8080, RURU8090 and RURU80100 (TA9887) are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

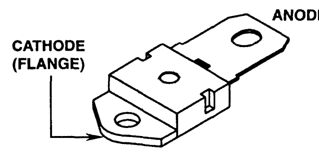
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU8070	TO-218	RURU8070
RURU8080	TO-218	RURU8080
RURU8090	TO-218	RURU8090
RURU80100	TO-218	RURU80100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU8070	RURU8080	RURU8090	RURU80100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +59°C)	$I_{F(AV)}$	80	80	80	80	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	160	160	160	160	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	500	A
Maximum Power Dissipation	P_D	180	180	180	180	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURU8070			RURU8080			RURU8090			RURU80100			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 80A	-	-	1.9	-	-	1.9	-	-	1.9	-	-	1.9	V
V_F	I_F = 80A, T_C = 150°C	-	-	1.7	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = 150°C	-	-	2	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = 150°C	-	-	-	-	-	2	-	-	-	-	-	-	mA
	V_R = 900V, T_C = 150°C	-	-	-	-	-	-	-	-	2	-	-	-	mA
	V_R = 1000V, T_C = 150°C	-	-	-	-	-	-	-	-	-	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	125	-	-	125	-	-	125	-	-	125	ns
	I_F = 80A, dI_F/dt = 100A/μs	-	-	200	-	-	200	-	-	200	-	-	200	ns
t_A	I_F = 80A, dI_F/dt = 100A/μs	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	I_F = 80A, dI_F/dt = 100A/μs	-	65	-	-	65	-	-	65	-	-	65	-	ns
$R_{\theta JC}$		-	-	0.83	-	-	0.83	-	-	0.83	-	-	0.83	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

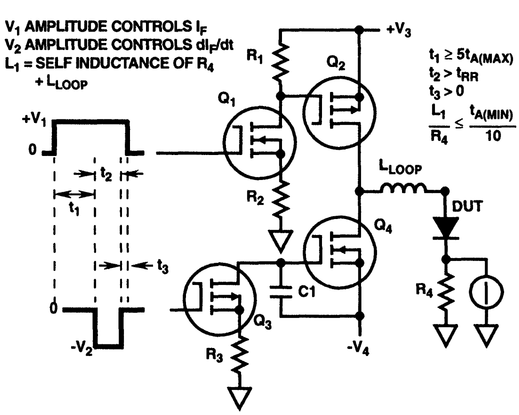


FIGURE 1. t_{RR} TEST CIRCUIT

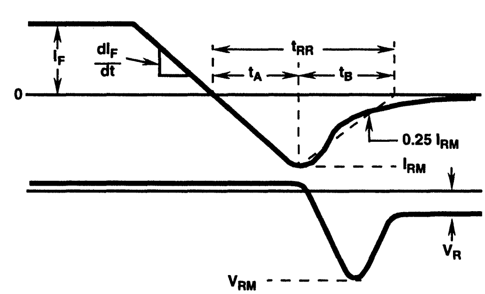


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

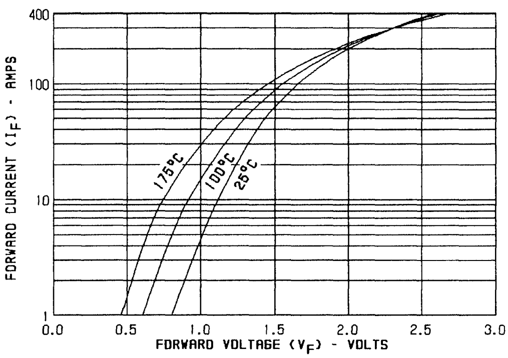


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

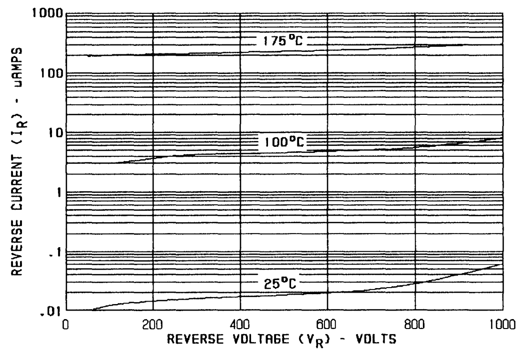


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

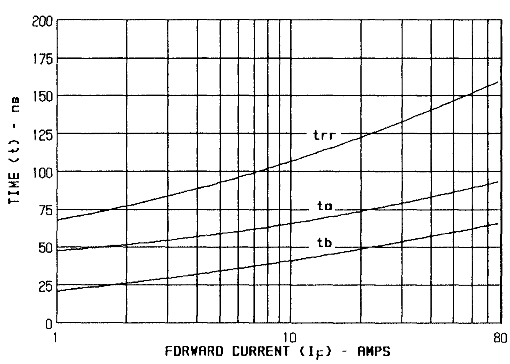


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

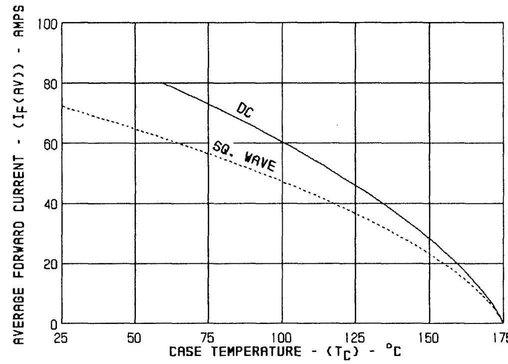


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

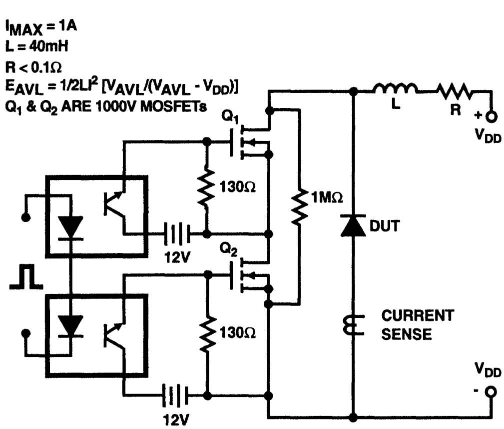


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

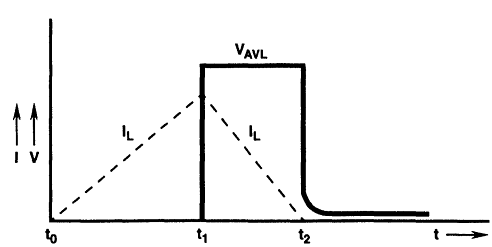


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

5 ULTRAFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

RURU10040, RURU10050, RURU10060

April 1995

100A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <80ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU10040, RURU10050 and RURU10060 (TA49019) are ultrafast diodes with soft recovery characteristics (t_{RR} < 80ns).They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

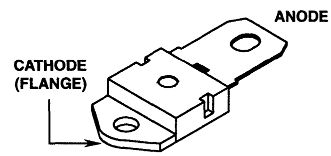
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU10040	TO-218	RURU10040
RURU10050	TO-218	RURU10050
RURU10060	TO-218	RURU10060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings $T_C = +25^oC$

		RURU10040	RURU10050	RURU10060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current ($T_C = +68.2^oC$)	$I_{F(AV)}$	100	100	100	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	200	200	200	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1000	1000	1000	A
Maximum Power Dissipation	P_D	210	210	210	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	^oC

File Number **3546.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RURU10040 LIMITS			RURU10050 LIMITS			RURU10060 LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 100A		-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	I_F = 100A	T_C = +150°C	-	-	1.4	-	-	1.4	-	-	1.4	
I_R	V_R = 400V V_R = 500V V_R = 600V		- - -	- - -	500 - -	- - -	- - -	- 500 -	- - -	- - -	- - 500	μA
I_R	V_R = 400V V_R = 500V V_R = 600V	T_C = +150°C	- - -	- - -	2.0 - -	- - -	- - -	- 2.0 -	- - -	- - -	- - 2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	80	-	-	80	-	-	80	
t_{RR}	I_F = 100A, dI_F/dt = 100A/μs		-	-	100	-	-	100	-	-	100	
t_A	I_F = 100A, dI_F/dt = 100A/μs		-	45	-	-	45	-	-	45	-	ns
t_B	I_F = 100A, dI_F/dt = 100A/μs		-	25	-	-	25	-	-	25	-	
$R_{\theta JC}$			-	-	0.71	-	-	0.71	-	-	0.71	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

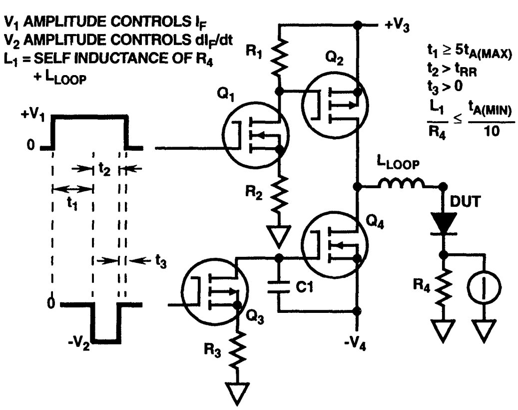


FIGURE 1. t_{RR} TEST CIRCUIT

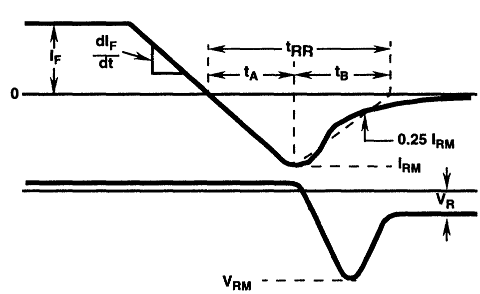


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

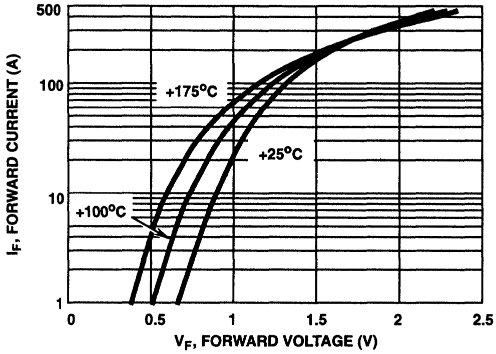


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

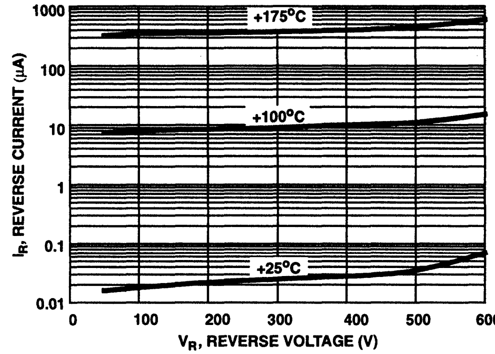


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

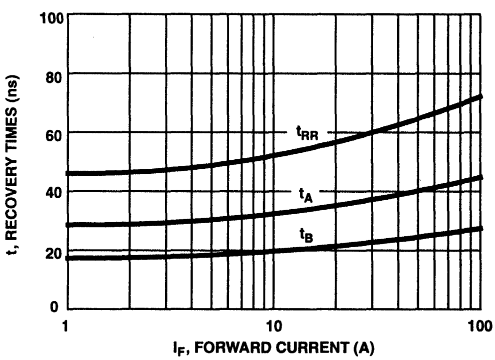


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

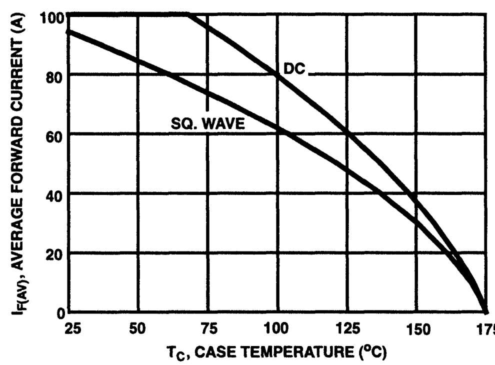


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

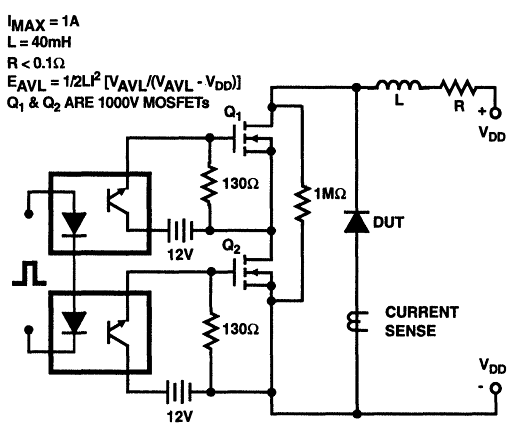


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

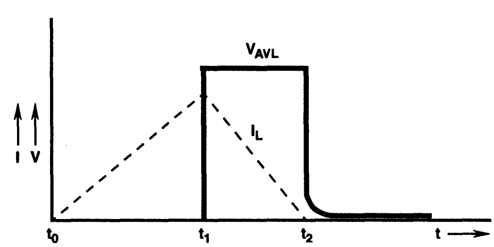


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU100120

April 1945

100A, 1200V Ultrafast Diode

Features

- **Ultrafast with Soft Recovery . . . . <125ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage 1200V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

The RURU100120 (TA49020) is an ultrafast diode with soft recovery characteristics (t_{RR} < 125ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

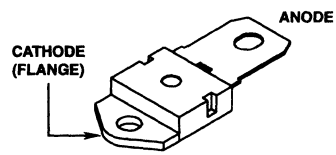
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU100120	TO-218	URU100120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings $T_C = +25^oC$

		RURU100120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current ($T_C = +48.7^oC$)	$I_{F(AV)}$	100	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	200	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	210	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 100A		-	-	2.1	V
V_F	I_F = 100A	T_C = +150°C	-	-	1.9	
I_R	V_R = 1200V		-	-	500	μA
I_R	V_R = 1200V	T_C = +150°C	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	125	ns
t_{RR}	I_F = 100A, dI_F/dt = 100A/μs		-	-	200	
t_A	I_F = 100A, dI_F/dt = 100A/μs		-	90	-	
t_B	I_F = 100A, dI_F/dt = 100A/μs		-	65	-	
$R_{\theta JC}$			-	-	0.71	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

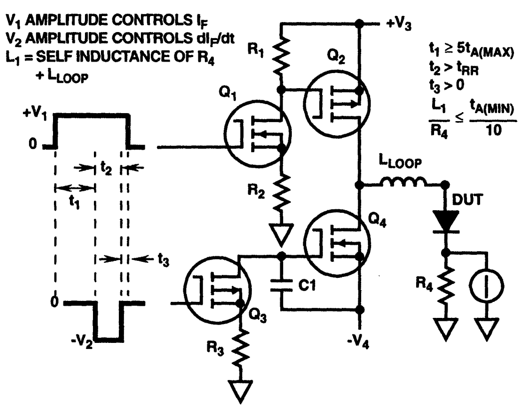


FIGURE 1. t_{RR} TEST CIRCUIT

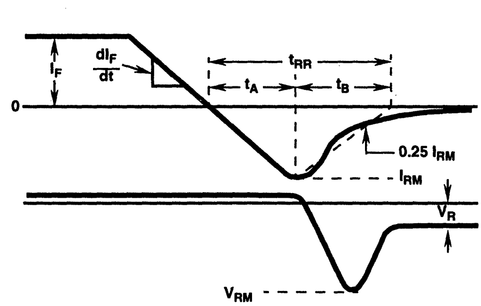


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

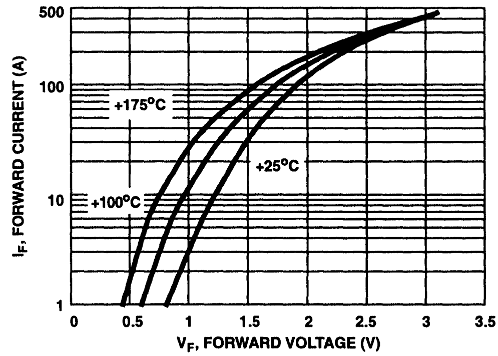


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

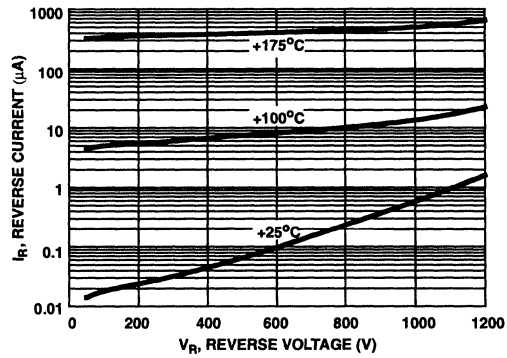


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

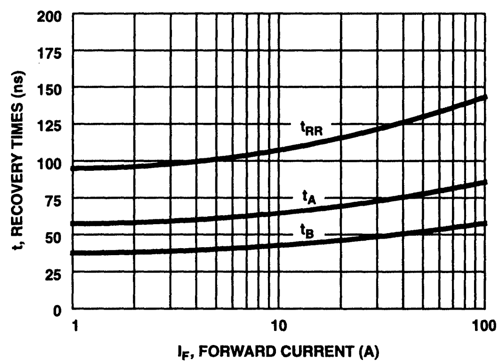


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

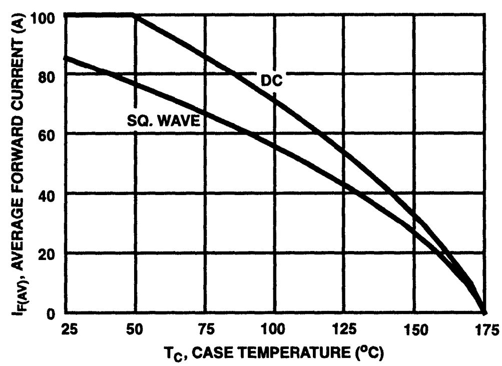


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

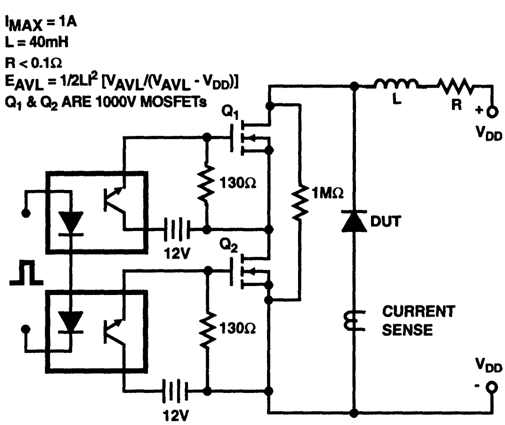


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

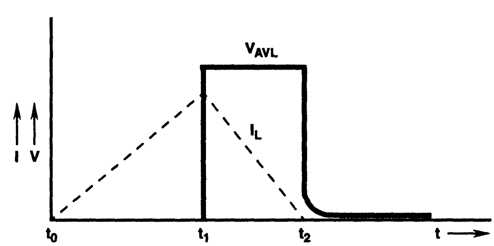


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU15040, RURU15050, RURU15060

April 1995

150A, 400V - 600V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switchssing Circuits
- General Purpose

Description

RURU15040, RURU15050 and RURU15060 are ultrafast diodes with soft recovery characteristics (t_{RR} < 85ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

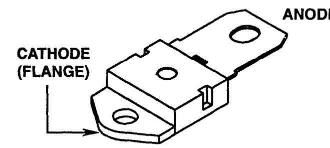
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU15040	TO-218	RURU15040
RURU15050	TO-218	RURU15050
RURU15060	TO-218	RURU15060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU15040	RURU15050	RURU15060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +85°C)	$I_{F(AV)}$	150	150	150	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	300	300	300	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1500	1500	1500	A
Maximum Power Dissipation	P_D	375	375	375	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3201.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURU15040			RURU15050			RURU15060			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 150A$, $T_C = +25^oC$	-	-	1.6	-	-	1.6	-	-	1.6	V
V_F	$I_F = 150A$, $T_C = +150^oC$	-	-	1.4	-	-	1.4	-	-	1.4	V
I_R	$V_R = 400V$, $T_C = +25^oC$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 500V$, $T_C = +25^oC$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 600V$, $T_C = +25^oC$	-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 400V$, $T_C = 150^oC$	-	-	3.0	-	-	-	-	-	-	mA
	$V_R = 500V$, $T_C = 150^oC$	-	-	-	-	-	3.0	-	-	-	mA
	$V_R = 600V$, $T_C = 150^oC$	-	-	-	-	-	-	-	-	3.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	85	-	-	85	-	-	85	ns
	$I_F = 150A$, $dI_F/dt = 100A/\mu s$	-	-	100	-	-	100	-	-	100	ns
t_A	$I_F = 150A$, $dI_F/dt = 100A/\mu s$	-	60	-	-	60	-	-	60	-	ns
t_B	$I_F = 150A$, $dI_F/dt = 100A/\mu s$	-	30	-	-	30	-	-	30	-	ns
$R_{\theta JC}$		-	-	0.4	-	-	0.4	-	-	0.4	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

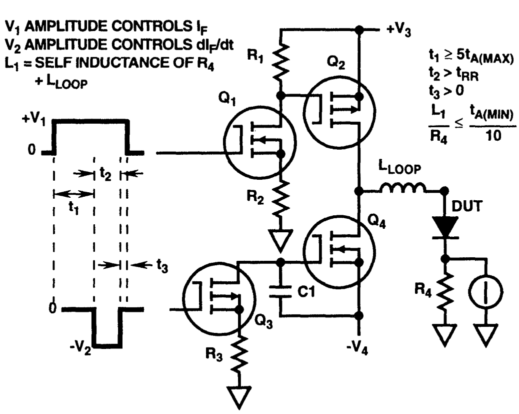


FIGURE 1. t_{RR} TEST CIRCUIT

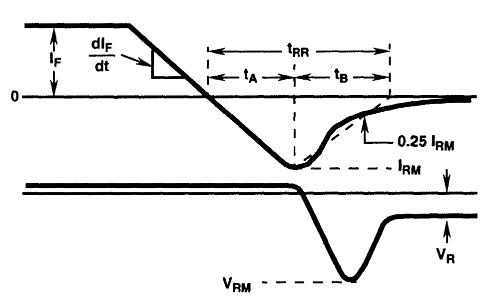


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

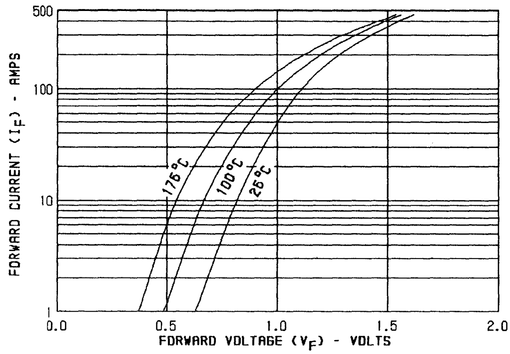


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

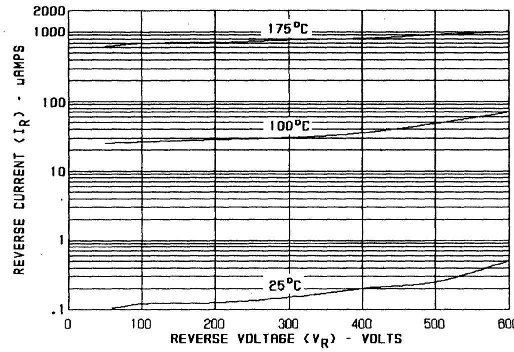


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

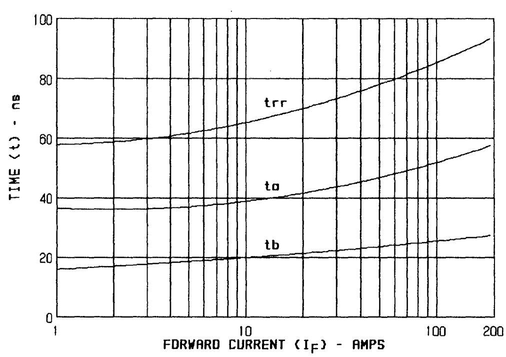


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

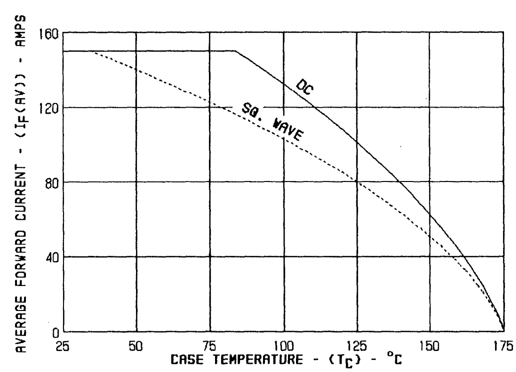


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

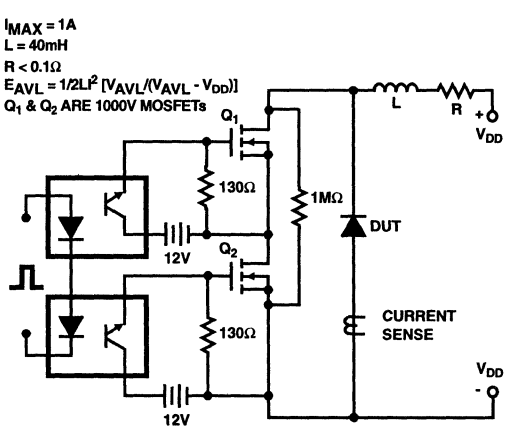


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

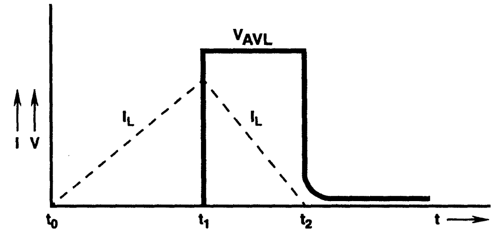


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURU15070, RURU15080, RURU15090, RURU150100

April 1995

150A, 700V - 1000V Ultrafast Diodes

Features

- Ultrafast with Soft Recovery .... <125ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURU15070, RURU15080 and RURU15090 and RURU150100 are ultrafast diodes with soft recovery characteristics (t_{RR} < 125ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

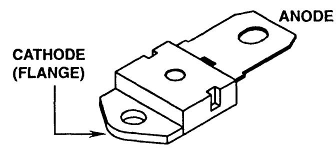
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURU15070	TO-218	RURU15070
RURU15080	TO-218	RURU15080
RURU15090	TO-218	RURU15090
RURU150100	TO-218	RUR150100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE SINGLE LEAD TO-218



Symbol

5

ULTRAFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURU15070	RURU15080	RURU15090	RURU150100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +65°C)	$I_{F(AV)}$	150	150	150	150	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	300	300	300	300	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1500	1500	1500	1500	A
Maximum Power Dissipation	P_D	375	375	375	375	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3202.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURU15070 MIN	RURU15070 TYP	RURU15070 MAX	RURU15080 MIN	RURU15080 TYP	RURU15080 MAX	RURU15090 MIN	RURU15090 TYP	RURU15090 MAX	RURU150100 MIN	RURU150100 TYP	RURU150100 MAX	UNITS
V_F	I_F = 150A, T_C = +25°C	-	-	1.9	-	-	1.9	-	-	1.9	-	-	1.9	V
V_F	I_F = 150A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	3.0	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	3.0	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	3.0	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	3.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	125	-	-	125	-	-	125	-	-	125	ns
	I_F = 150A, dI_F/dt = 100A/μs	-	-	200	-	-	200	-	-	200	-	-	200	ns
t_A	I_F = 150A, dI_F/dt = 100A/μs	-	100	-	-	100	-	-	100	-	-	100	-	ns
t_B	I_F = 150A, dI_F/dt = 100A/μs	-	75	-	-	75	-	-	75	-	-	75	-	ns
$R_{\theta JC}$		-	-	0.4	-	-	0.4	-	-	0.4	-	-	0.4	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

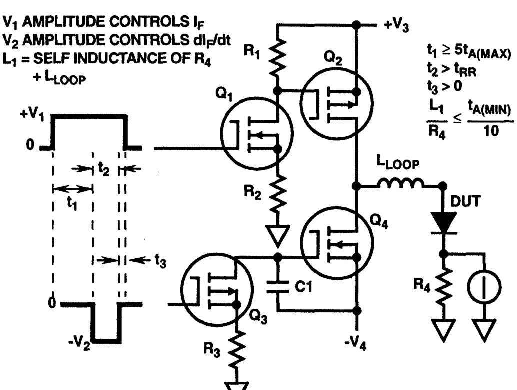


FIGURE 1. t_{RR} TEST CIRCUIT

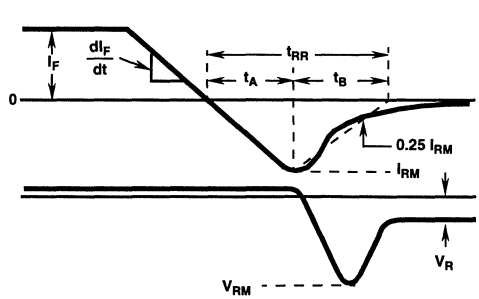


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

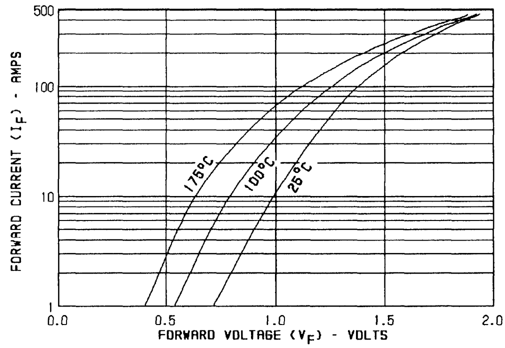


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

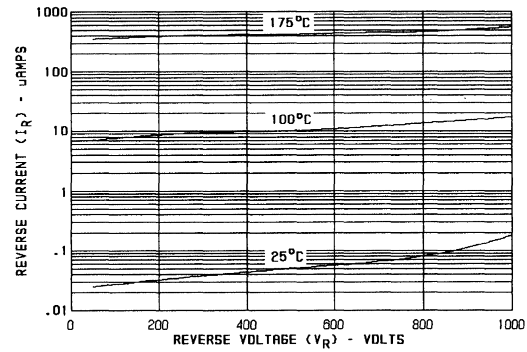


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

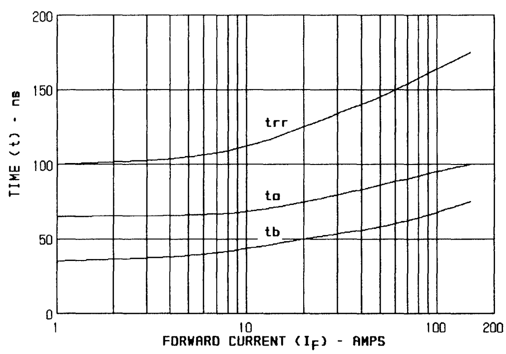


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

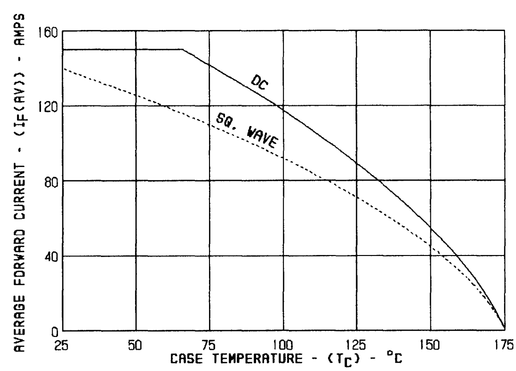


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

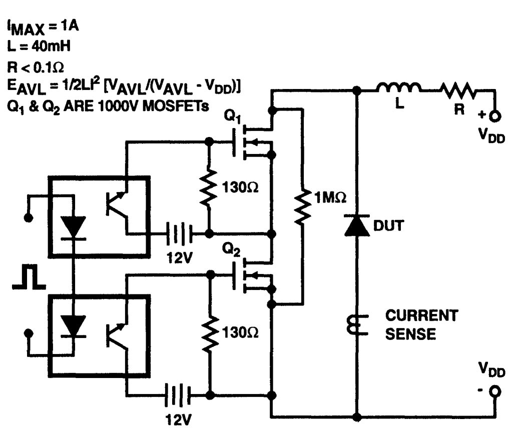


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

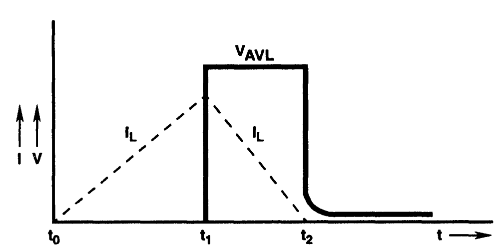


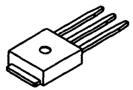
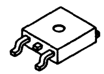
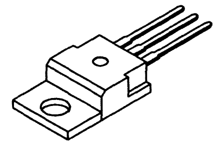
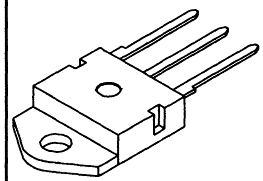
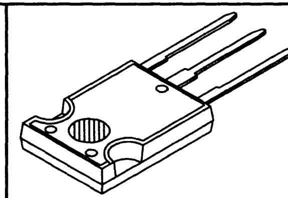
FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

MCT/IGBT/DIODES 6

ULTRAFAST DUAL DIODES

Ultrafast Dual Diodes (Continued)

HARRIS DUAL ULTRA-FAST RECOVERY RECTIFIER PRODUCT LINE

	 TO-251AA		 TO-252AA		 TO-220AB			 TO-218AC		 TO-247	
	$I_{F(AVG)}$		$I_{F(AVG)}$		$I_{F(AVG)}$			$I_{F(AVG)}$		$I_{F(AVG)}$	
V_{RRM}	4Ax2	6Ax2	4Ax2	6Ax2	4Ax2	6Ax2	8Ax2	15Ax2	30Ax2	15Ax2	30Ax2
100V	*RURD410CC* 1.0V 35ns	*RURD610CC* 1.0V 35ns	*RURD410CCS* 1.0V 35ns	*RURD610CCS* 1.0V 35ns			BYW51100 0.95V 35ns† MUR1610CT RURP810CC 0.975V 35ns	MUR3010PT RURH1510CC 1.05V 35ns	RURH3010CC 1.0V 50ns	RURG1510CC 1.05V35ns	RURG3010CC 1.0V 50ns
150V	*RURD415CC* 1.0V 35ns	*RURD615CC* 1.0V 35ns	*RURD415CCS* 1.0V 35ns	*RURD615CCS* 1.0V 35ns			BYW51150 0.95V 35ns† MUR1615CT RURP815CC 0.975V 35ns	MUR3015PT RURH1515CC 1.05V 35ns	RURH3015CC 1.0V 50ns	RURG1515CC 1.05V35ns	RURG3015CC 1.0V 50ns
200V	*RURD420CC* 1.0V 35ns	*RURD620CC* 1.0V 35ns	*RURD420CCS* 1.0V 35ns	*RURD620CCS* 1.0V 35ns			BYW51200 0.95V 35ns† MUR1620CT RURP820CC 0.975V 35ns	MUR3020PT RURH1520CC 1.05V 35ns	RURH3020CC 1.0V 50ns	RURG1520CC 1.05V35ns	RURG3020CC 1.0V 50ns
400V	*RURD440CC* 1.5V 60ns		*RURD440CCS* 1.5V 60ns			*RURP640CC* 1.5V 60ns	RURP840CC 1.3V 70ns	MUR3040PT RURH1540CC 1.25V 60ns	RURH3040CC 1.5V 60ns	RURG1540CC 1.5V60ns	RURG3040CC 1.5V 60ns
500V	*RURD450CC* 1.5V 60ns		*RURD450CCS* 1.5V 60ns			*RURP650CC* 1.5V 60ns	RURP850CC 1.5V 70ns	MUR3050PT RURH1550CC 1.25V 60ns	RURH3050CC 1.5V 60ns	RURG1550CC 1.5V 60ns	RURG3050CC 1.5V 60ns
600V	*RURD460CC* 1.5V 60ns		*RURD4460CCS* 1.5V 60ns			*RURP660CC* 1.5V 60ns	RURP860CC 1.5V 70ns	MUR3060PT RURH1560CC 1.25V 60ns	RURH3060CC 1.5V 60ns	RURG1560CC 1.5V 60ns	RURG3060CC 1.5V 60ns
700V							RURP870CC 1.8V 110ns	RURH1570CC 1.8V 125ns	RURH3070CC 1.8V 150ns	RURG1570CC 1.5V 125ns	RURG3070CC 1.5V 150ns
800V							RURP880CC 1.8V 110ns	RURH1580CC 1.8V 125ns	RURH3080CC 1.8V 150ns	RURG1580CC 1.5V 125ns	RURG3080CC 1.5V 150ns
900V							RURP890CC 1.8V 110ns	RURH1590CC 1.8V 125ns	RURH3090CC 1.8V 150ns	RURG1590CC 1.5V 125ns	RURG3090CC 1.5V 150ns
1000V							RURP8100CC 1.8V 110ns	RURH15100CC 1.8V 125ns	RURH30100CC 1.8V 150ns	RURG15100CC 1.5V 125ns	RURG30100CC 1.5V 150ns
1200V					*RURP4120CC* 2.1V 90ns	*RURP6120CC* 2.1V 90ns	RURP8120CC 2.1V 110ns			RURG15120CC 2.1V 130ns	RURG30120CC 2.1 150ns

ITALICS = Future Product Offerings; V_F at $I_{F(AVG)}$, $T_J = 25^oC$; T_{RR} at $I_{F(AVG)}$, $dI_F/dt = 100A/\mu sec$ $T_J = 25^oC$; † T_{RR} at $I_F = 1A$.

BYW51-100, BYW51-150, BYW51-200

June 1995

8A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultra Fast Recovery Time (<35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Planar Design
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Full-Wave Rectification

Description

The BYW51 series devices are low forward voltage drop, ultra-fast-recovery rectifiers (t_{RR} < 35ns). They use a planar ion-implanted epitaxial construction.

These devices are intended for use as output rectifiers and fly-wheel diodes in a variety of high-frequency pulse-width-modulated and switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

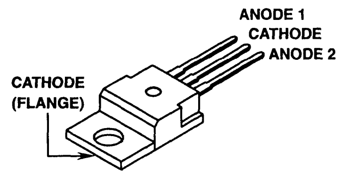
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
BYW51-100	TO-220AB	BYW51100
BYW51-150	TO-220AB	BYW51150
BYW51-200	TO-220AB	BYW51200

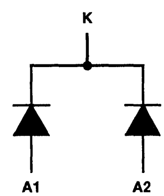
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings Per Junction

	BYW51-100	BYW51-150	BYW51-200	UNITS
Maximum Peak Repetitive Reverse Voltage . . . . V_{RRM}	100	150	200	V
Maximum Peak Surge Voltage . . . . V_{RSM}	110	165	220	V
Repetitive Peak Surge Current . . . . I_{FRM}, t_P < 10μs	100	100	100	A
Nonrepetitive Peak Surge Current . . . . I_F(RMS), Total	20	20	20	A
Average Rectified forward Current . . . . $I_{F(AV)}$, Total T_C = +125°C, a = 0.5	8	8	8	A
Repetitive Peak Surge Current . . . . I_{FSM} t_P = 10ms, Sinusoidal	100	100	100	A
Maximum Power Dissipation . . . . P_D, T_C = +125°C	20	20	20	W
Operating and Storage Temperature . . . . T_J	-40 + 150	-40 + 150	-40 + 150	°C
T_L (Lead Temperature During Soldering) . . . . At Distance > 1/8 in. (3.17mm) From Case For 10s max.	260	260	260	°C

Electrical Specifications Per Junction

SYMBOL	TEST CONDITIONS			LIMITS						UNITS
	T_J °C	VOLTAGE V_R V	CURRENT i_F A	BYW51-100		BYW51-150		BYW51-200		
				MIN	MAX	MIN	MAX	MIN	MAX	
I_R	25	100	-	-	5	-	-	-	-	μA
		150	-	-	-	-	5	-	-	μA
		200	-	-	-	-	-	-	5	μA
	100	100	-	-	1	-	-	-	-	mA
		150	-	-	-	-	1	-	-	mA
		200	-	-	-	-	-	-	1	mA
V_F	25	-	8	-	0.95	-	0.95	-	0.95	V
	100	-	8	-	0.89	-	0.89	-	0.89	V
t_{RR}	25	-	1 (Note 1)	-	35	-	35	-	35	ns
$R_{\theta JC}$, Per Leg		-	-	-	2.5	-	2.5	-	2.5	°C/W
$R_{\theta JC}$, Total		-	-	-	1.3	-	1.3	-	1.3	°C/W
$R_{\theta JA}$		-	-	-	60	-	60	-	60	°C/W
C_J	25	10	0	All types (typ.) 40						pF

NOTE:

1. $dI_F/dt > 50A/\mu s$, $I_{RM}(rec) < 1A$, $I_{RR} = 0.25A$.

Typical Performance Curves

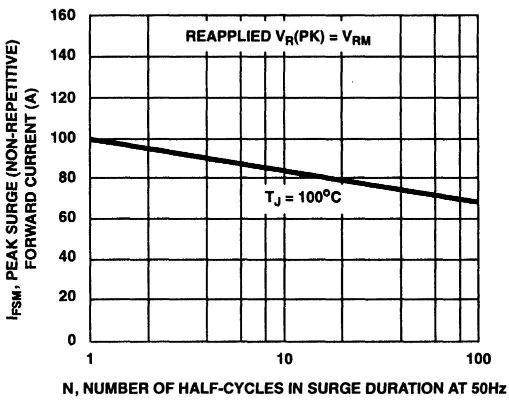


FIGURE 1. PEAK SURGE FORWARD CURRENT vs SURGE DURATION

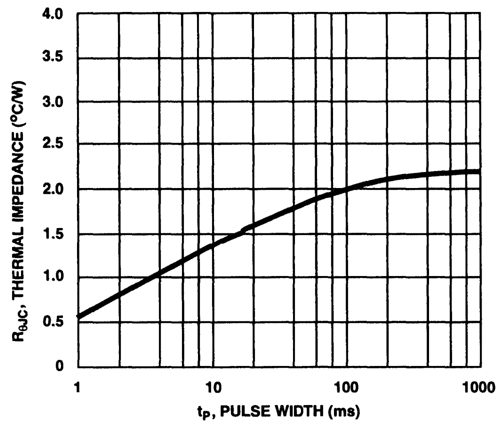


FIGURE 2. THERMAL IMPEDANCE vs PULSE WIDTH (PER JUNCTION)

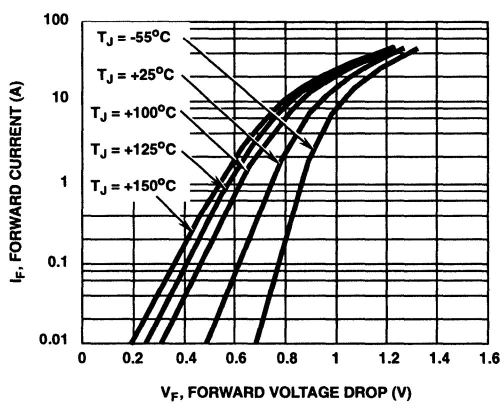


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

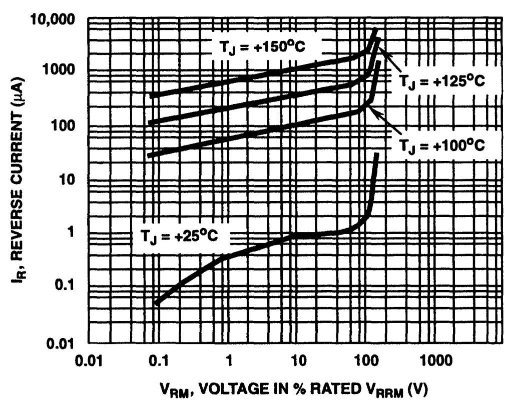


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

6

ULTRAFAST DUAL DIODES

HARRIS SEMICONDUCTOR

MUR1610CT, MUR1615CT, MUR1620CT, RURP810CC, RURP815CC, RURP820CC

June 1995

8A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery .... <25ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The MUR1610CT, MUR1615CT, MUR1620CT, RURP810CC, RURP815CC and RURP820CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 25ns). They have low forward voltage drop and are silicon nitride passivated ionimplanted epitaxial planar construction.

These devices are intended for use as freewheeling/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGE AVAILABILITY

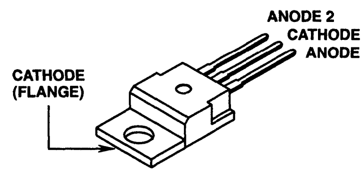
PART NUMBER	PACKAGE	BRAND
MUR1610CT	TO-220AB	MUR1610C
MUR1615CT	TO-220AB	MUR1615C
MUR1620CT	TO-220AB	MUR1620C
RURP810CC	TO-220AB	RURP810C
RURP815CC	TO-220AB	RURP815C
RURP820CC	TO-220AB	RURP820C

NOTE: When ordering, use the entire part number.

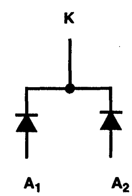
Formerly developmental type TA09224.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		MUR1610CT RURP810CC	MUR1615CT RURP815CC	MUR1620CT RURP820CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	100	150	200	V
Working Peak Reverse Voltage	V_{RWM}	100	150	200	V
DC Blocking Voltage	V_R	100	150	200	V
Average Rectified Forward Current (T_C = +157°C)	$I_{F(AV)}$	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	A
Maximum Power Dissipation	P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MUR1610CT RURP810CC			MUR1615CT RURP815CC			MUR1620CT RURP820CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A, T_C = +25°C	-	-	0.975	-	-	0.975	-	-	0.975	V
	I_F = 8A, T_C = +150°C	-	-	0.895	-	-	0.895	-	-	0.895	V
I_R	V_R = 100V, T_C = +25°C	-	-	100	-	-	-	-	-	-	µA
	V_R = 150V, T_C = +25°C	-	-	-	-	-	100	-	-	-	µA
	V_R = 200V, T_C = +25°C	-	-	-	-	-	-	-	-	100	µA
I_R	V_R = 100V, T_C = +150°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V, T_C = +150°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V, T_C = +150°C	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	25	-	-	25	-	-	25	ns
	I_F = 8A, dI_F/dt = 200A/µs	-	-	30	-	-	30	-	-	30	ns
t_A	I_F = 8A, dI_F/dt = 200A/µs	-	13	-	-	13	-	-	13	-	ns
t_B	I_F = 8A, dI_F/dt = 200A/µs	-	5	-	-	5	-	-	5	-	ns
Q_{RR}	I_F = 8A, dI_F/dt = 200A/µs	-	25	-	-	25	-	-	25	-	nC
C_J	V_R = 10V, I_F = 0A	-	60	-	-	60	-	-	60	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current .
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled Avalanche Energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

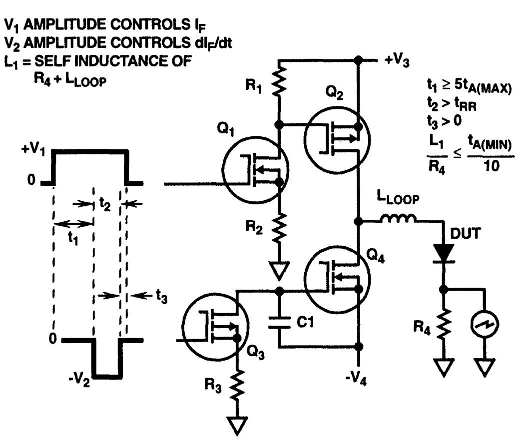


FIGURE 1. t_{RR} TEST CIRCUIT

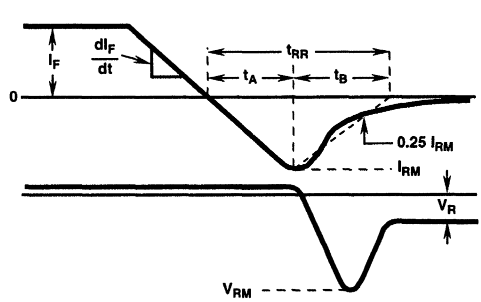


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

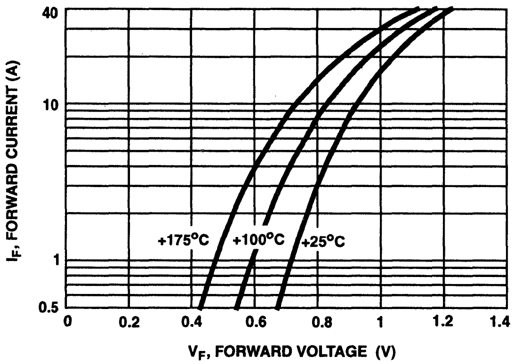


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

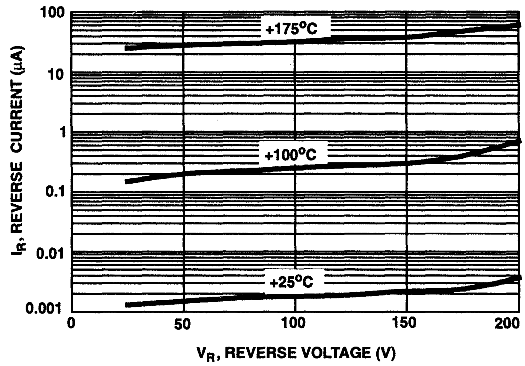


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

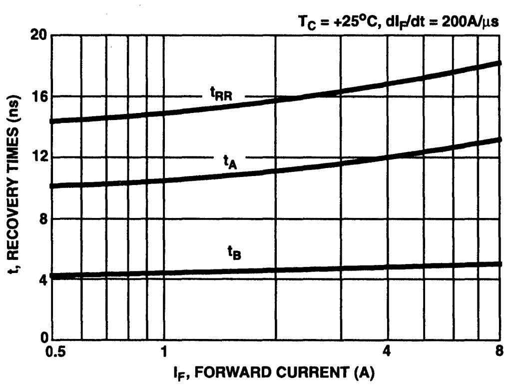


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

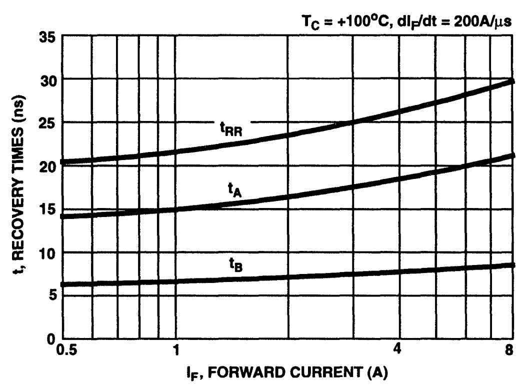


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

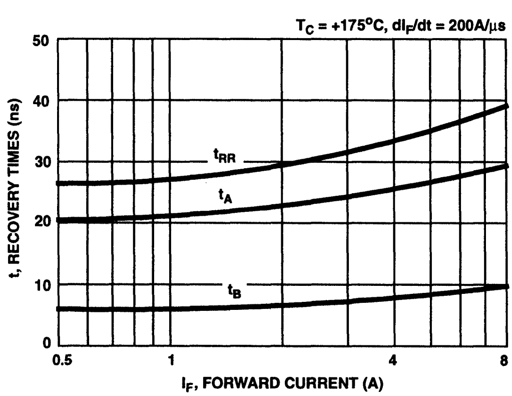


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

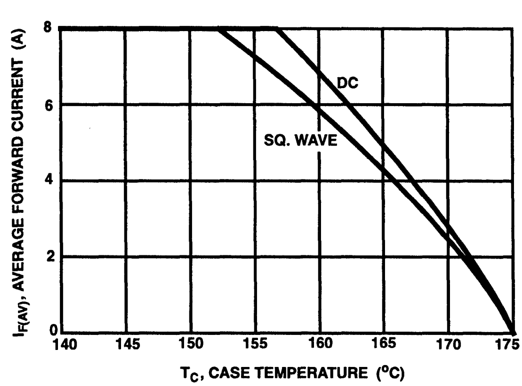


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

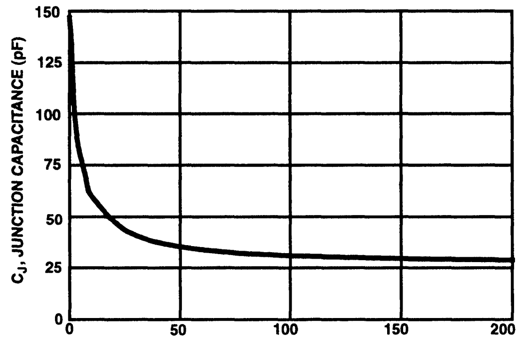


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

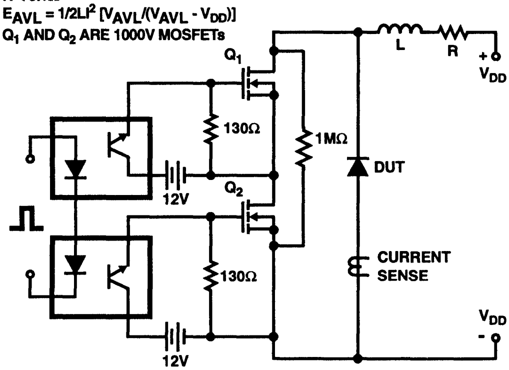


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

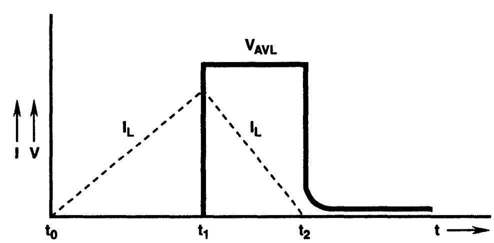


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

MUR3010PT, RURH1510CC, MUR3015PT, RURH1515CC, MUR3020PT, RURH1520CC

April 1995

15A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 30ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

MUR3010PT, MUR3015PT, MUR3020PT and RURH1510CC, RURH1515CC, RURH1520CC are ultrafast dual diodes (t_{RR} < 30ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

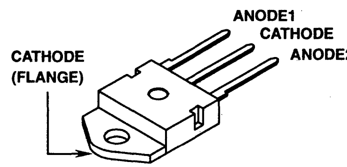
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR3010PT	TO-218AC	MUR3010PT
RURH1510CC	TO-218AC	RURH1510C
MUR3015PT	TO-218AC	MUR3015PT
RURH1515CC	TO-218AC	RURH1515C
MUR3020PT	TO-218AC	MUR3020PT
RURH1520CC	TO-218AC	RURH1520C

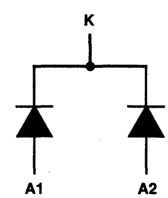
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		MUR3010PT RURH1510CC	MUR3015PT RURH1515CC	MUR3020PT RUR1520CC
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Total device forward current at rated V_R and $T_C = 150^oC$)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

File Number **2775.4**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR3010PT, RURH1510CC			MUR3015PT, RURH1515CC			MUR3020PT, RURH1520CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
	I_F = 15A, T_C = +25°C	-	-	1.05	-	-	1.05	-	-	1.05	V
IR at T_C = +150°C	V_R = 100V	-	-	500	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	500	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	500	µA
IR at T_C = +25°C	V_R = 100V	-	-	100	-	-	-	-	-	-	µA
	V_R = 150V	-	-	-	-	-	100	-	-	-	µA
	V_R = 200V	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	30	-	-	30	-	-	30	ns
	I_F = 15A	-	-	35	-	-	35	-	-	35	ns
t_A	I_F = 1A	-	18	-	-	18	-	-	18	-	ns
	I_F = 15A	-	20	-	-	20	-	-	20	-	ns
t_B	I_F = 1A	-	9	-	-	9	-	-	9	-	ns
	I_F = 15A	-	10	-	-	10	-	-	10	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}	see Fig. 7, 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

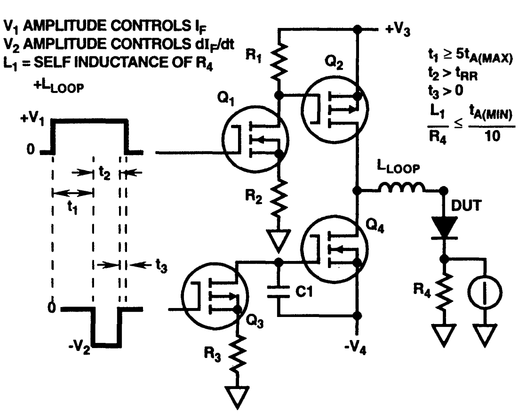


FIGURE 1. t_{RR} TEST CIRCUIT

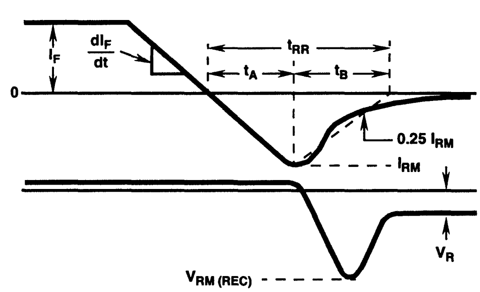


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

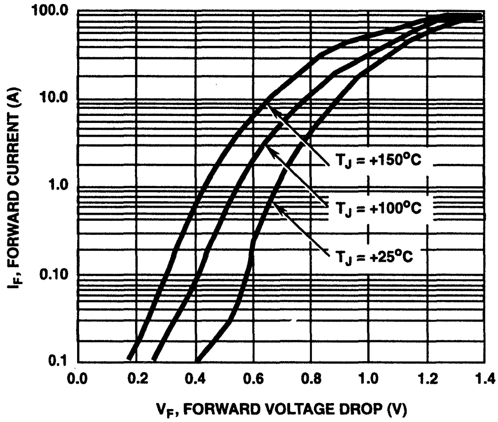


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

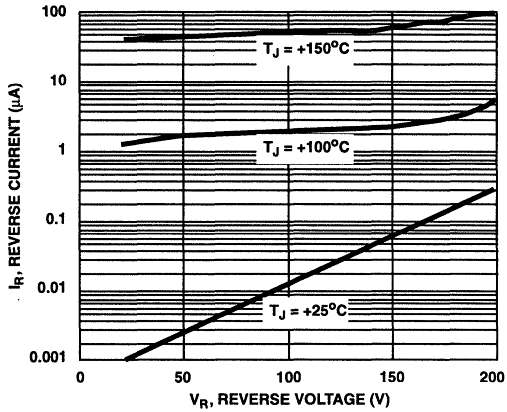


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

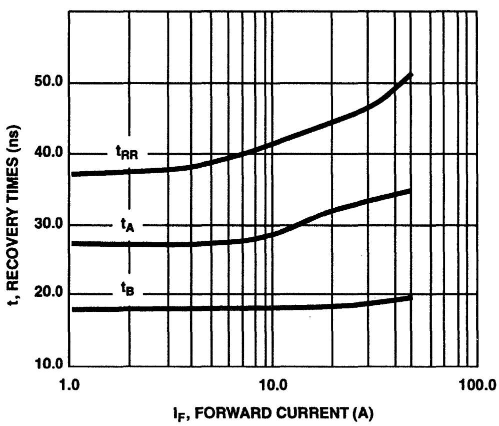


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

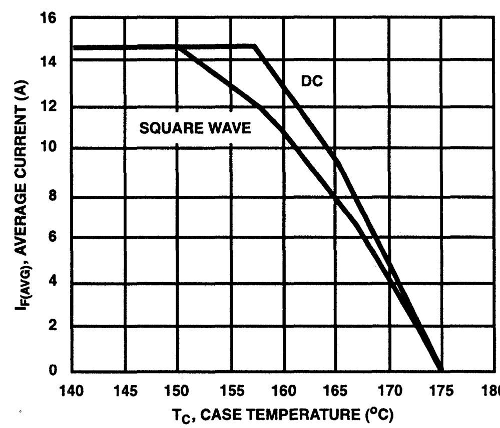


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

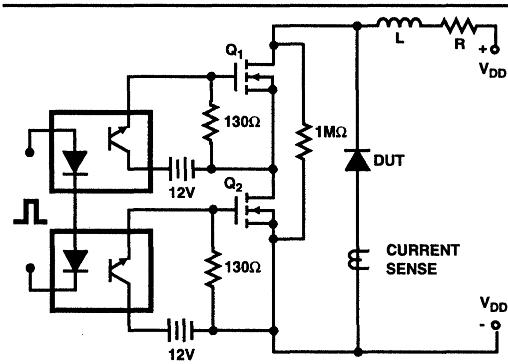


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

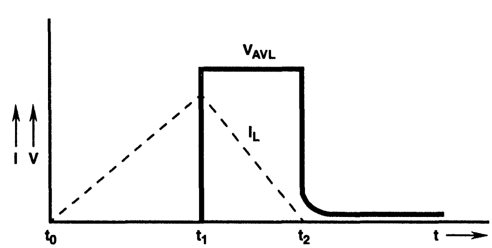


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_{L\ PEAK}$ = 1A, L = 40mH, R < 0.1W, $E_{AVL} = 1/2LI^2\ [V_{AVL}/(V_{AVL} - V_{DD})]$

HARRIS SEMICONDUCTOR

MUR3040PT, RURH1540CC, MUR3050PT, RURH1550CC, MUR3060PT, RURH1560CC

April 1995

15A, 400V - 600V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

MUR3040PT, MUR3050PT, MUR3060PT and RURH1540CC, RURH1550CC, RURH1560CC are ultrafast dual diodes (t_{RR} < 55ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial constructiodn.

These devices are intended for use as energy steering/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

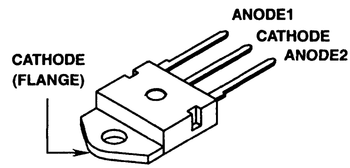
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
MUR3040PT	TO-218AC	MUR3040PT
RURH1540CC	TO-218AC	RURH1540C
MUR3050PT	TO-218AC	MUR3050PT
RURH1550CC	TO-218AC	RURH1550C
MUR3060PT	TO-218AC	MUR3060PT
RURH1560CC	TO-218AC	RURH1560C

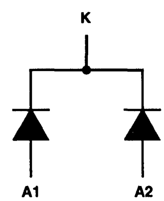
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		MUR3040PT RURH1540CC	MUR3050PT RURH1550CC	MUR3060PT RURH1560CC
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	42	42	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1phase 60Hz)	I_{FSM}	200A	200A	200A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

File Number 2774.3

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		MUR3040PT, RURH1540CC			MUR3050PT, RURH1550CC			MUR3060PT, RURH1560CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +150°C	-	-	1.12	-	-	1.20	-	-	1.20	V
	I_F = 15A, T_C = +25°C	-	-	1.25	-	-	1.50	-	-	1.50	V
IR at T_C = +150°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
IR at T_C = +25°C	V_R = 400V	-	-	100	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	100	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 15A	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 15A	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 15A	-	17	-	-	17	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}	see Fig. 7, 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

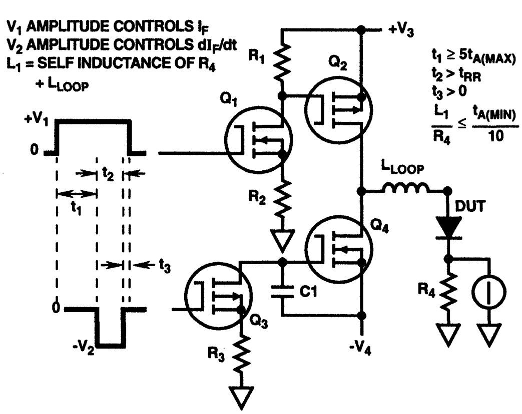


FIGURE 1. t_{RR} TEST CIRCUIT

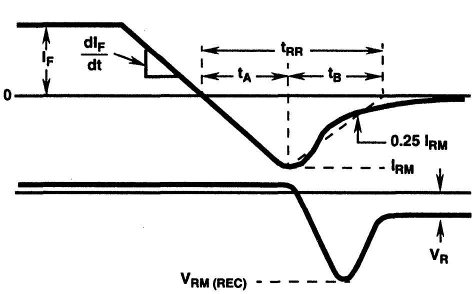


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

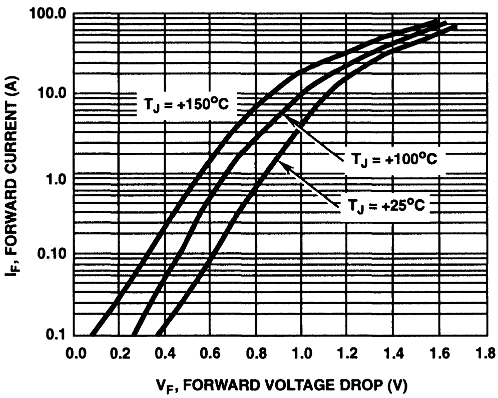


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

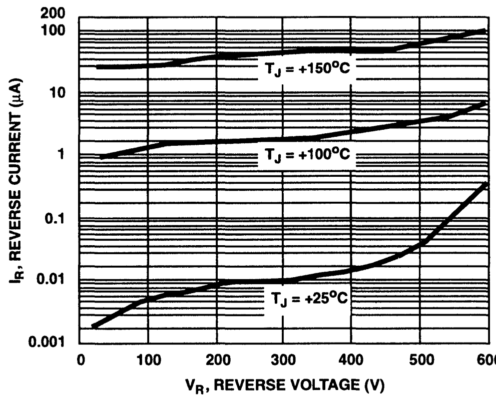


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

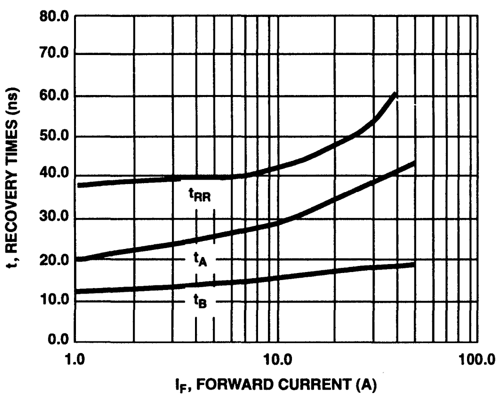


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

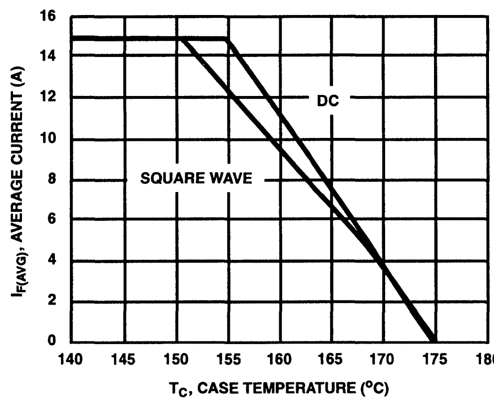


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

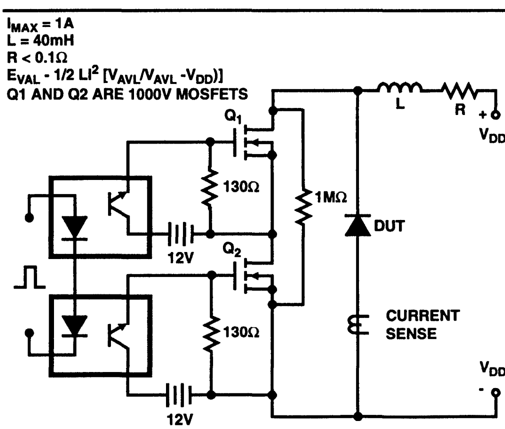


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

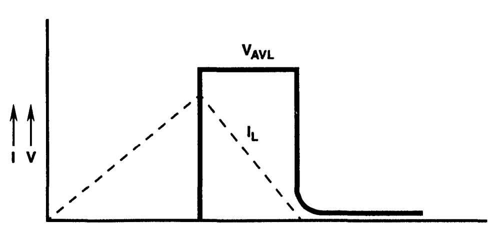


FIGURE 8. CURRENT VOLTAGE WAVEFORM

HARRIS SEMICONDUCTOR

RURG1510CC, RURG1515CC, RURG1520CC

April 1995

15A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <30ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG1510CC, RURG1515CC and RURG1520CC (TA9926) are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 30ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

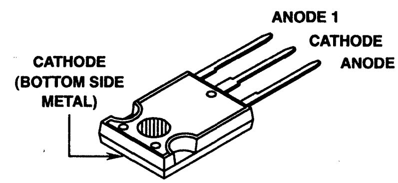
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG1510CC	TO-247	RURG1510C
RURG1515CC	TO-247	RURG1510C
RURG1520CC	TO-247	RURG1510C

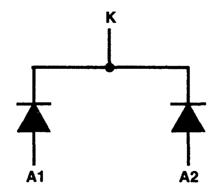
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C

	RURG1510CC	RURG1515CC	RURG1520CC	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	100	150	200	V
Working Peak Reverse Voltage . . . . V_{RWM}	100	150	200	V
DC Blocking Voltage . . . . V_R	100	150	200	V
Average Rectified Forward Current (Per Leg) . . . . $I_{F(AV)}$ (T_C = +145°C)	15	15	15	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	30	30	30	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	200	200	200	A
Maximum Power Dissipation . . . . P_D	100	100	100	W
Avalanche Energy . . . . E_{AVL} (L = 40mH)	20	20	20	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number 3551.2

Electrical Specifications
T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RURG1510CC LIMITS			RURG1515CC LIMITS			RURG1520CC LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A		-	-	1.05	-	-	1.05	-	-	1.05	V
V_F	I_F = 15A	T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
I_R	V_R = 100V		-	-	100	-	-	-	-	-	-	μA
	V_R= 150V		-	-	-	-	-	100	-	-	-	μA
	V_R = 200V		-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 100V	T_C = +150°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 150V	T_C = +150°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 200V	T_C = +150°C	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	30	-	-	30	-	-	30	ns
t_{RR}	I_F = 15A, dI_F/dt = 100A/μs		-	-	35	-	-	35	-	-	35	ns
t_A	I_F = 15A, dI_F/dt = 100A/μs		-	20	-	-	20	-	-	20	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/μs		-	10	-	-	10	-	-	10	-	ns
$R_{\theta JC}$			-	-	1.5	-	-	1.5	-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

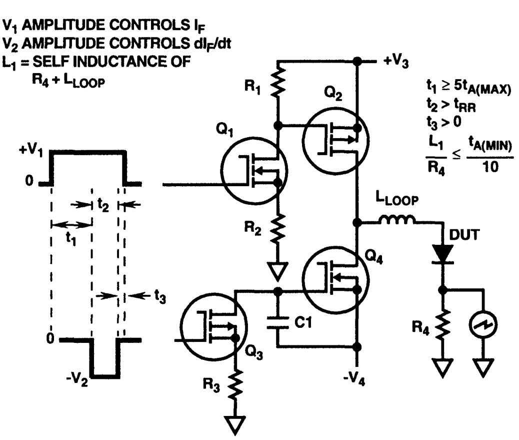


FIGURE 1. t_{RR} TEST CIRCUIT

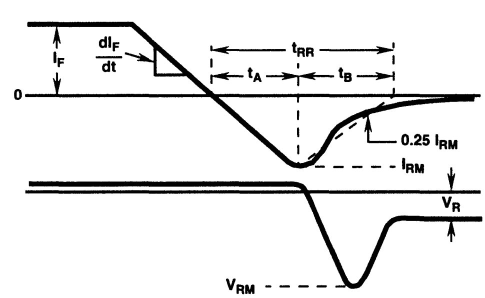


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

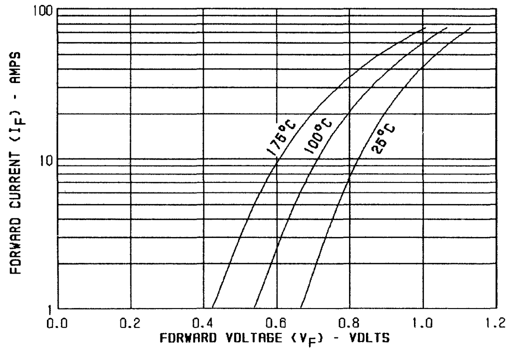


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

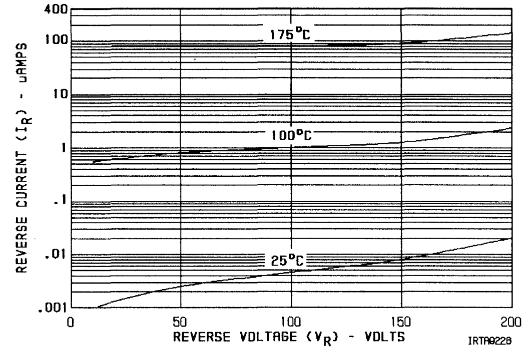


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

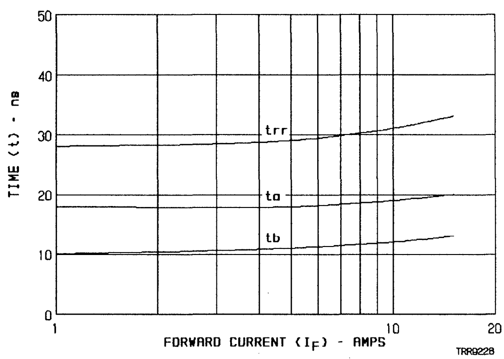


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

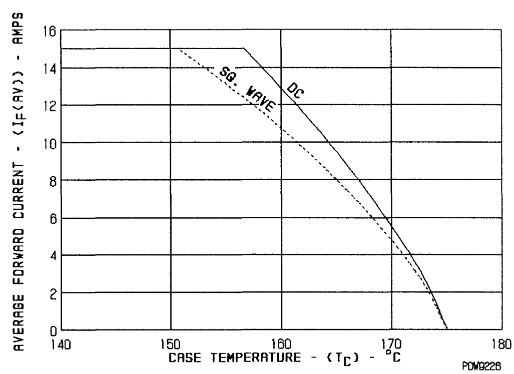


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

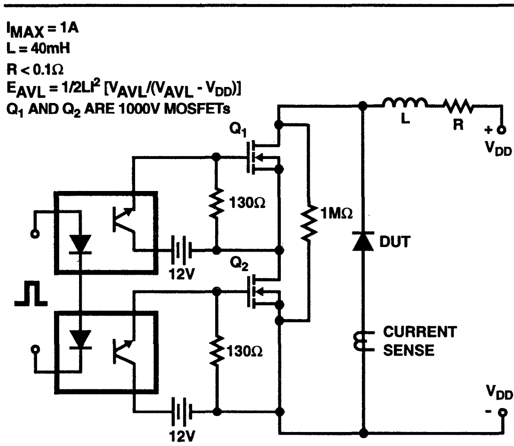


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

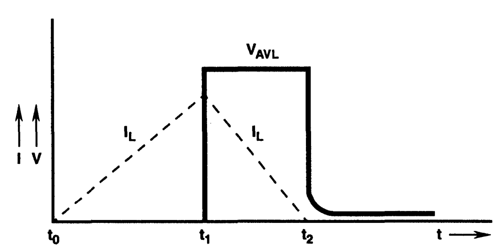


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG1540CC, RURG1550CC, RURG1560CC

April 1995

15A, 400V - 600V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG1540CC, RURG1550CC and RURG1560CC (TA9905) are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

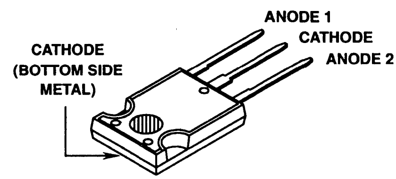
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG1540CC	TO-247	RURG1540C
RURG1550CC	TO-247	RURG1550C
RURG1560CC	TO-247	RURG1560C

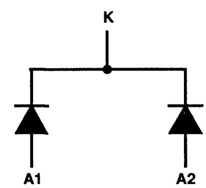
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RURG1540CC	RURG1550CC	RURG1560CC
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Per Leg) ($T_C = +145^oC$)	$I_{F(AV)}$	15A	15A	15A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30A	30A	30A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200A	200A	200A
Maximum Power Dissipation	P_D	100W	100W	100W
Avalanche Energy (L = 40mH)	E_{AVL}	20mj	20mj	20mj
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

File Number **3548.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURG1540CC LIMITS			RURG1550CC LIMITS			RURG1560CC LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A	-	-	1.5	-	-	1.5	-	-	1.5	V
V_F	I_F = 15A, T_C = +150°C	-	-	1.3	-	-	1.3	-	-	1.3	V
I_R	V_R = 400V	-	-	100	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	100	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	100	µA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	55	-	-	55	-	-	55	ns
t_{RR}	I_F = 15A, dI_F/dt = 100A/µs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 15A, dI_F/dt = 100A/µs	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/µs	-	17	-	-	17	-	-	17	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

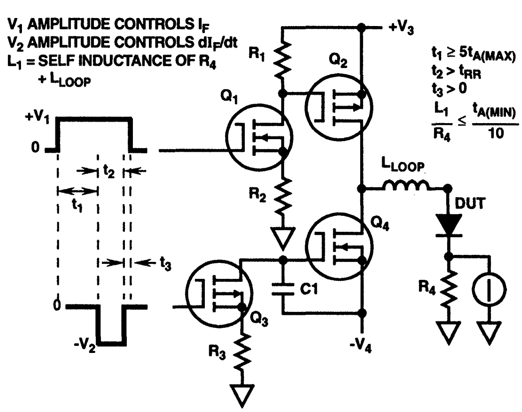


FIGURE 1. t_{RR} TEST CIRCUIT

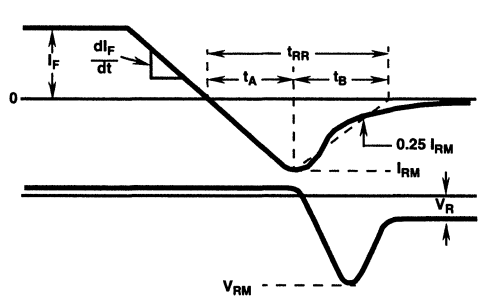


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

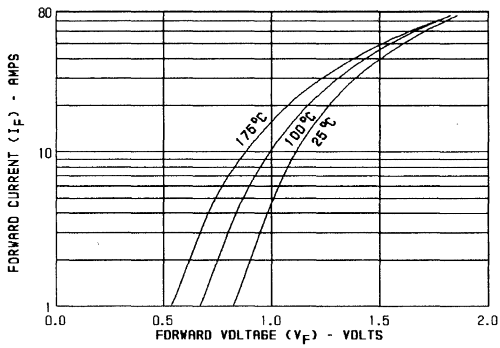


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

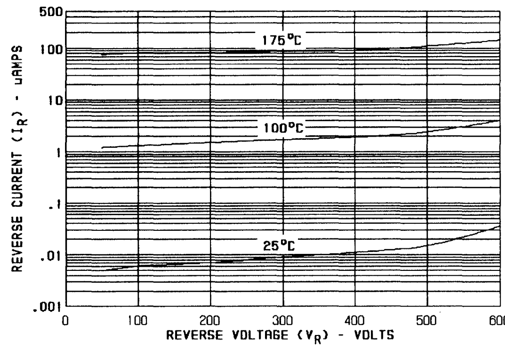


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

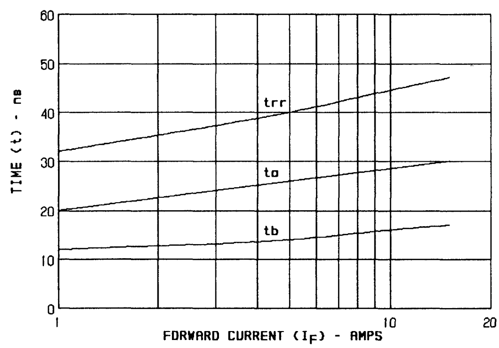


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

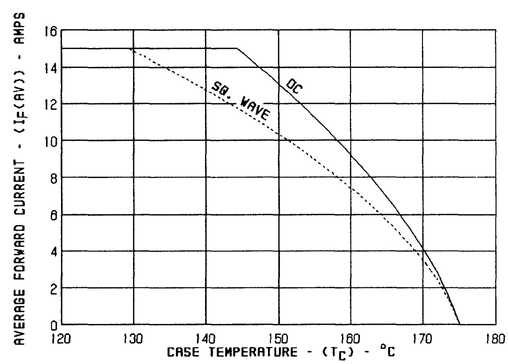


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

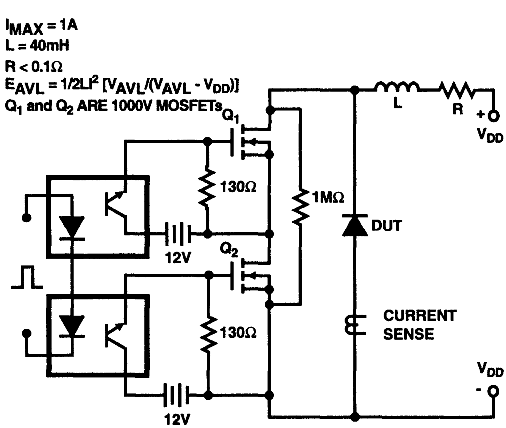


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

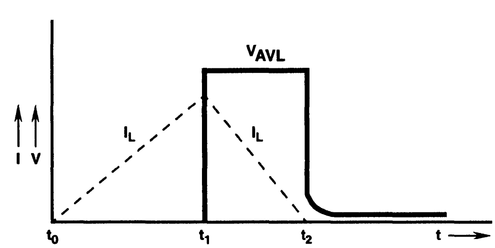


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG1570CC, RURG1580CC, RURG1590CC, RURG15100CC

April 1995

15A, 700V - 1000V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <100ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG1570CC, RURG1580CC, RURG1590CC and RUR15100CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 100ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheel/clamping diode and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

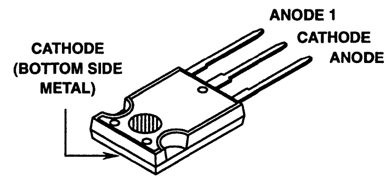
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG1570CC	TO-247	RURG1570C
RURG1580CC	TO-247	RURG1580C
RURG1590CC	TO-247	RURG1590C
RURG15100CC	TO-247	URG15100C

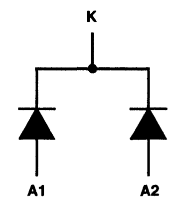
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG1570CC	RURG1580CC	RURG1590CC	RURG15100CC
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current (Per Leg) (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	15A	15A	15A	15A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHZ)	I_{FRM}	30A	30A	30A	30A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	200A	200A	200A	200A
Maximum Power Dissipation	P_D	100W	100W	100W	100W
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURG1570CC			RURG1580CC			RURG1590CC			RURG15100CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	I_F = 15A T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at T_C = +150°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +25°C	V_R = 700V	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	100	-	-	100	-	-	100	-	-	100	ns
	I_F = 15A	-	-	125	-	-	125	-	-	125	-	-	125	ns
t_A	I_F = 15A	-	75	-	-	75	-	-	75	-	-	75	-	ns
t_B	I_F = 15A	-	40	-	-	40	-	-	40	-	-	40	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}		-	-	20	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

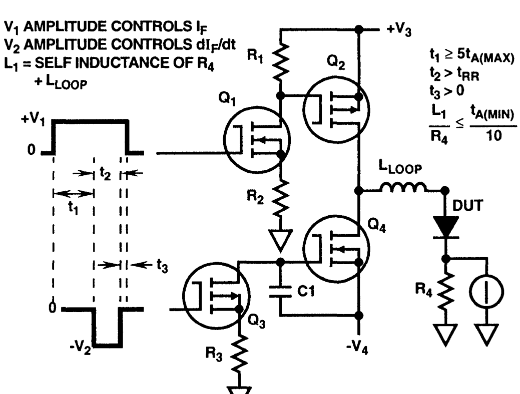


FIGURE 1. t_{RR} TEST CIRCUIT

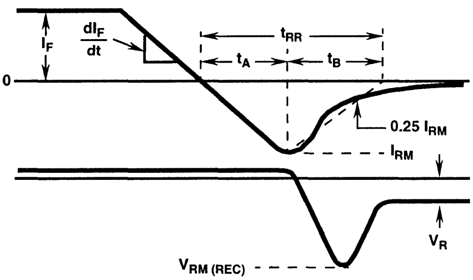


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

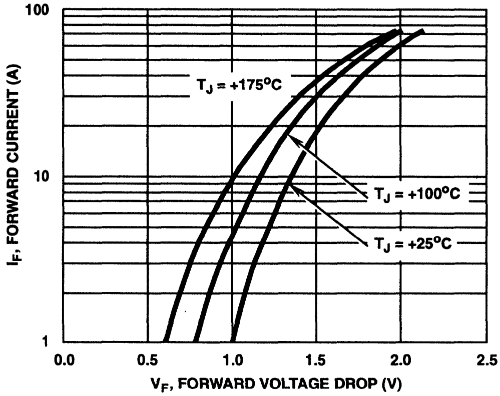


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

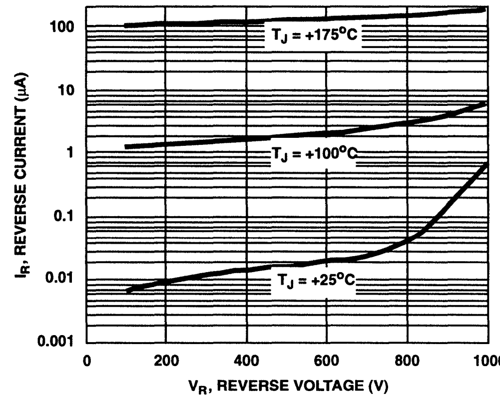


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

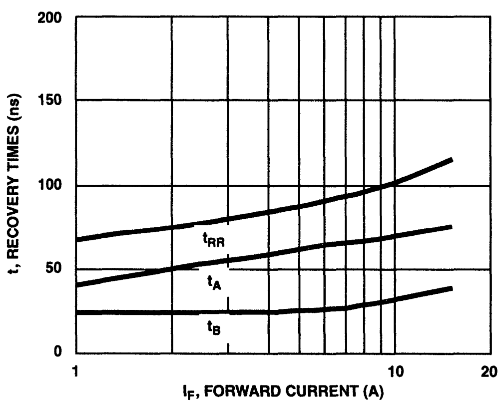


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

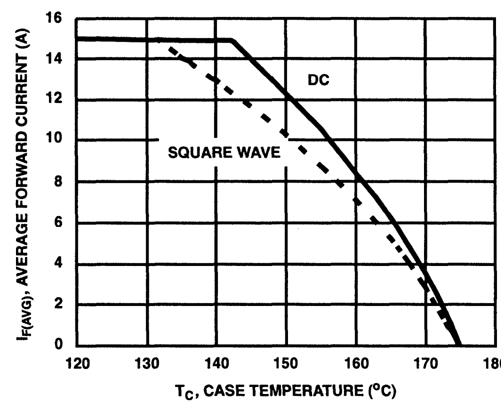


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

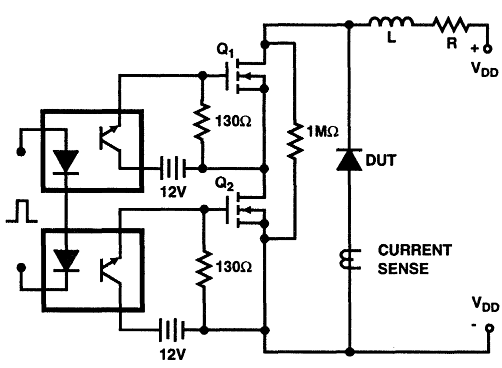


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

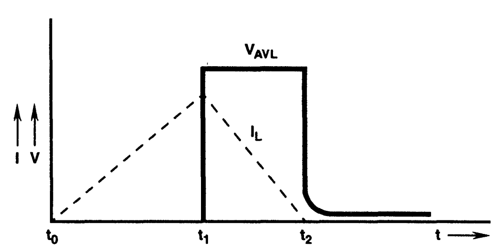


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2)\ LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$

Q1 AND Q2 ARE 1000V MOSFETs

HARRIS SEMICONDUCTOR

RURG15120CC

April 1995

15A, 1200V Ultrafast Dual Diode

Features

- Ultrafast with Soft Recovery . . . . <100ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURG15120CC (TA49097) are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 100ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

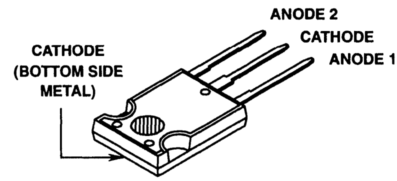
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG15120CC	TO-247	URG15120C

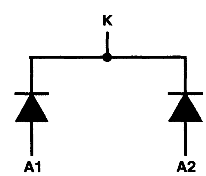
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RURG15120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	200	A
Maximum Power Dissipation	P_D	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3695.1**

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 15A, T_C = +25°C	-	-	2.1	V
	I_F = 15A, T_C = +150°C	-	-	1.9	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	100	ns
	I_F = 15A, dI_F/dt = 100A/µs	-	-	130	ns
t_A	I_F = 15A, dI_F/dt = 100A/µs	-	65	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/µs	-	40	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/µs	-	400	-	nC
C_J	V_R = 10V, I_F = 0A	-	56	-	pF
$R_{\theta JC}$		-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

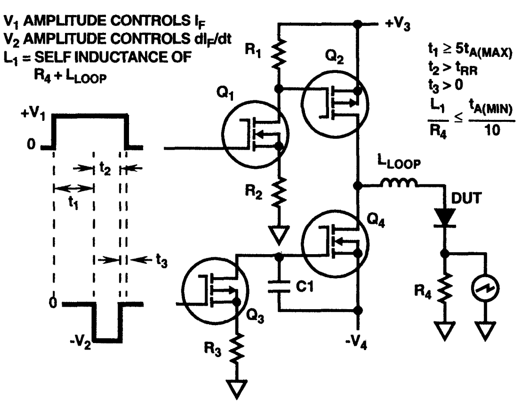


FIGURE 1. t_{RR} TEST CIRCUIT

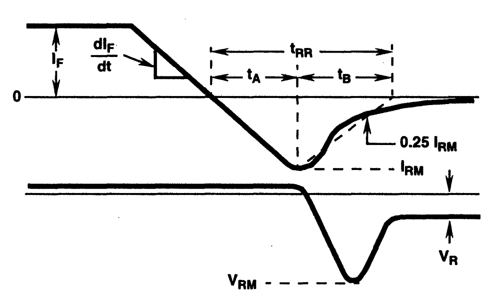


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

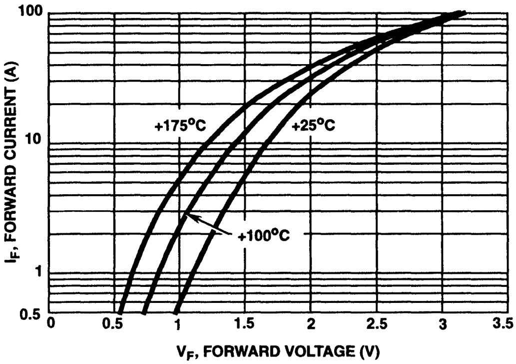


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

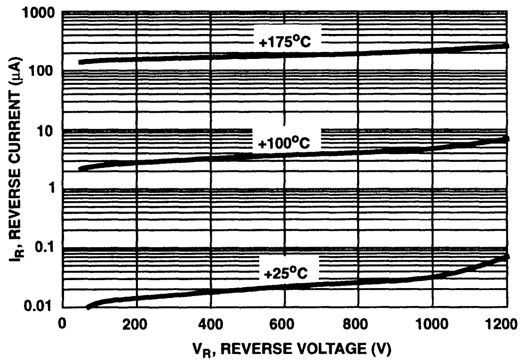


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

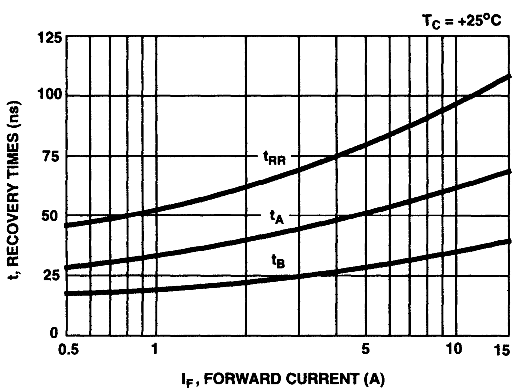


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

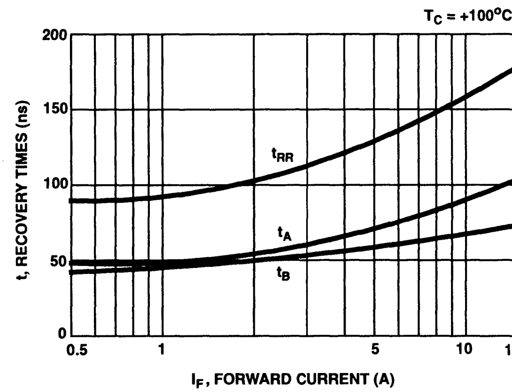


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

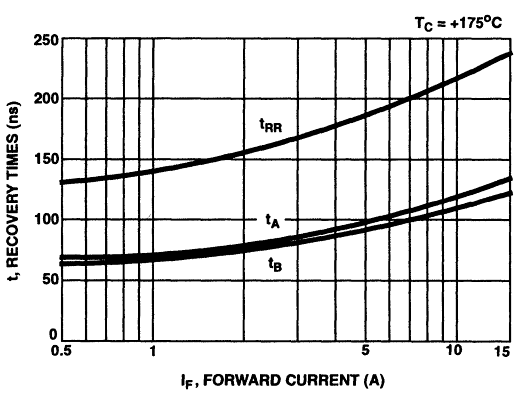


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

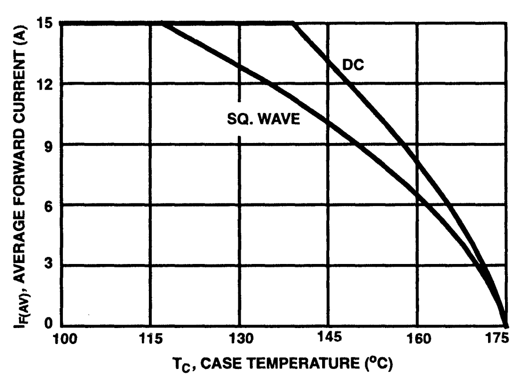


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

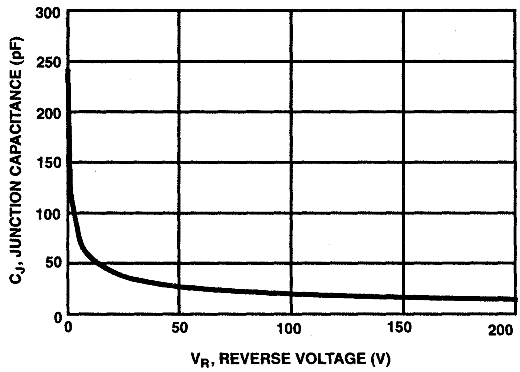


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

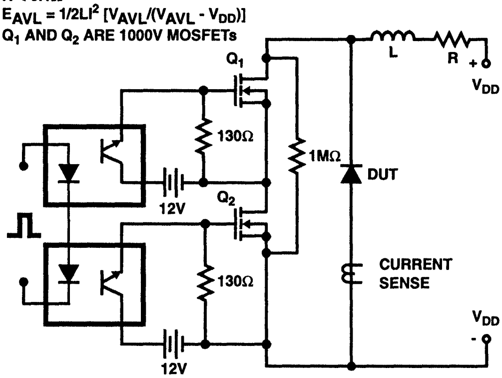


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

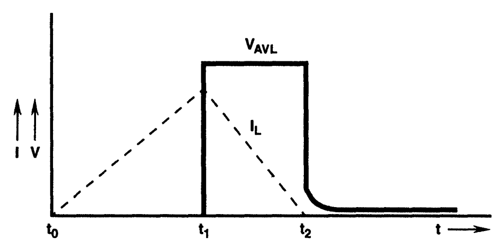


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RURG3010CC, RURG3015CC, RURG3020CC

HARRIS SEMICONDUCTOR

April 1995

30A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <45ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3010CC, RURG3015CC and RURG3020CC (TA9645) are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 45ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

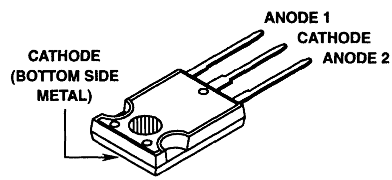
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3010CC	TO-247	RURG3010C
RURG3015CC	TO-247	RURG3015C
RURG3020CC	TO-247	RURG3020C

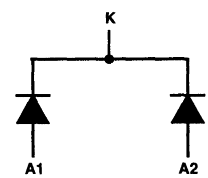
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



6

ULTRAFAST DUAL DIODES

Absolute Maximum Ratings $T_C = +25^oC$

	RURG3010CC	RURG3015CC	RURG3020CC	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	100	150	200	V
Working Peak Reverse Voltage . . . . V_{RWM}	100	150	200	V
DC Blocking Voltage . . . . V_R	100	150	200	V
Average Rectified Forward Current (Per Leg) . . . . $I_{F(AV)}$ ($T_C = +145^oC$)	30	30	30	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	70	70	70	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	325	325	325	A
Maximum Power Dissipation . . . . P_D	125	125	125	W
Avalanche Energy . . . . E_{AVL} (L = 40mH)	20	20	20	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3552.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RURG3010CC LIMITS			RURG3015CC LIMITS			RURG3020CC LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A		-	-	1.0	-	-	1.0	-	-	1.0	V
V_F	I_F = 30A	T_C = +150°C	-	-	0.85	-	-	0.85	-	-	0.85	V
I_R	V_R = 100V		-	-	500	-	-	-	-	-	-	μA
	V_R= 150V		-	-	-	-	-	500	-	-	-	μA
	V_R = 200V		-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 100V	T_C = +150°C	-	-	100	-	-	-	-	-	-	mA
	V_R = 150V	T_C = +150°C	-	-	-	-	-	100	-	-	-	mA
	V_R = 200V	T_C = +150°C	-	-	-	-	-	-	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	45	-	-	45	-	-	45	ns
t_{RR}	I_F = 30A, dI_F/dt = 100A/μs		-	-	50	-	-	50	-	-	50	ns
t_A	I_F = 30A, dI_F/dt = 100A/μs		-	20	-	-	20	-	-	20	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/μs		-	15	-	-	15	-	-	15	-	ns
$R_{\theta JC}$			-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

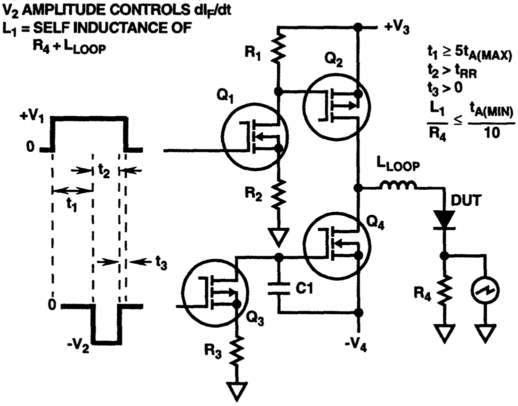


FIGURE 1. t_{RR} TEST CIRCUIT

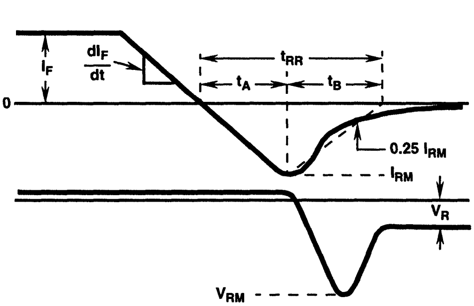


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

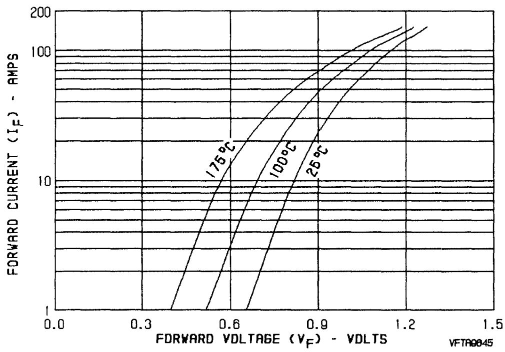


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

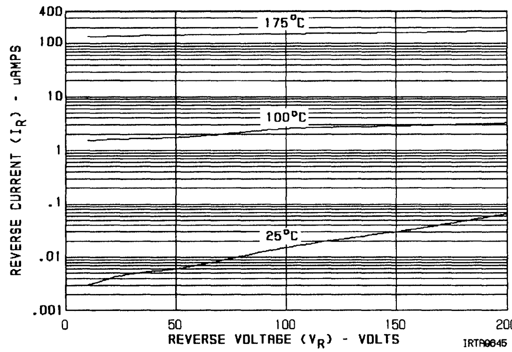


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

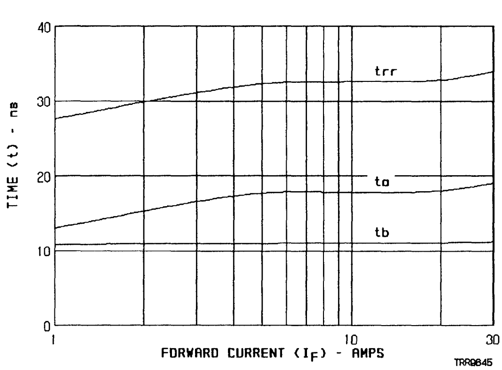


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

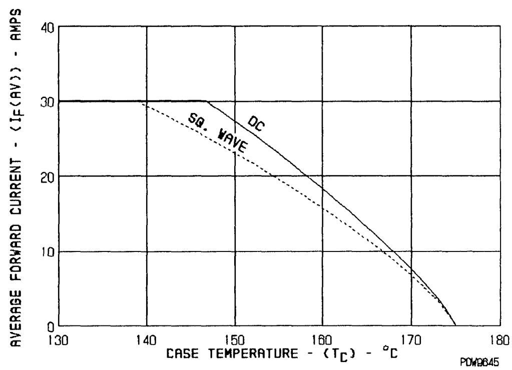


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

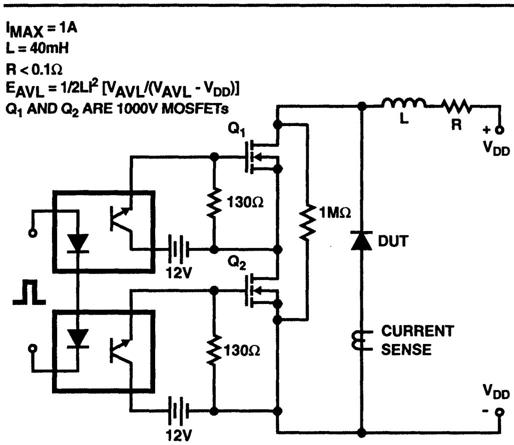


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

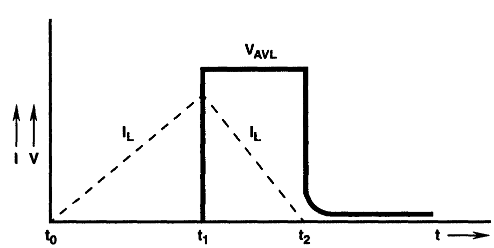


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

6

ULTRAFAST DUAL DIODES

HARRIS SEMICONDUCTOR

RURG3040CC, RURG3050CC, RURG3060CC

April 1995

30A, 400V - 600V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3040CC, RURG3050CC and RURG3060CC (TA9903) are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

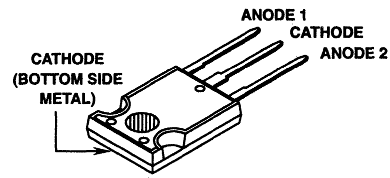
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3040CC	TO-247	RURG3040C
RURG3050CC	TO-247	RURG3050C
RURG3060CC	TO-247	RURG3060C

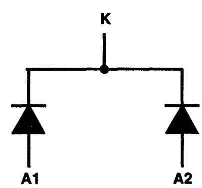
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings $T_C = +25°C$

		RURG3040CC	RURG3050CC	RURG3060CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (Per Leg) (T_C = +130°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RURG3040CC LIMITS			RURG3050CC LIMITS			RURG3060CC LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A$		-	-	1.5	-	-	1.5	-	-	1.5	V
V_F	$I_F = 30A$	$T_C = +150^oC$	-	-	1.3	-	-	1.3	-	-	1.3	V
I_R	$V_R = 400V$		-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V$		-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V$		-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 400V$	$T_C = +150^oC$	-	-	1.0	-	-	-	-	-	-	mA
	$V_R = 500V$	$T_C = +150^oC$	-	-	-	-	-	1.0	-	-	-	mA
	$V_R = 600V$	$T_C = +150^oC$	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$		-	-	55	-	-	55	-	-	55	ns
t_{RR}	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	-	60	-	-	60	-	-	60	ns
t_A	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	30	-	-	30	-	-	30	-	ns
t_B	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$			-	-	1.2	-	-	1.2	-	-	1.2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

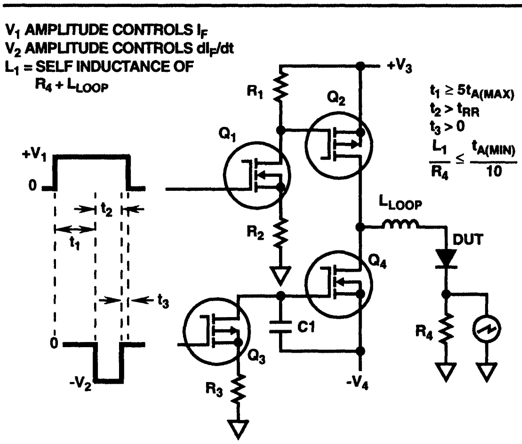


FIGURE 1. t_{RR} TEST CIRCUIT

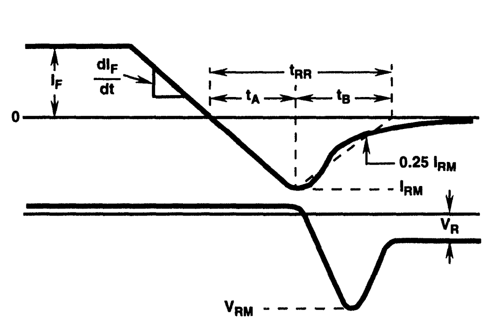


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

6

ULTRAFAST DUAL DIODES

Typical Performance Curves

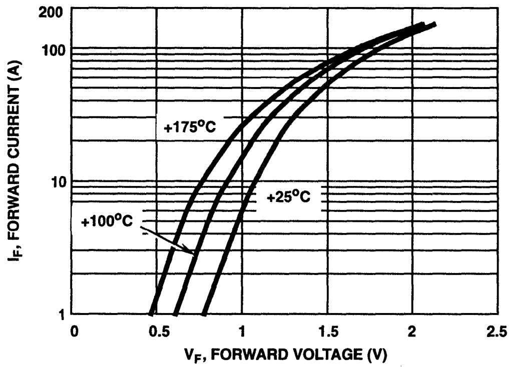


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

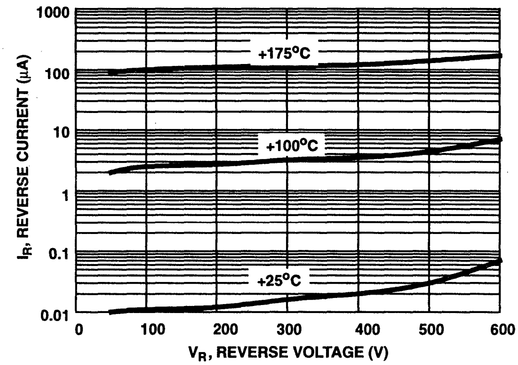


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

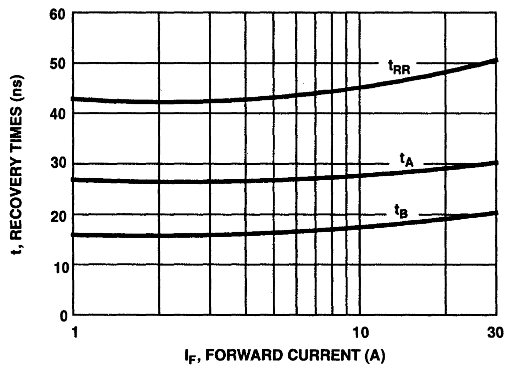


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

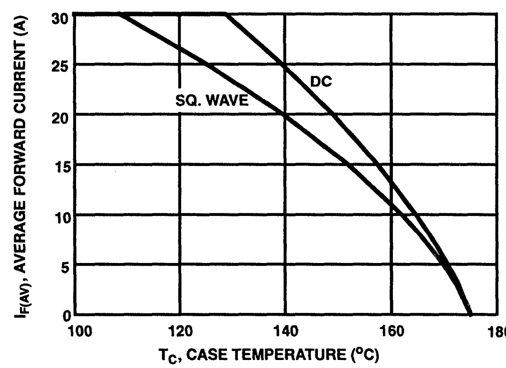


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

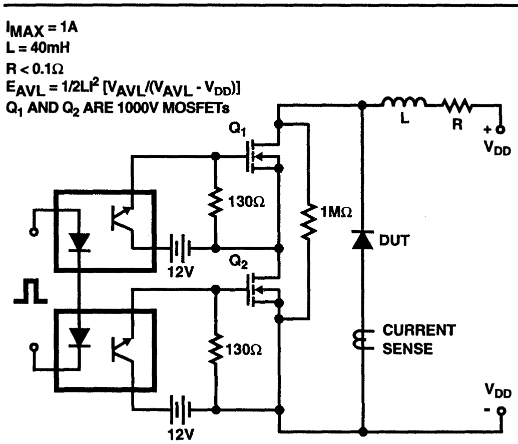


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

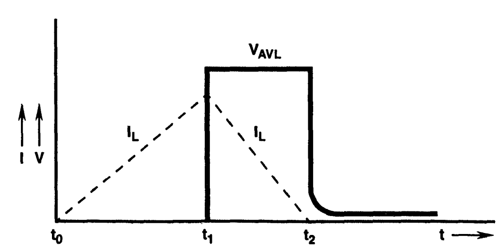


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURG3070CC, RURG3080CC, RURG3090CC, RURG30100CC

April 1995

30A, 700V - 1000V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <110ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURG3070CC, RURG3080CC, RURG3090CC and RURG30100CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 110ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheel/clamping diode and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

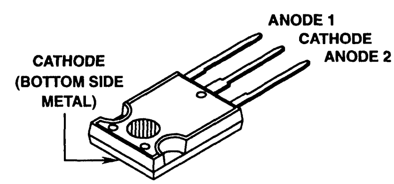
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG3070CC	TO-247	RURG3070C
RURG3080CC	TO-247	RURG3080C
RURG3090CC	TO-247	RURG3090C
RURG30100CC	TO-247	URG30100C

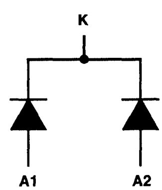
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURG3070CC	RURG3080CC	RURG3090CC	RURG30100CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (Per Leg) (T_C = +117°C)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	60	60	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	300	300	300	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **2935.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURDG3070CC			RURG3080CC			RURG3090CC			RURG30100CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	I_F = 30A, T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at T_C = +150°C	V_R = 700V	-	-	1	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V	-	-	-	-	-	1	-	-	-	-	-	-	mA
	V_R = 900V	-	-	-	-	-	-	-	-	1	-	-	-	mA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	1	mA
I_R at T_C = +25°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A	-	-	110	-	-	110	-	-	110	-	-	110	ns
	I_F = 30A	-	-	150	-	-	150	-	-	150	-	-	150	ns
t_A	I_F = 30A	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	I_F = 30A	-	45	-	-	45	-	-	45	-	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	-	-	1.2	°C/W
E_{AVL}		-	-	30	-	-	30	-	-	30	-	-	30	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), at dI_F/dt = 100A/µs summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = pulse width.

D = duty cycle.

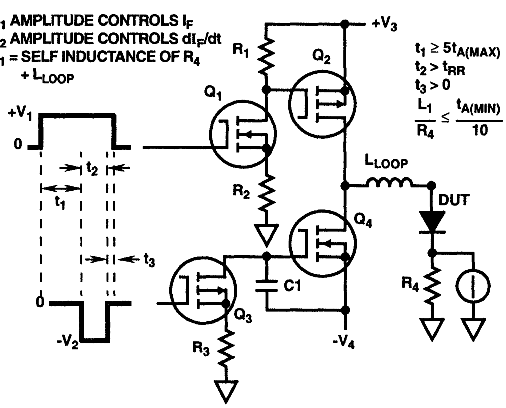


FIGURE 1. t_{RR} TEST CIRCUIT

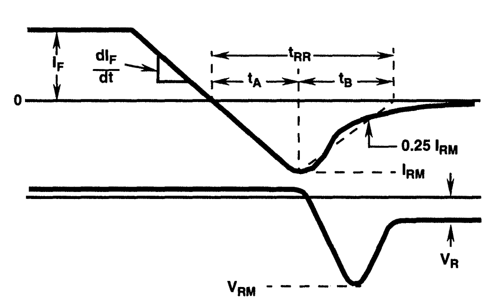


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

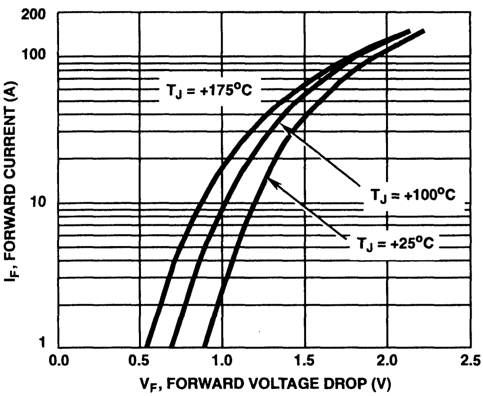


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

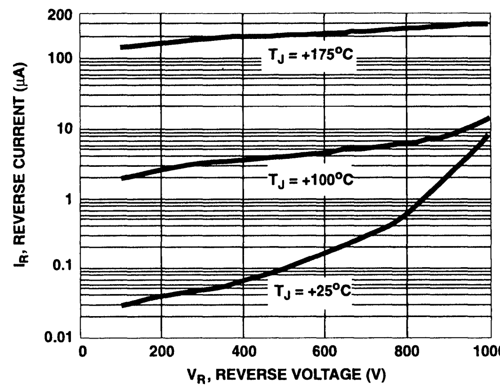


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

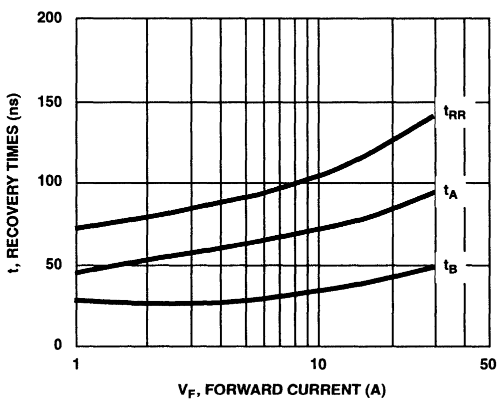


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

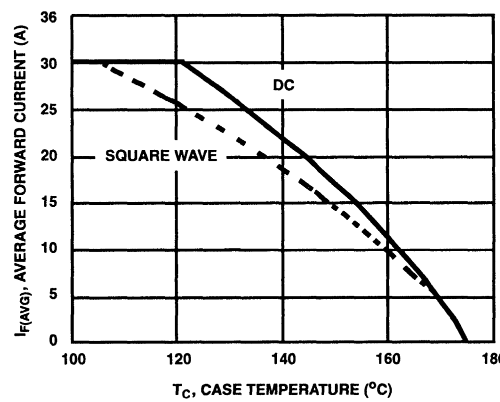


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

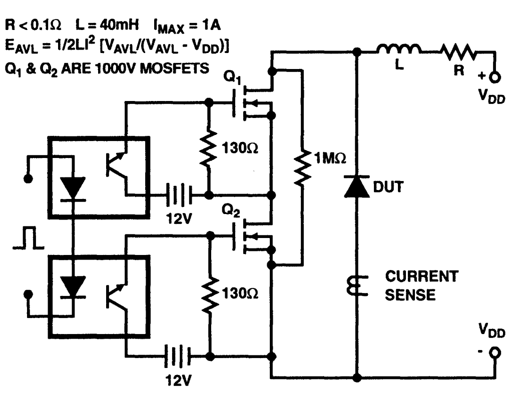


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

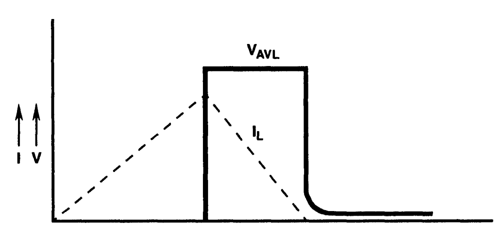


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RURG30120CC

April 1995

30A, 1200V Ultrafast Dual Diode

Features

- Ultrafast with Soft Recovery .... <110ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURG30120CC (49031) is an ultrafast dual diode with soft recovery characteristic (t_{RR} < 110ns). It has low forward voltage drop and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and ultrafast recovery with soft recovery characteristic minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

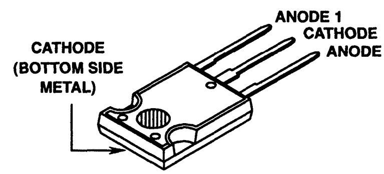
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURG30120CC	TO-247	URG30120C

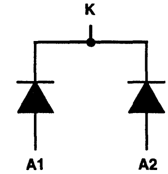
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		RURG30120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (Per Leg) ($T_C = +110°C$)	$I_{F(AV)}$	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	A
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
V_F	$I_F = 30A$, $T_C = +25^oC$	-	-	2.1	V
V_F	$I_F = 30A$, $T_C = +150^oC$	-	-	1.9	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	500	µA
I_R	$V_R = 1200V$, $T_C = +150^oC$	-	-	1	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	110	ns
	$I_F = 30A$, $dI_F/dt = 100A/\mu s$	-	-	150	ns
t_A	$I_F = 30A$, $dI_F/dt = 100A/\mu s$	-	90	-	ns
t_B	$I_F = 30A$, $dI_F/dt = 100A/\mu s$	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = pulse width.

D = duty cycle.

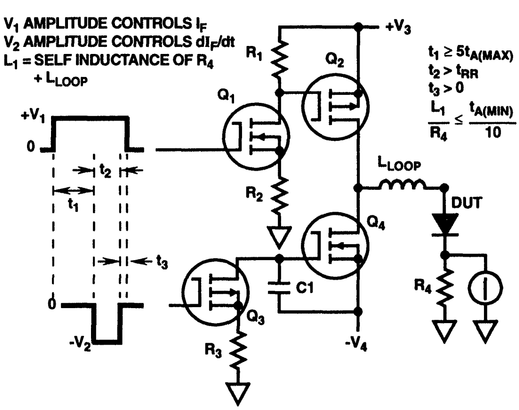


FIGURE 1. t_{RR} TEST CIRCUIT

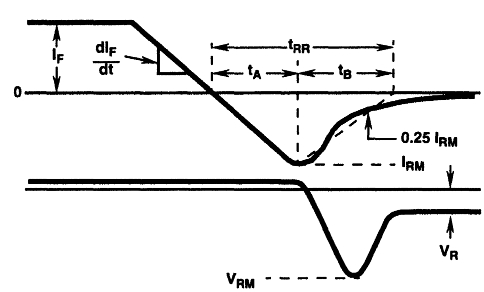


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

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ULTRAFAST DUAL DIODES

Typical Performance Curves

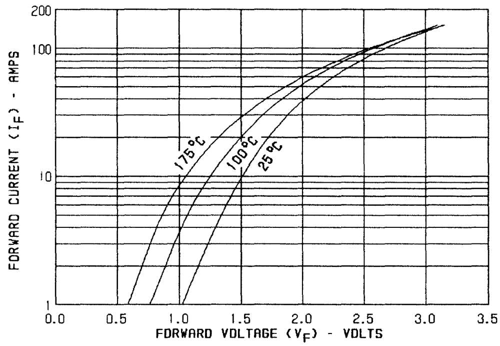


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

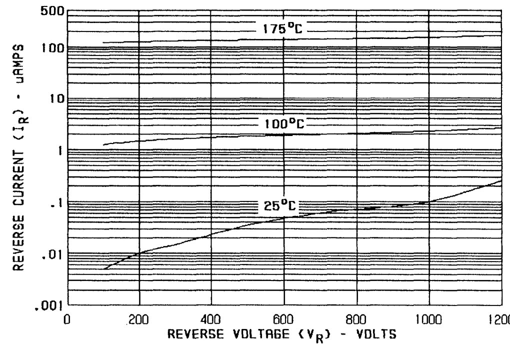


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

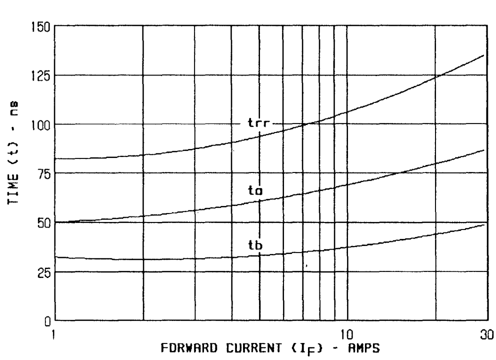


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

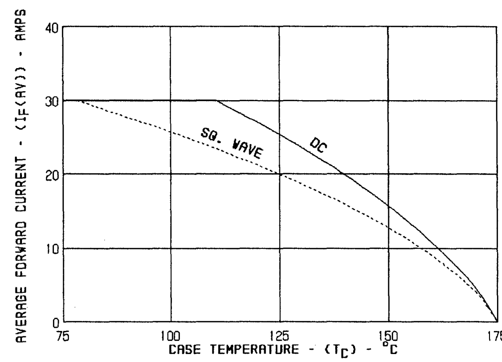


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 & Q_2 ARE 1000V MOSFETs

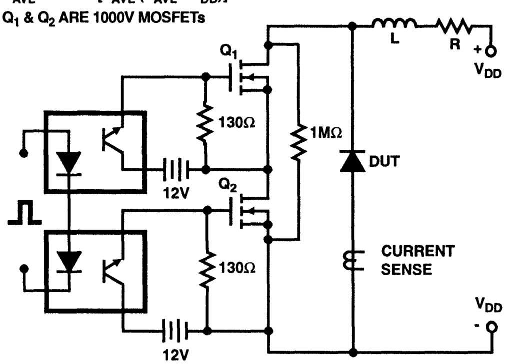


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

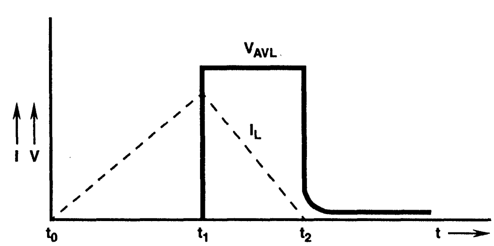


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURH1570CC, RURH1580CC, RURH1590CC, RURH15100CC

April 1995

15A, 700V - 1000V Ultrafast Dual Diodes

Features

- **Ultrafast with Soft Recovery................<100ns**
- **Operating Temperature....................+175°C**
- **Reverse Voltage Up to......................1000V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RURH1570CC, RURH1580CC, RURH1590CC and RURH15100CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 100ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheel/clamping diode and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

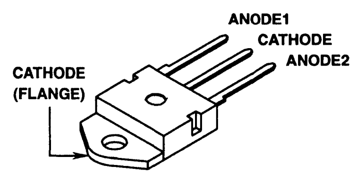
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURH1570CC	TO-218AC	RURH1570C
RURH1580CC	TO-218AC	RURH1580C
RURH1590CC	TO-218AC	RURH1590C
RURH15100CC	TO-218AC	URH15100C

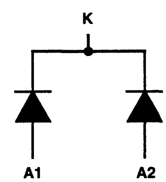
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURH1570CC	RURH1580CC	RURH1590CC	RURH15100CC
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current (Per Leg) (T_C = +141.25°C)	$I_{F(AV)}$	15A	15A	15A	15A
Repetitive Peak Surge Current (Square Wave 20kHz)	I_{FRM}	30A	30A	30A	30A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase 60Hz)	I_{FSM}	200A	200A	200A	200A
Maximum Power Dissipation	P_D	100W	100W	100W	100W
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

File Number **2934.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RURH1570CC			RURH1580CC			RURH1590CC			RURH15100CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A T_C = +150°C	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	I_F = 15A T_C = +25°C	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at T_C=+150°C	V_R = 700V	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	500	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +25°C	V_R = 700V	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V	-	-	-	-	-	-	-	-	-	-	-	100	µA
t_{RR}	I_F = 1A	-	-	100	-	-	100	-	-	100	-	-	100	ns
	I_F = 15A	-	-	125	-	-	125	-	-	125	-	-	125	ns
t_A	I_F = 15A	-	75	-	-	75	-	-	75	-	-	75	-	ns
t_B	I_F = 15A	-	40	-	-	40	-	-	40	-	-	40	-	ns
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	°C/W
E_{AVL}		-	-	20	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

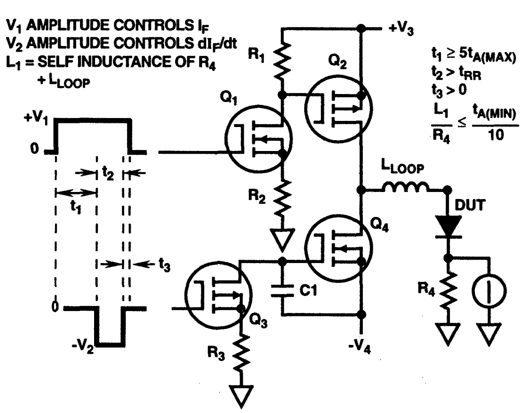


FIGURE 1. t_{RR} TEST CIRCUIT

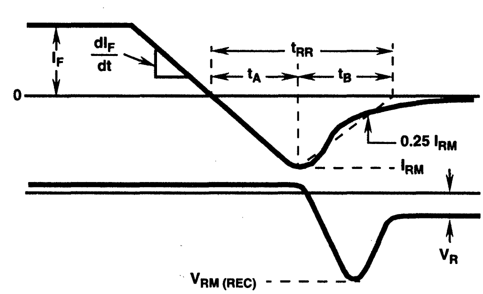


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

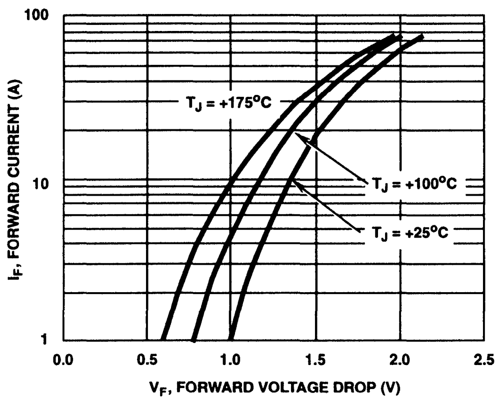


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

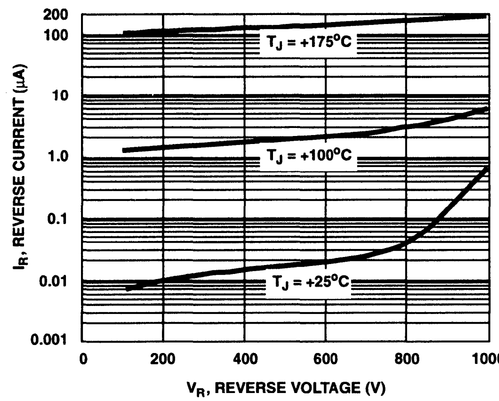


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

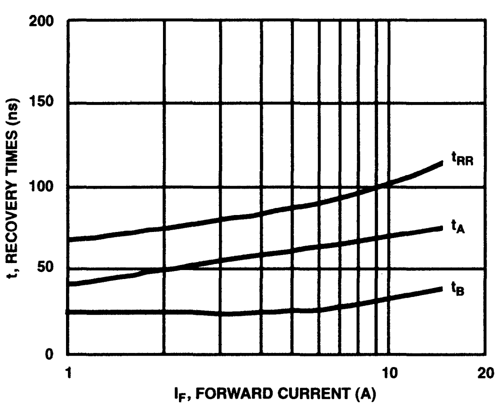


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

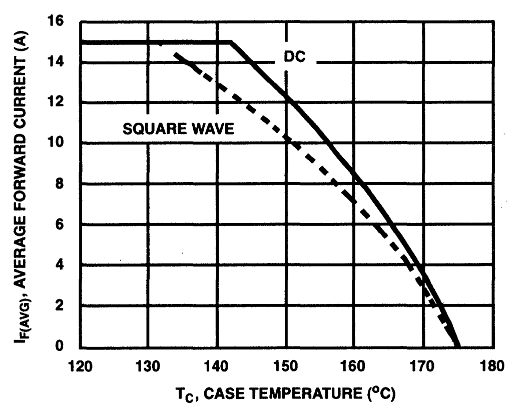


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

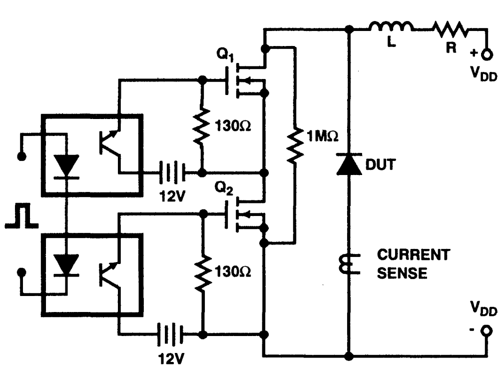


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

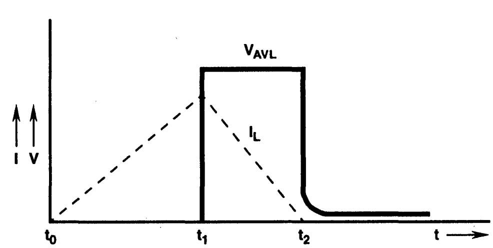


FIGURE 8. CURRENT VOLTAGE WAVEFORM

$I_L$peak = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = (^1/_2) LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$
Q1 AND Q2 ARE 1000V MOSFETs

HARRIS SEMICONDUCTOR

RURH3010CC, RURH3015CC, RURH3020CC

April 1995

30A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 45ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 200V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

RURH3010CC, RURH3015CC, RURH3020CC are ultrafast dual diodes (t_{RR} < 45ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

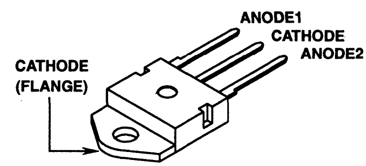
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURH3010CC	TO-218AC	RURH3010C
RURH3015CC	TO-218AC	RURH3015C
RURH3020CC	TO-218AC	RURH3020C

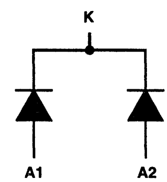
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURH3010CC	RURH3015CC	RURH3020CC
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Working Peak Reverse Voltage	V_{RWM}	100V	150V	200V
DC Blocking Voltage	V_R	100V	150V	200V
Average Rectified Forward Current (Per Leg) (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, Square Wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURH3010CC			RURH3015CC			RURH3020CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A$, $T_C = +150^oC$	-	-	0.85	-	-	0.85	-	-	0.85	V
	$I_F = 30A$, $T_C = +25^oC$	-	-	1.00	-	-	1.00	-	-	1.00	V
I_R at $T_C = +150^oC$	$V_R = 100V$	-	-	1.00	-	-	-	-	-	-	mA
	$V_R = 150V$	-	-	-	-	-	1.00	-	-	-	mA
	$V_R = 200V$	-	-	-	-	-	-	-	-	1.00	mA
I_R at $T_C = +25^oC$	$V_R = 100V$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 150V$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 200V$	-	-	-	-	-	-	-	-	500	µA
t_{RR}	$I_F = 1A$	-	-	45	-	-	45	-	-	45	ns
	$I_F = 30A$	-	-	50	-	-	50	-	-	50	ns
t_A	$I_F = 1A$	-	24	-	-	24	-	-	24	-	ns
	$I_F = 30A$	-	28	-	-	28	-	-	28	-	ns
t_B	$I_F = 1A$	-	17	-	-	17	-	-	17	-	ns
	$I_F = 30A$	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	$^oC/W$
E_{AVL}	see Fig. 7 and 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

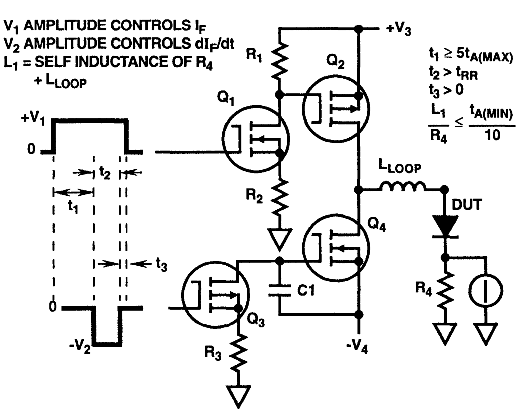


FIGURE 1. t_{RR} TEST CIRCUIT

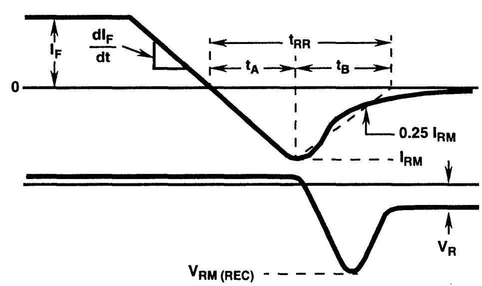


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

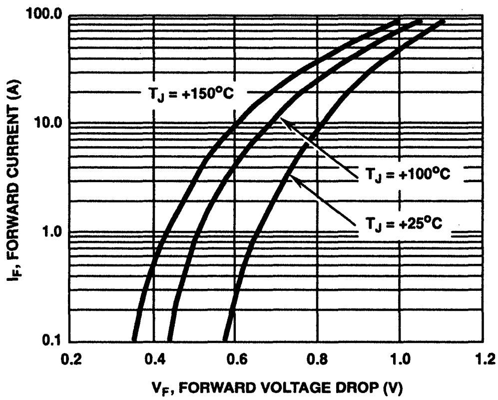


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

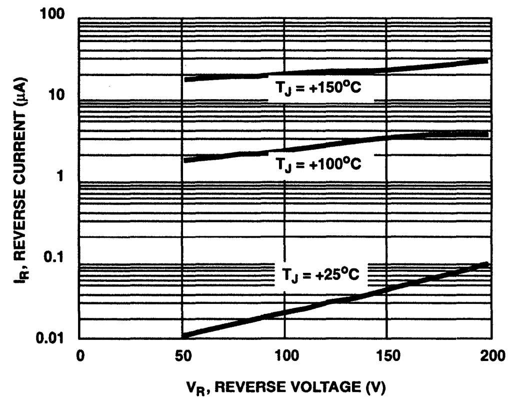


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

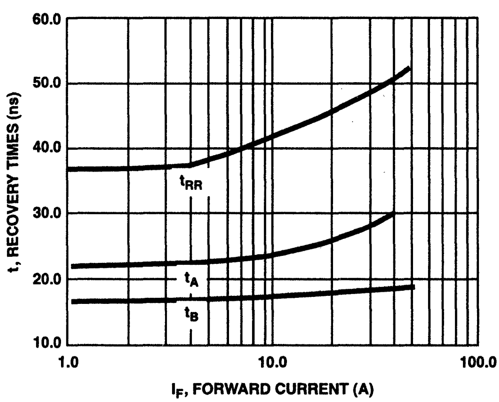


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

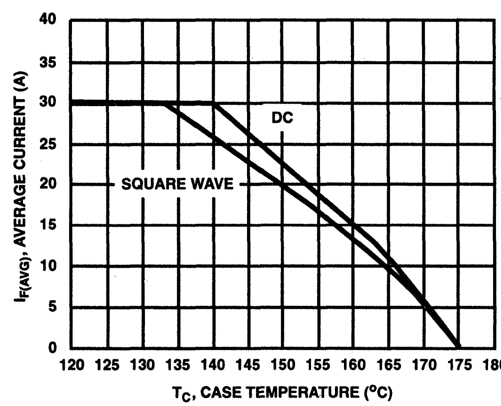


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

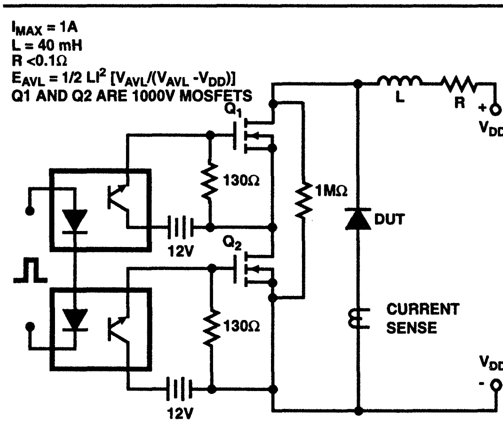


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

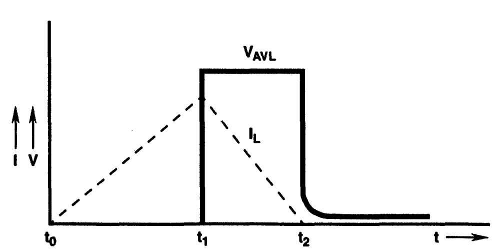


FIGURE 8. CURRENT VOLTAGE WAVEFORM

RURH3040CC, RURH3050CC, RURH3060CC

April 1995

30A, 400V - 600V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery Characteristic (t_{RR} < 55ns)
- +175°C Rated Junction Temperature
- Reverse Voltage Up to 600V
- Avalanche Energy Rated

Applications

- Switching Power Supply
- Power Switching Circuits
- General Purpose

Description

RURH3040CC, RURH3050CC, RURH3060CC are ultrafast dual diodes (t_{RR} < 55ns) with soft recovery characteristics. They have a low forward voltage drop and are of planar, silicon nitride passivated, ion-implanted, epitaxial construction.

These devices are intended for use as energy steering/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristics minimizes ringing and electrical noise in many power switching circuits thus reducing power loss in the switching transistor.

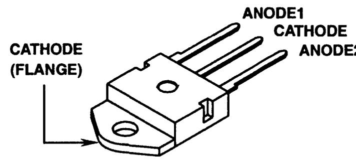
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURH3040CC	TO-218AC	RURH3040C
RURH3050CC	TO-218AC	RURH3050C
RURH3060CC	TO-218AC	RURH3060C

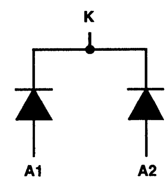
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURH3040CC	RURH3050CC	RURH3060CC
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (Per Leg) (Total device forward current at rated V_R and T_C = +150°C)	$I_{F(AV)}$	30A	30A	30A
Peak Forward Repetitive Current (Rated V_R, square wave 20kHz)	I_{FRM}	70A	70A	70A
Nonrepetitive Peak Surge Current (Surge applied at rated load condition halfwave 1 phase 60Hz)	I_{FSM}	325A	325A	325A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURH3040CC			RURH3050CC			RURH3060CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +150°C	-	-	1.30	-	-	1.30	-	-	1.30	V
	I_F = 30A, T_C = +25°C	-	-	1.50	-	-	1.50	-	-	1.50	V
I_R at T_C = +25°C	V_R = 400V	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V	-	-	-	-	-	-	-	-	500	µA
I_R at T_C = +150°C	V_R = 400V	-	-	1	-	-	-	-	-	-	mA
	V_R = 500V	-	-	-	-	-	1	-	-	-	mA
	V_R = 600V	-	-	-	-	-	-	-	-	1	mA
t_{RR}	I_F = 1A	-	-	55	-	-	55	-	-	55	ns
	I_F = 30A	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 1A	-	20	-	-	20	-	-	20	-	ns
	I_F = 30A	-	38	-	-	38	-	-	38	-	ns
t_B	I_F = 1A	-	15	-	-	15	-	-	15	-	ns
	I_F = 30A	-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W
E_{AVL}	see Fig. 7 and 8	-	-	20	-	-	20	-	-	20	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time at dI_F/dt = 100A/µs (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

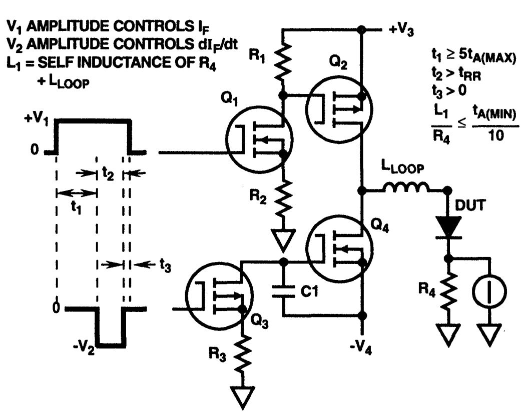


FIGURE 1. t_{RR} TEST CIRCUIT

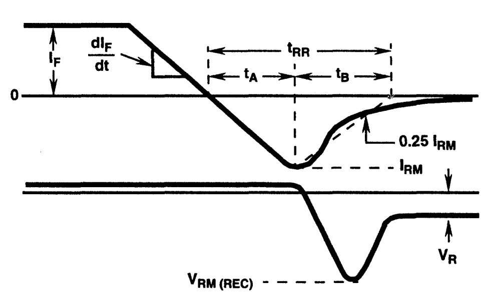


FIGURE 2. DEFINITIONS OF t_{RR}, t_A AND t_B

Typical Performance Curves

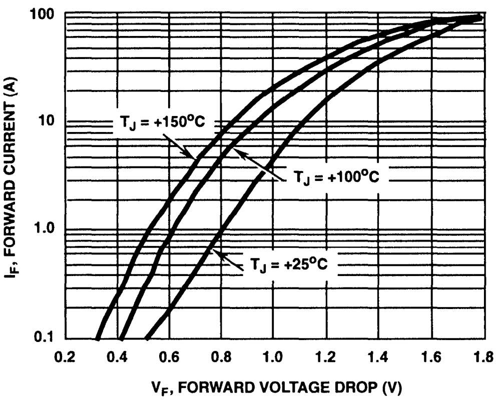


FIGURE 3. FORWARD VOLTAGE vs FORWARD CURRENT CHARACTERISTIC

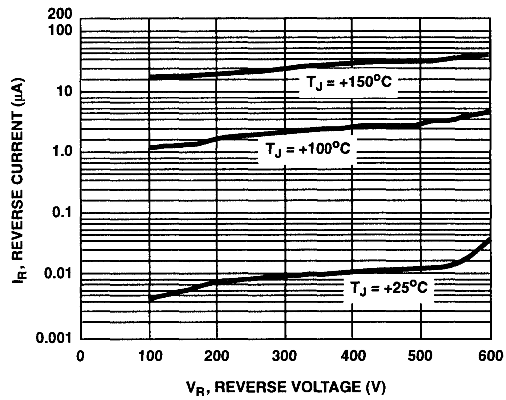


FIGURE 4. REVERSE VOLTAGE vs REVERSE CURRENT CHARACTERISTIC

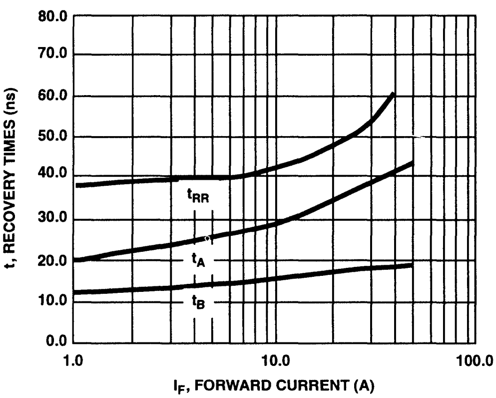


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

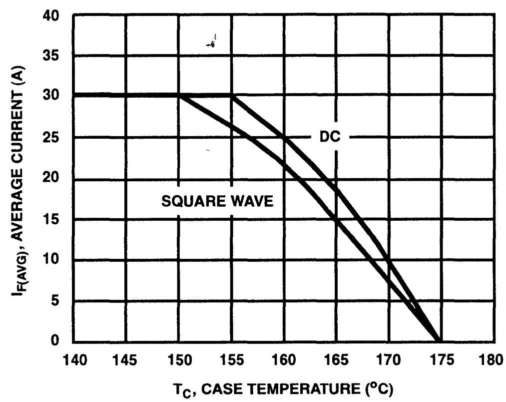


FIGURE 6. TYPICAL CURRENT DERATING CURVE vs CASE TEMPERATURE

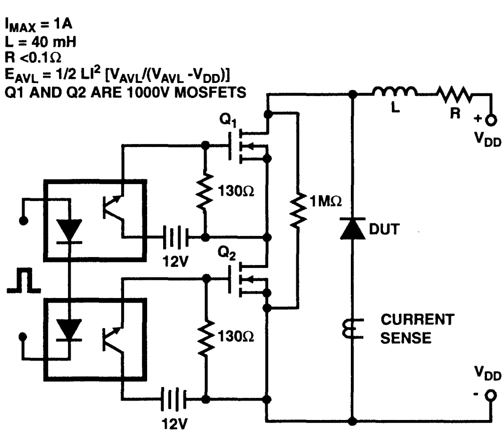


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

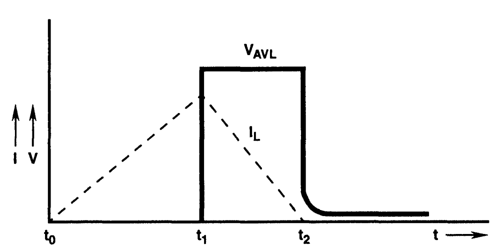


FIGURE 8. CURRENT VOLTAGE WAVEFORM

6
ULTRAFAST DUAL DIODES

HARRIS SEMICONDUCTOR

RURH3070CC, RURH3080CC, RURH3090CC, RURH30100CC

April 1995

30A, 700V - 1000V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <110ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RURH3070CC, RURH3080CC, RURH3090CC and RURH30100CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 110ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast recovery with soft recovery characteristic minimizes ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

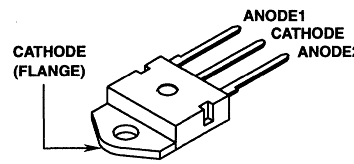
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURH3070CC	TO-218AC	RURH3070C
RURH3080CC	TO-218AC	RURH3080C
RURH3090CC	TO-218AC	RURH3090C
RURH30100CC	TO-218AC	URH30100C

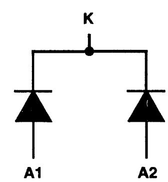
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-218AC



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RURH3070CC	RURH3080CC	RURH3090CC	RURH30100CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (Per Leg) (T_C = +121°C)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	60	60	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	300	300	300	300	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RURH3070CC			RURH3080CC			RURH3090CC			RURH30100CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A$, $T_C = +150^oC$	-	-	1.50	-	-	1.50	-	-	1.50	-	-	1.50	V
	$I_F = 30A$, $T_C = +25^oC$	-	-	1.80	-	-	1.80	-	-	1.80	-	-	1.80	V
I_R at $T_C = +25^oC$	$V_R = 700V$	-	-	500	-	-	-	-	-	-	-	-	-	µA
	$V_R = 800V$	-	-	-	-	-	500	-	-	-	-	-	-	µA
	$V_R = 900V$	-	-	-	-	-	-	-	-	500	-	-	-	µA
	$V_R = 1000V$	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R at $T_C = +150^oC$	$V_R = 700V$	-	-	1	-	-	-	-	-	-	-	-	-	mA
	$V_R = 800V$	-	-	-	-	-	1	-	-	-	-	-	-	mA
	$V_R = 900V$	-	-	-	-	-	-	-	-	1	-	-	-	mA
	$V_R = 1000V$	-	-	-	-	-	-	-	-	-	-	-	1	mA
t_{RR}	$I_F = 1A$	-	-	110	-	-	110	-	-	110	-	-	110	ns
	$I_F = 30A$	-	-	150	-	-	150	-	-	150	-	-	150	ns
t_A	$I_F = 30A$	-	90	-	-	90	-	-	90	-	-	90	-	ns
t_B	$I_F = 30A$	-	45	-	-	45	-	-	45	-	-	45	-	ns
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	-	-	1.2	$^oC/W$
E_{AVL}		-	-	30	-	-	30	-	-	30	-	-	30	mj

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), at dI_F/dt = 100A/µs summation of $t_A + t_B$.

t_A = Time to reach peak reverse current at dI_F/dt = 100A/µs (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

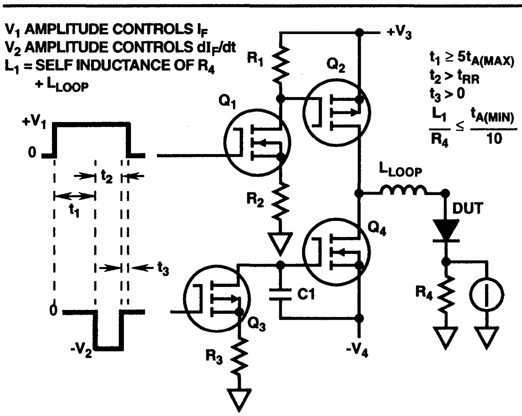


FIGURE 1. t_{RR} TEST CIRCUIT

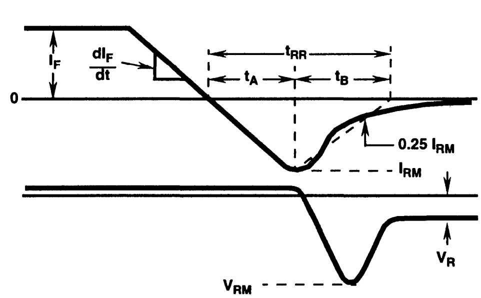


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

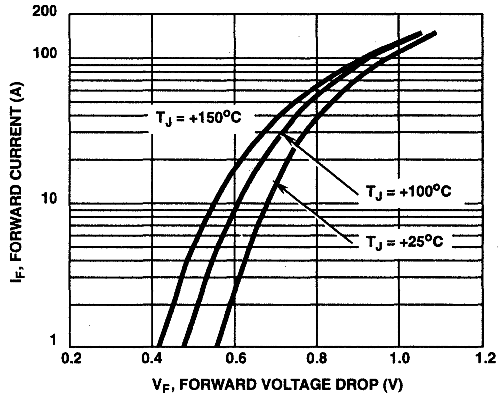


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

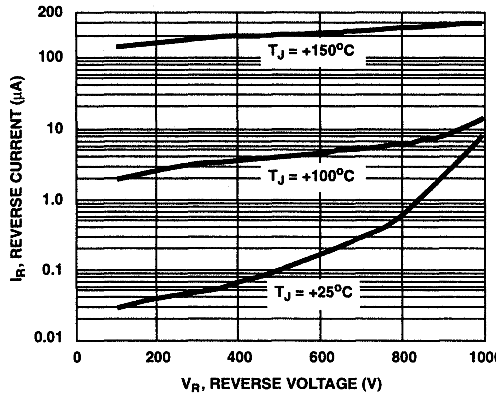


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

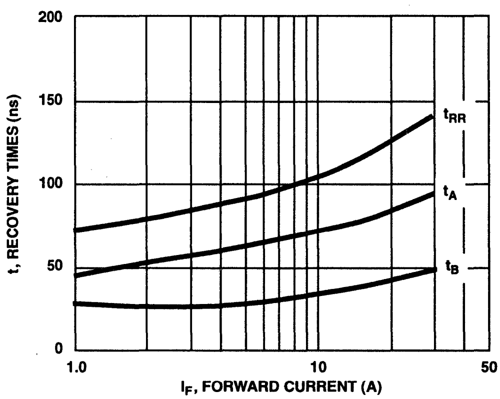


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

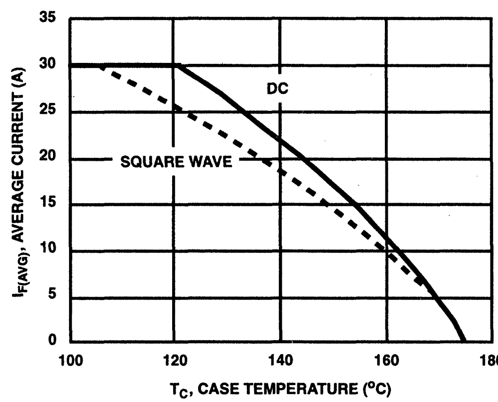


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

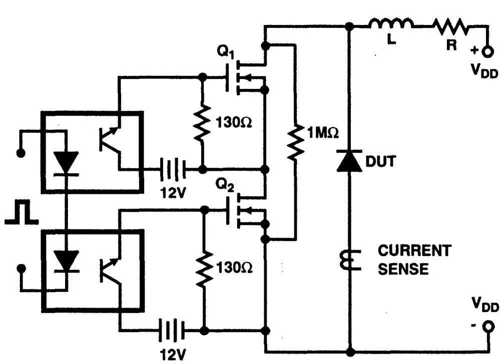


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

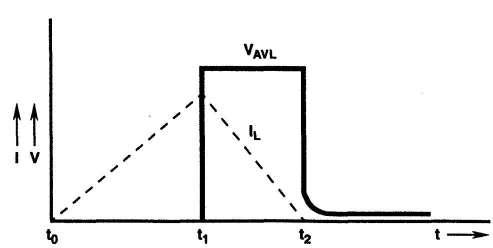


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

I_{MAX} = 1A, L = 40mH, R < 0.1Ω, $E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$, Q_1 & Q_2 ARE 1000V MOSFETS

RURP640CC, RURP650CC, RURP660CC

HARRIS SEMICONDUCTOR

April 1995

6A, 400V - 600V Ultrafast Dual Diodes

Features

- Ultrafast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RURP640CC, RURP650CC, and RURP660CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 55ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

PACKAGE AVAILABILITY

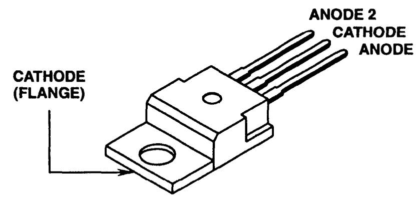
PART NUMBER	PACKAGE	BRAND
RURP640CC	TO-220AB	RURP640C
RURP650CC	TO-220AB	RURP650C
RURP660CC	TO-220AB	RURP660C

NOTE: When ordering, use the entire part number.

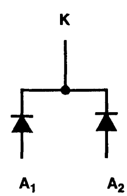
Formerly developmental type TA49038.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RURP640CC	RURP650CC	RURP660CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +155°C)	$I_{F(AV)}$	6	6	6	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	12	12	12	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	60	60	60	A
Maximum Power Dissipation	P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	10	10	10	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications (per leg) $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS									UNITS
		RURP640CC			RURP650CC			RURP660CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 6A, T_C = +25^oC$	-	-	1.5	-	-	1.5	-	-	1.5	V
	$I_F = 6A, T_C = +150^oC$	-	-	1.2	-	-	1.2	-	-	1.2	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	µA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	µA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	µA
t_{RR}	$I_F = 1A, dI_F/dt = 200A/\mu s$	-	-	55	-	-	55	-	-	55	ns
	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	-	60	-	-	60	-	-	60	ns
t_A	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	28	-	-	28	-	-	28	-	ns
t_B	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	16	-	-	16	-	-	16	-	ns
Q_{RR}	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	150	-	-	150	-	-	150	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	25	-	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

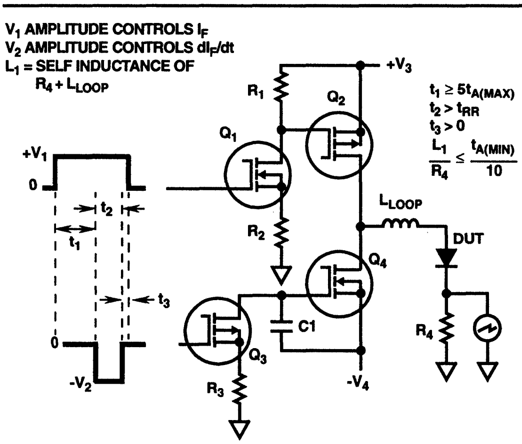


FIGURE 1. t_{RR} TEST CIRCUIT

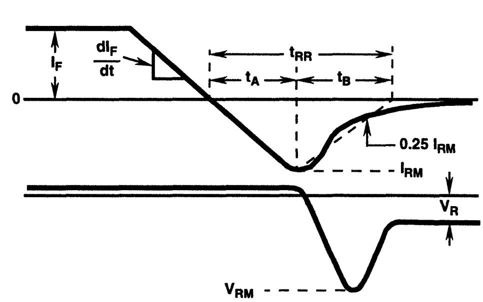


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

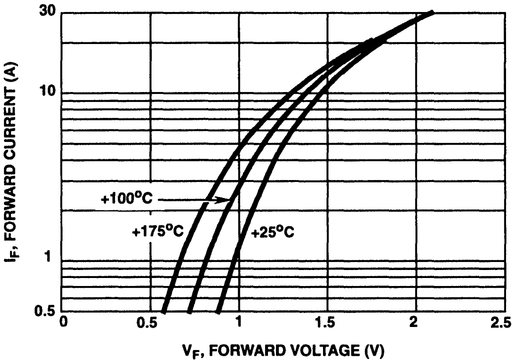


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

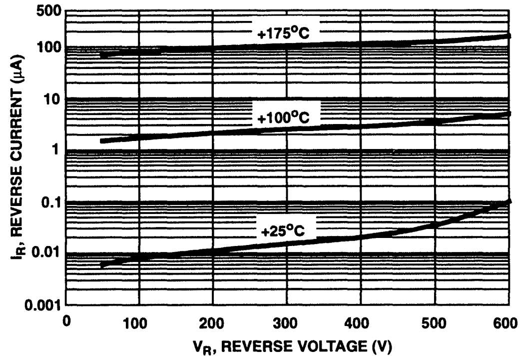


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

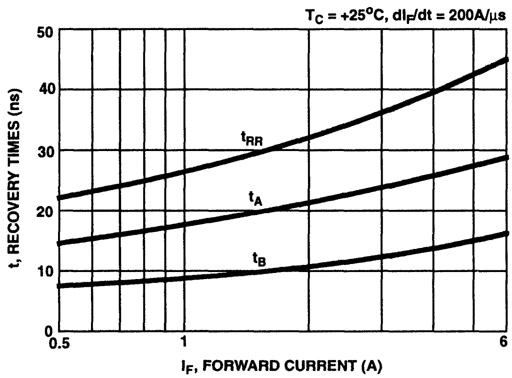


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

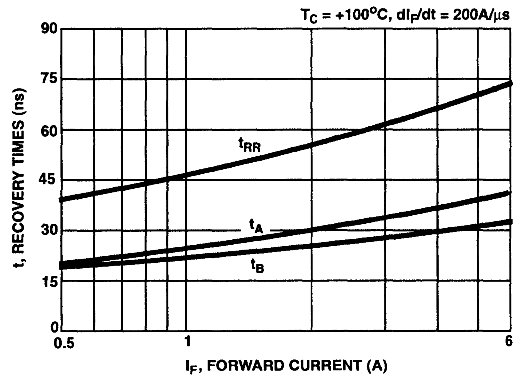


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

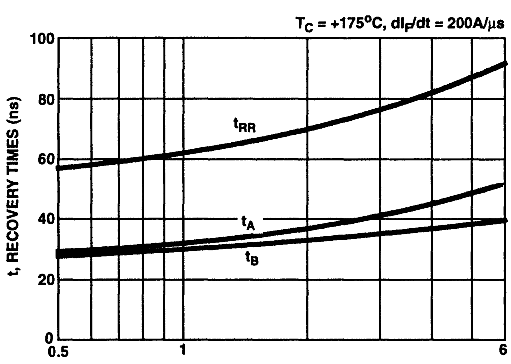


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

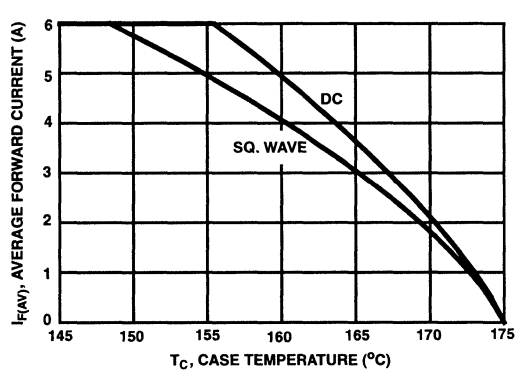


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

6

ULTRAFAST DUAL DIODES

Typical Performance Curves (Continued)

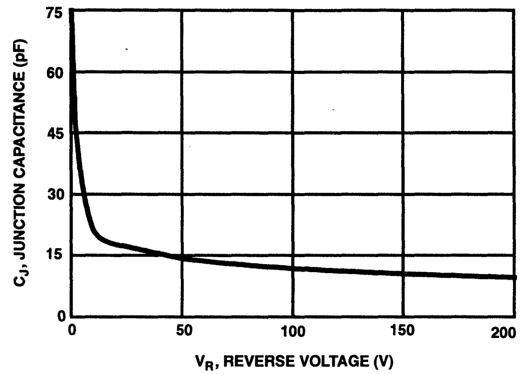


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

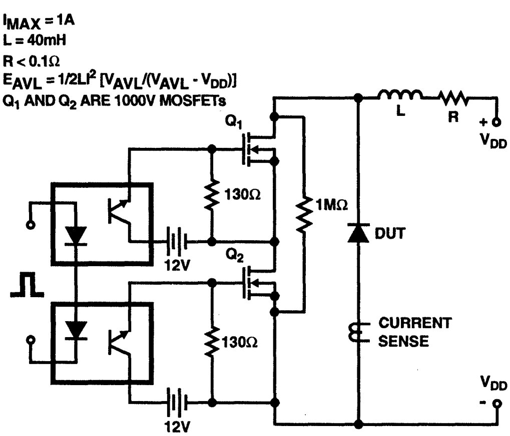


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

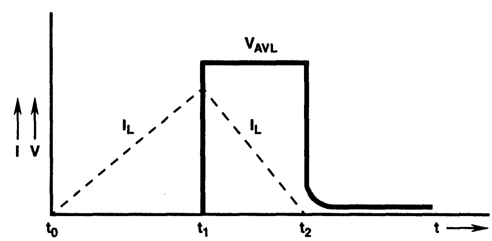


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RURP810CC, RURP815CC, RURP820CC

April 1995

8A, 100V - 200V Ultrafast Dual Diodes

Features

- Ultrafast Recovery Time (t_{RR} < 35ns)
- Low Forward Voltage
- Low Thermal Resistance
- Planar Design
- Wire-Bonded Construction

Applications

- General Purpose
- Power Switching Circuits to 100kHz
- Full-Wave Rectification

Description

RURP810CC, RURP815CC, RURP820CC are low forward voltage drop ultrafast rectifiers (t_{RR} < 35ns). They use an ion-implanted planar epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodes in a variety of high frequency pulse width modulated and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

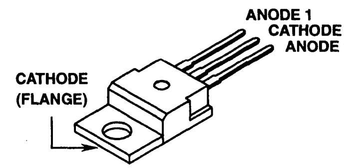
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RURP810CC	TO-220AB	RURP810CC
RURP815CC	TO-220AB	RURP815CC
RURP820CC	TO-220AB	RURP820CC

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



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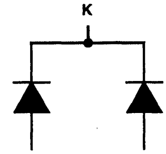


6 ULTRAFAST DUAL DIODES

Absolute Maximum Ratings $T_C = +25^oC$

		RURP810CC	RURP815CC	RURP820CC
Peak Repetitive Reverse Voltage	V_{RRM}	100V	150V	200V
Average Rectified Forward Current (Per Leg)				
$T_A = +25^oC$ (No Heat Sink)	$I_{F(AV)}$	3A	3A	3A
$T_A = +25^oC$ (With Heat Sink)†	$I_{F(AV)}$	8A	8A	8A
$T_C = +125^oC$	$I_{F(AV)}$	8A	8A	8A
Nonrepetitive Peak Surge Current (8.3ms, 1/2 cycle)	I_{FSM}	100A	100A	100A
Operating and Storage Temperature	T_{STG}, T_J	-55°C to +175°C	-55°C to +175°C	-55°C to +175°C
Maximum Lead Temperature During Solder (At distance > 1/8" (3.17mm) from case or 10s max)	T_L	260°C	260°C	260°C

† Wakefield type 295 heat sink with convection cooling.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified.

SYMBOL	TEST CONDITION	RURP810CC			RURP815CC			RURP820CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 8A$, $T_C = +150^oC$	-	-	0.895	-	-	0.895	-	-	0.895	V
	$I_F = 8A$, $T_C = +25^oC$	-	-	0.975	-	-	0.975	-	-	0.975	V
I_R at $T_C = +150^oC$	$V_R = 100V$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 150V$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 200V$	-	-	-	-	-	-	-	-	500	μA
I_R at $T_C = +25^oC$	$V_R = 100V$	-	-	100	-	-	-	-	-	-	μA
	$V_R = 150V$	-	-	-	-	-	100	-	-	-	μA
	$V_R = 200V$	-	-	-	-	-	-	-	-	100	μA
t_{RR}	$I_F = 8A$†	-	-	35	-	-	35	-	-	35	ns
$R_{\theta JC}$		-	-	2.25	-	-	2.25	-	-	2.25	°C/W
$R_{\theta JA}$		-	-	60	-	-	60	-	-	60	°C/W
C_J	$V_R = 10V$, $I_F = 0A$	-	40	-	-	40	-	-	40	-	pF

†$dI_F/dt = 50A/\mu s$, I_{RM} (rec) < 1A, $I_{RR} = 0.25A$.

Typical Performance Curves

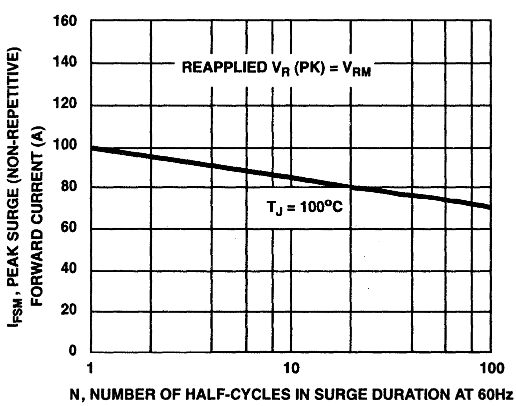


FIGURE 1. PEAK SURGE FORWARD CURRENT vs SURGE DURATION

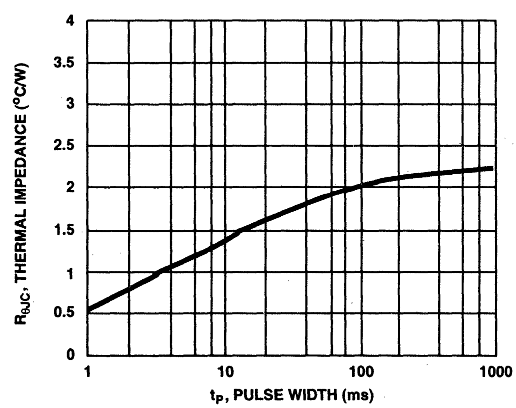


FIGURE 2. THERMAL IMPEDANCE vs PULSE WIDTH (PER JUNCTION)

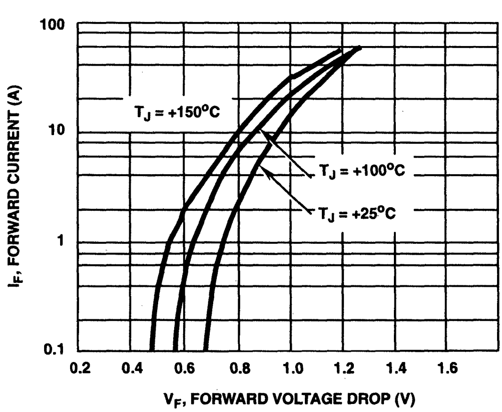


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

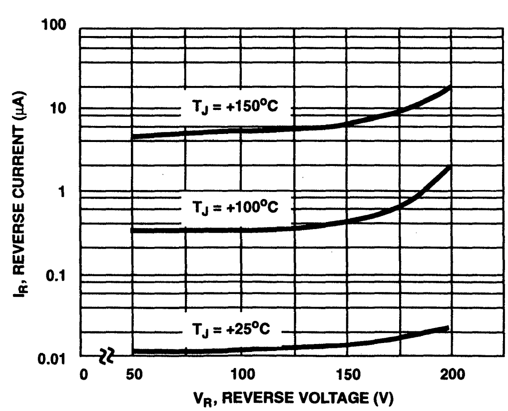


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

HARRIS SEMICONDUCTOR

RURP840CC, RURP850CC, RURP860CC

April 1995

8A, 400V - 600V Ultrafast Dual Diodes

Features

- **Ultrafast with Soft Recovery . . . . <60ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage Up To 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

The RURP840CC, RURP850CC, and RURP860CC are ultrafast dual diodes with soft recovery characteristics (t_{RR} < 60ns). They have low forward voltage drop and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and ultrafast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGING AVAILABILITY

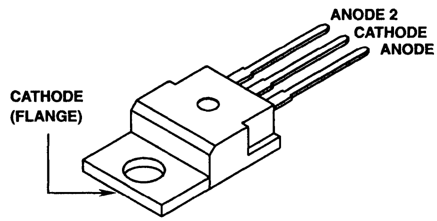
PART NUMBER	PACKAGE	BRAND
RURP840CC	TO-220AB	RURP840C
RURP850CC	TO-220AB	RURP850C
RURP860CC	TO-220AB	RURP860C

NOTE: When ordering, use the entire part number.

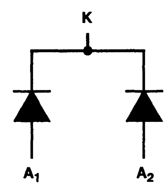
Formerly developmental type TA09616.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RURP840CC	RURP850CC	RURP860CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +155°C)	$I_{F(AV)}$	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	100	100	100	A
Maximum Power Dissipation	P_D	75	75	75	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3974**

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

		LIMITS									
		RURP840CC			RURP850CC			RURP860CC			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 8A, T_C = +25°C	-	-	1.3	-	-	1.5	-	-	1.5	V
	I_F = 8A, T_C = +150°C	-	-	1.0	-	-	1.2	-	-	1.2	V
I_R	V_R = 400V, T_C = +25°C	-	-	100	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	100	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 200A/μs	-	-	60	-	-	60	-	-	60	ns
	I_F = 8A, dI_F/dt = 200A/μs	-	-	70	-	-	70	-	-	70	ns
t_A	I_F = 8A, dI_F/dt = 200A/μs	-	32	-	-	32	-	-	32	-	ns
t_B	I_F = 8A, dI_F/dt = 200A/μs	-	21	-	-	21	-	-	21	-	ns
Q_{RR}	I_F = 8A, dI_F/dt = 200A/μs	-	195	-	-	195	-	-	195	-	nC
C_J	V_R = 10V, I_F = 0A	-	25	-	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	2	-	-	2	-	-	2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

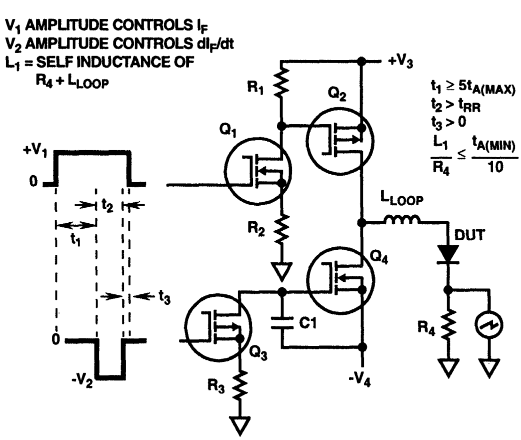


FIGURE 1. t_{RR} TEST CIRCUIT

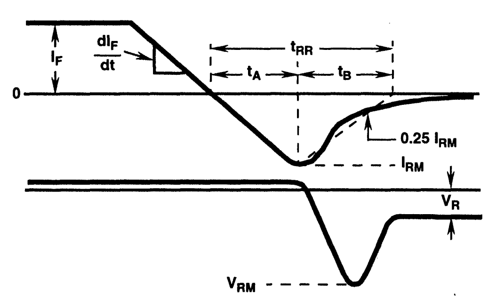


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

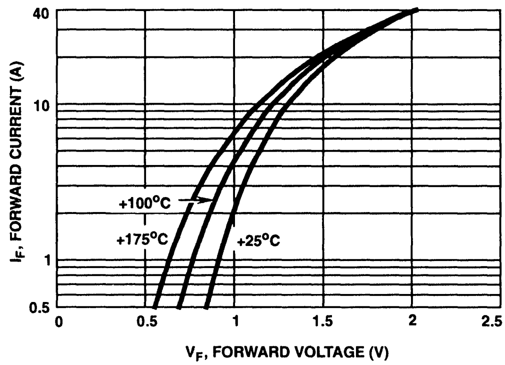


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

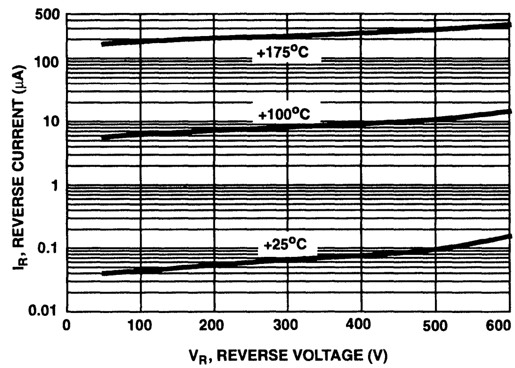


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

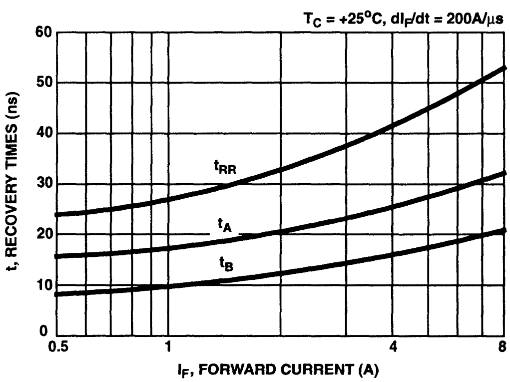


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

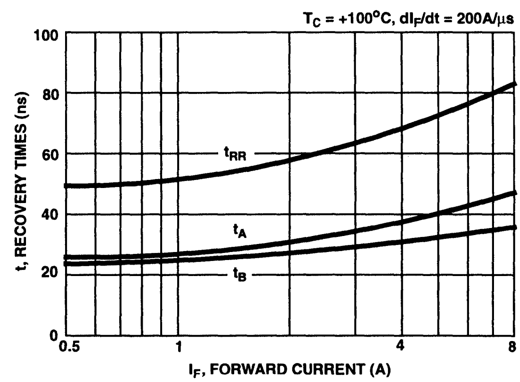


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

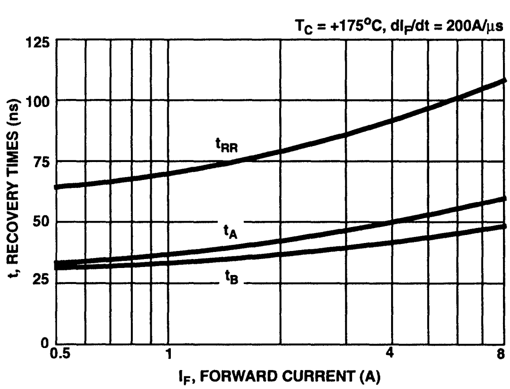


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

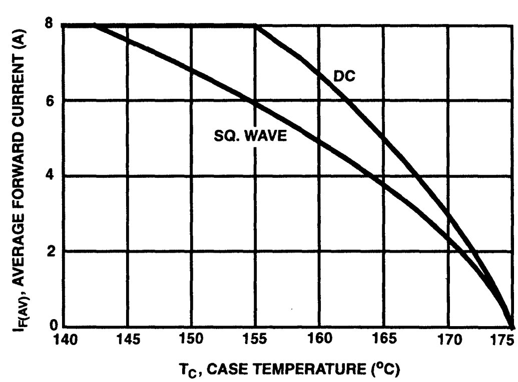


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

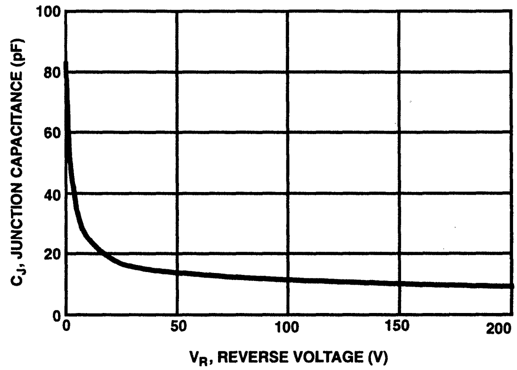


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

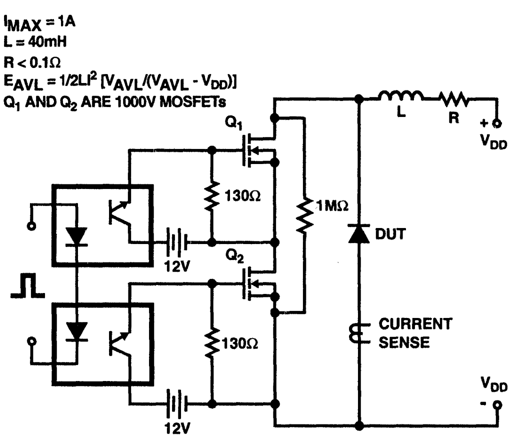


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

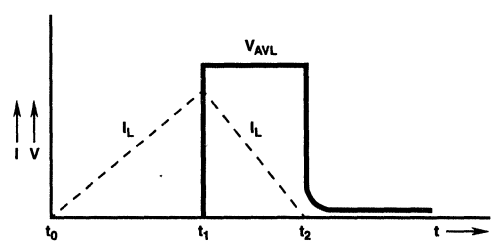


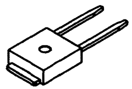
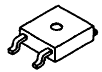
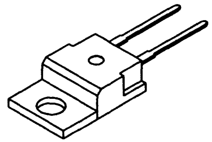
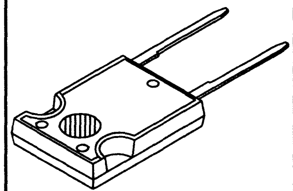
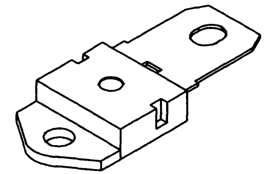
FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

MCT/IGBT/DIODES 7

HYPERFAST SINGLE DIODES

Hyperfast Single Diodes (Continued)

HARRIS HYPER-FAST RECOVERY RECTIFIER PRODUCT LINE

	 TO-251		 TO-252		 TO-220AC			 2 LEADED TO-247			 SINGLE LEAD TO-218			
	$I_{F(AVG)}$		$I_{F(AVG)}$		$I_{F(AVG)}$			$I_{F(AVG)}$			$I_{F(AVG)}$			
V_{RRM}	4A	6A	4A	6A	8A	15A	30A	30A	50A	75A	50A	75A	100A	150A
400V	RHRD440 2.1V 35ns	RHRD640 2.1V 35ns	RHRD440S 2.1V 35ns	RHRD640S 2.1V 35ns	RHRP840 2.1V 35ns	RHRP1540 2.1V 40ns	RHRP3040 2.1V 45ns	RHRG3040 2.1V 45ns	RHRG5040 2.1V 50ns	RHRG7540 2.1V 60ns	RHRU5040 2.1V 50ns	RHRU7540 2.1V 60ns	RHRU10040 2.1V 60ns	RHRU15040 2.1V 70ns
500V	RHRD450 2.1V 35ns	RHRD650 2.1V 35ns	RHRD450S 2.1V 35ns	RHRD650S 2.1V 35ns	RHRP850 2.1V 35ns	RHRP1550 2.1V 40ns	RHRP3050 2.1V 45ns	RHRG3050 2.1V 45ns	RHRG5050 2.1V 50ns	RHRG7550 2.1V 60ns	RHRU5050 2.1V 50ns	RHRU7550 2.1V 60ns	RHRU10050 2.1V 60ns	RHRU15050 2.1V 70ns
600V	RHRD460 2.1V 35ns	RHRD660 2.1V 35ns	RHRD460S 2.1V 35ns	RHRD660S 2.1V 35ns	RHRP860 2.1V 35ns	RHRP1560 2.1V 40ns	RHRP3060 2.1V 45ns	RHRG3060 2.1V 45ns	RHRG5060 2.1V 50ns	RHRG7560 2.1V 60ns	RHRU5060 2.1V 50ns	RHRU7560 2.1V 60ns	RHRU10060 2.1V 60ns	RHRU15060 2.1V 70ns
700V					RHRP870 3.0V 65ns	RHRP1570 3.0V 70ns	RHRP3070 3.0V 75ns	RHRG3070 3.0V 75ns	RHRG5070 3.0V 95ns	RHRG7570 3.0V 100ns	RHRU5070 3.0V 95ns	RHRU7570 3.0V 100ns		
800V					RHRP880 3.0V 65ns	RHRP1580 3.0V 70ns	RHRP3080 3.0V 75ns	RHRG3080 3.0V 75ns	RHRG5080 3.0V 95ns	RHRG7580 3.0V 100ns	RHRU5080 3.0V 95ns	RHRU7580 3.0V 100ns		
900V					RHRP890 3.0V 65ns	RHRP1590 3.0V 70ns	RHRP3090 3.0V 75ns	RHRG3090 3.0V 75ns	RHRG5090 3.0V 95ns	RHRG7590 3.0V 100ns	RHRU5090 3.0V 95ns	RHRU7590 3.0V 100ns		RHRU15090 3.0V 100ns
1000V					RHRP8100 3.0V 65ns	RHRP15100 3.0V 70ns	RHRP30100 3.0V 75ns	RHRG30100 3.0V 75ns	RHRG50100 3.0V 95ns	RHRG75100 3.0V 100ns	RHRU50100 3.0V 95ns	RHRU75100 3.0V 100ns		RHRU150100 3.0V 100ns
1200V	RHRD4120 3.2V 70ns	*RHRD6120* 3.2V 65ns	RHRD4120S 3.2V 70ns	*RHRD6120S* 3.2V 65ns	RHRP8120 3.2V 70ns	RHRP15120 3.2V 75ns	RHRP30120 3.2V 75ns	RHRG30120 3.2V 75ns	RHRG50120 3.2V 100ns	RHRG75120 3.2V 100ns	RHRU50120 3.2V 100ns	RHRU75120 3.2V 100ns	RHRU100120 3.2V 100ns	*RHRU150120*

ITALICS = Future Product Offerings; V_F at $I_{F(AVG)}$, $T_J = 25^oC$; T_{RR} at $I_{F(AVG)}$, $dI_F/dt = 100A/\mu sec$ $T_J = 25^oC$; † T_{RR} at $I_F = 1A$

RHRD440, RHRD450, RHRD460, RHRD440S, RHRD450S, RHRD460S

April 1995

4A, 400V - 600V Hyperfast Diodes

Features

- **Hyperfast with Soft Recovery . . . . <30ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage Up to 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRD440, RHRD450, RHRD460, RHRD440S, RHRD450S, and RHRD460S (TA49055) are hyperfast diodes with soft recovery characteristics (t_{RR} < 30ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

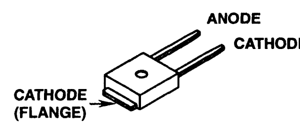
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRD440	TO-251	RHR440
RHRD450	TO-251	RHR450
RHRD460	TO-251	RHR460
RHRD440S	TO-252	RHR440
RHRD450S	TO-252	RHR450
RHRD460S	TO-252	RHR460

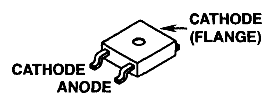
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RHRD450S9A.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	RHRD440 RHRD440S	RHRD450 RHRD450S	RHRD460 RHRD460S	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	400	500	600	V
Working Peak Reverse Voltage . . . . V_{RWM}	400	500	600	V
DC Blocking Voltage . . . . V_R	400	500	600	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ (T_C = +157°C)	4	4	4	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	8	8	8	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	40	40	40	A
Maximum Power Dissipation . . . . P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11) . . . . E_{AVL}	10	10	10	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3613.4**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		LIMITS									
		RHRD440 RHRD440S			RHRD450 RHRD450S			RHRD460 RHRD460S			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 4A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
V_F	I_F = 4A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	100	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	100	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 200A/μs	-	-	30	-	-	30	-	-	30	ns
	I_F = 4A, dI_F/dt = 200A/μs	-	-	35	-	-	35	-	-	35	ns
t_A	I_F = 4A, dI_F/dt = 200A/μs	-	16	-	-	16	-	-	16	-	ns
t_B	I_F = 4A, dI_F/dt = 200A/μs	-	7	-	-	7	-	-	7	-	ns
Q_{RR}	I_F = 4A, dI_F/dt = 200A/μs	-	45	-	-	45	-	-	45	-	nC
C_J	V_R = 10V, I_F = 0A	-	15	-	-	15	-	-	15	-	pf
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

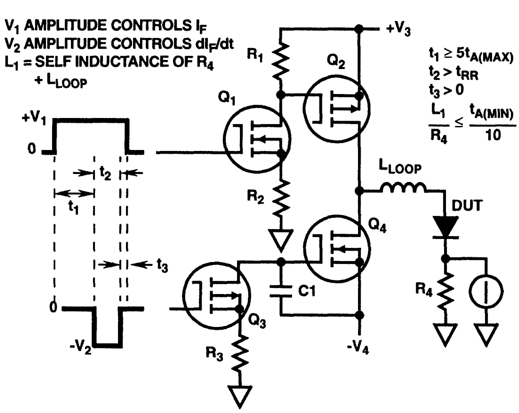


FIGURE 1. t_{RR} TEST CIRCUIT

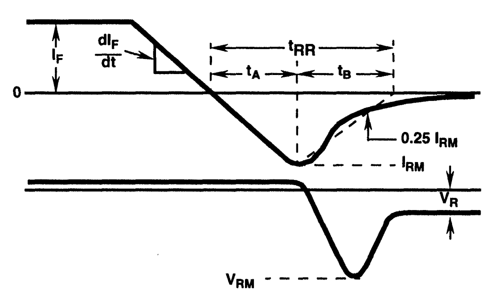


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

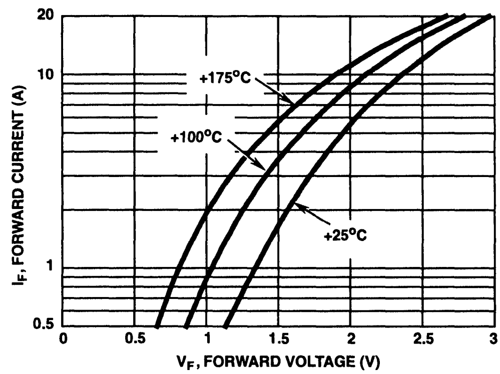


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

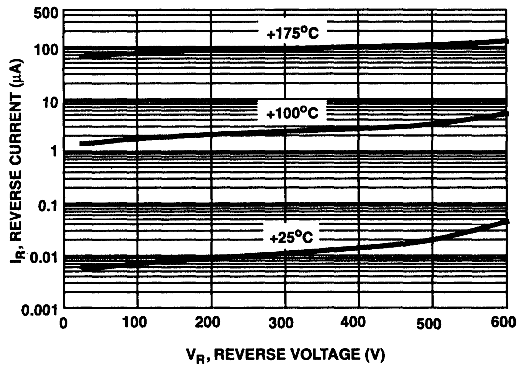


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

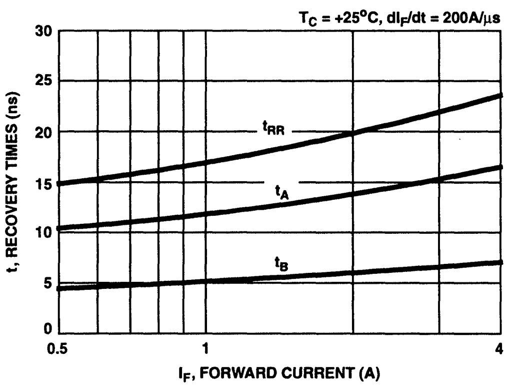


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

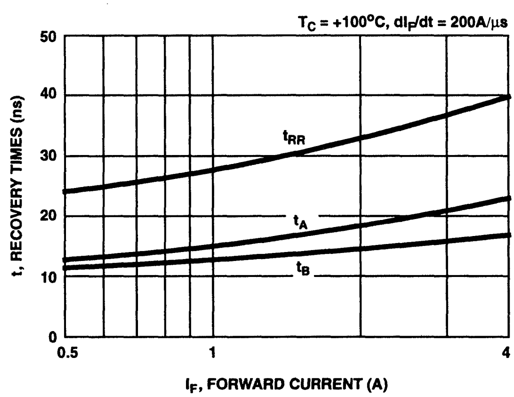


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

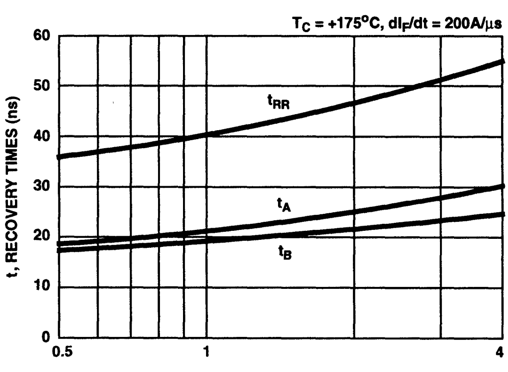


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

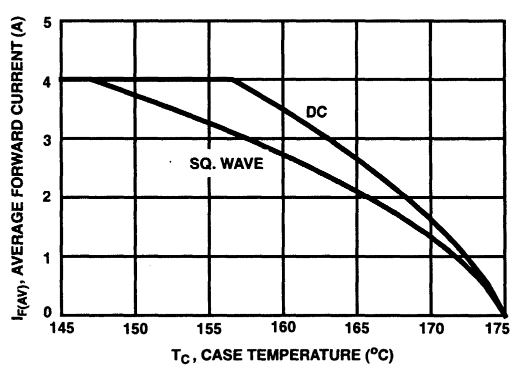


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

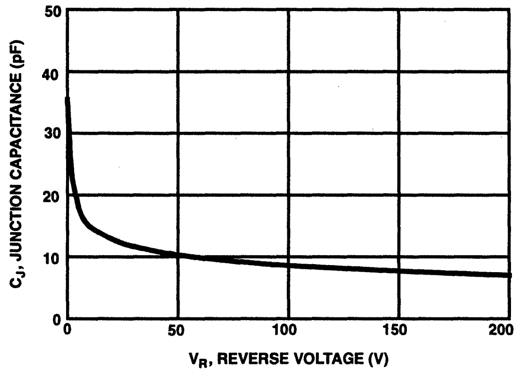


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuits and Waveforms

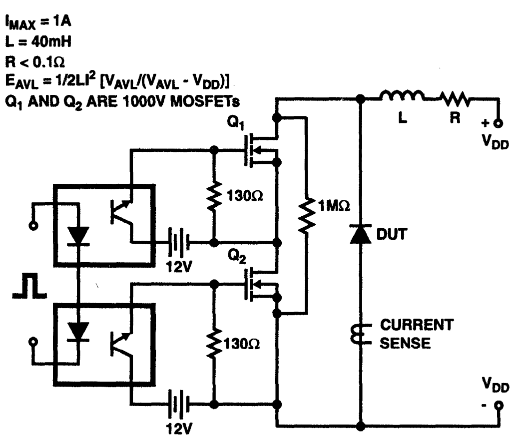


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

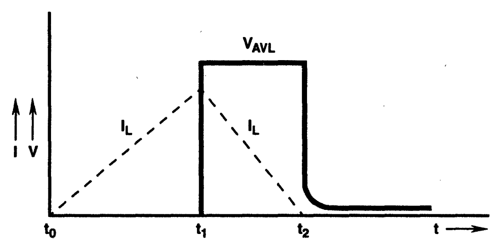


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRD4120, RHRD4120S

April 1995

4A, 1200V Hyperfast Diodes

Features

- **Hyperfast with Soft Recovery . . . . <60ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage 1200V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRD4120 and RHRD4120S (TA49056) are hyperfast diodes with soft recovery characteristics (t_{RR} < 60ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

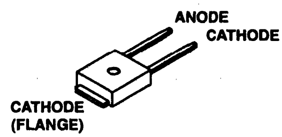
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRD4120	TO-251	HR4120
RHRD4120S	TO-252	HR4120

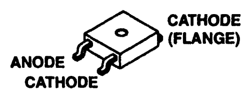
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RHRD4120S9A.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRD4120 RHRD4120S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +147.5°C)	$I_{F(AV)}$	4	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	8	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	40	A
Maximum Power Dissipation	P_D	50	W
Avalanche Energy (L = 40mH)	E_{AVL}	10	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3626.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRD4120, RHRD4120S			UNITS
		MIN	TYP	MAX	
V_F	$I_F = 4A$, $T_C = +25^oC$	-	-	3.2	V
V_F	$I_F = 4A$, $T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	100	µA
I_R	$V_R = 1200V$, $T_C = +150^oC$	-	-	500	µA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	60	ns
	$I_F = 4A$, $dI_F/dt = 100A/\mu s$	-	-	70	ns
t_A	$I_F = 4A$, $dI_F/dt = 100A/\mu s$	-	40	-	ns
t_B	$I_F = 4A$, $dI_F/dt = 100A/\mu s$	-	25	-	ns
Q_{RR}	$I_F = 4A$, $dI_F/dt = 100A/\mu s$	-	140	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	15	-	pF
$R_{\theta JC}$		-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figure 9 and Figure 10).

pw = pulse width.

D = duty cycle.

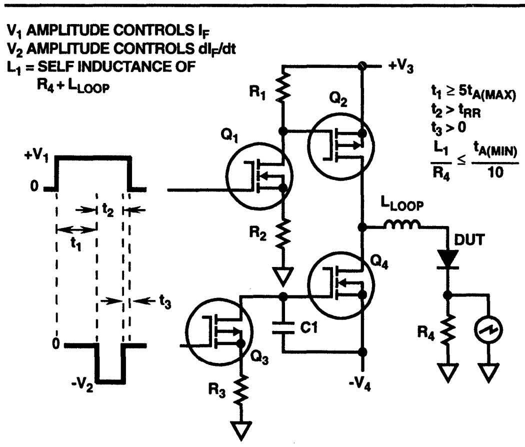


FIGURE 1. t_{RR} TEST CIRCUIT

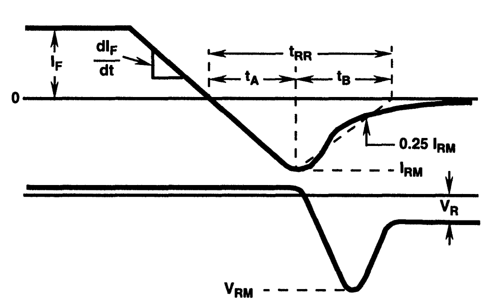


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

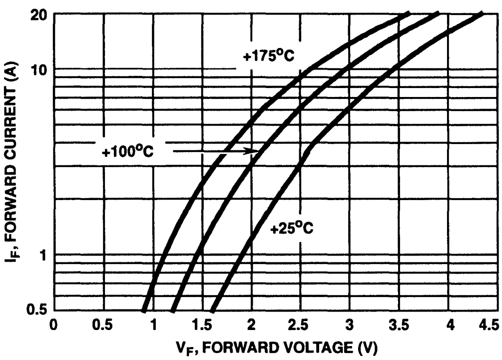


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

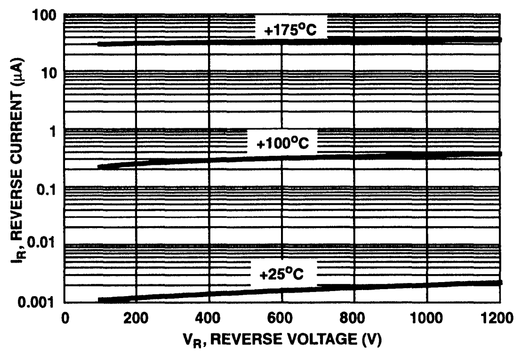


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

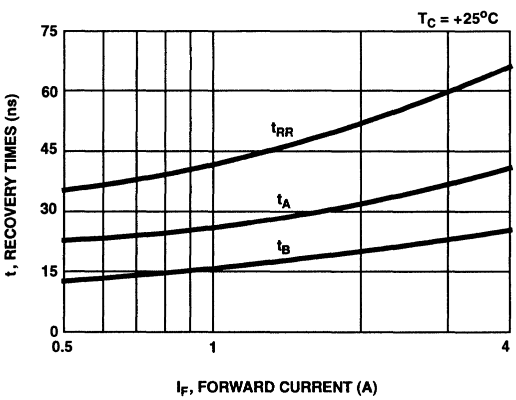


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

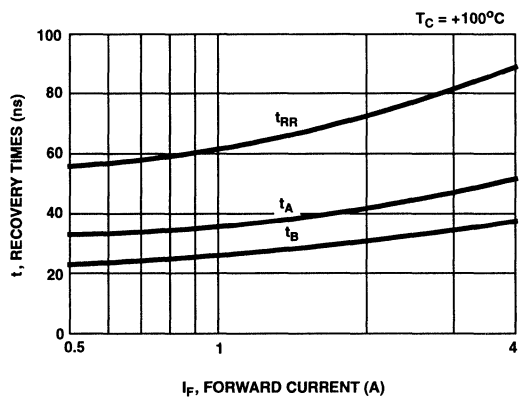


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

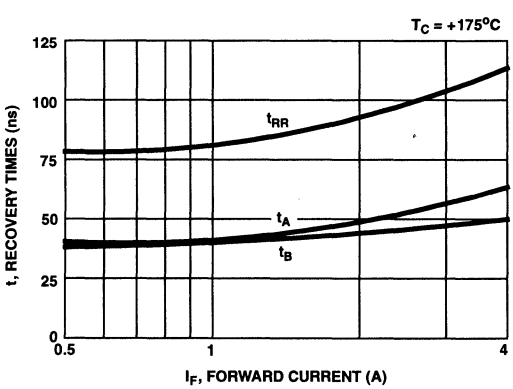


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

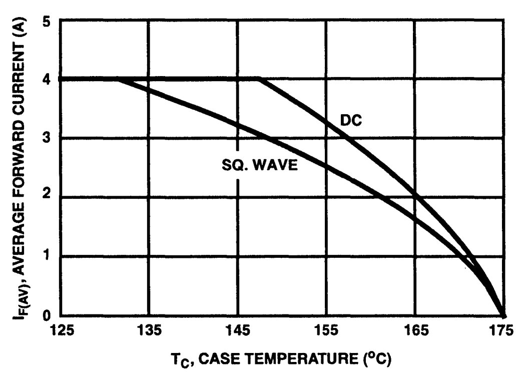


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

7

HYPERFAST SINGLE DIODES

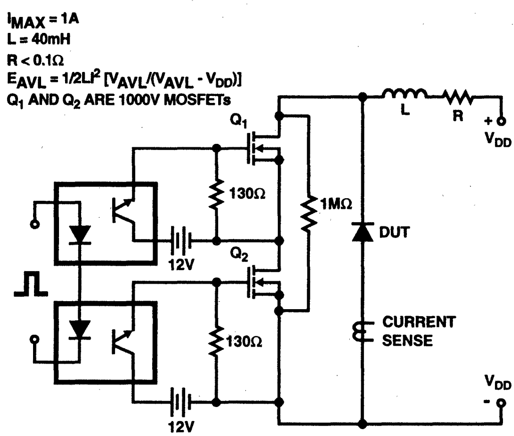


FIGURE 9. AVALANCHE ENERGY TEST CIRCUIT

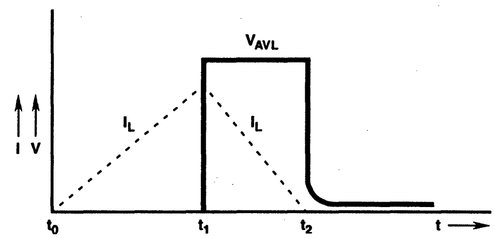


FIGURE 10. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRD640, RHRD650, RHRD660, RHRD640S, RHRD650S, RHRD660S

April 1995

6A, 400V - 600V Hyperfast Diodes

Features

- **Hyperfast with Soft Recovery .... <30ns**
- **Operating Temperature .... +175°C**
- **Reverse Voltage Up To 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRD640, RHRD650, RHRD660, RHRD640S, RHRD650S and RHRD660S are hyperfast diodes with soft recovery characteristics (t_{RR} < 30ns). They have half the recovery time of ultrafast diodes and are sil icon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGE AVAILABILITY

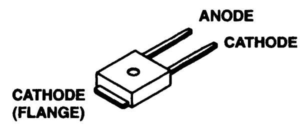
PART NUMBER	PACKAGE	BRAND
RHRD640	TO-251	RHR640
RHRD650	TO-251	RHR650
RHRD660	TO-251	RHR660
RHRD640S	TO-252	RHR640
RHRD650S	TO-252	RHR650
RHRD660S	TO-252	RHR660

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252 variant in tape and reel, e.g. RHRD660S9A.

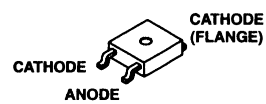
Formerly developmental type TA49057.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

	RHRD640 RHRD640S	RHRD650 RHRD650S	RHRD660 RHRD660S	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	400	500	600	V
Working Peak Reverse Voltage . . . . V_{RWM}	400	500	600	V
DC Blocking Voltage . . . . V_R	400	500	600	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ ($T_C = +152°C$)	6	6	6	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	12	12	12	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	60	60	60	A
Maximum Power Dissipation . . . . P_D	50	50	50	W
Avalanche Energy (See Figures 10 and 11) . . . . E_{AVL}	10	10	10	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3746.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRD640, RHRD640S			RHRD650, RHRD650S			RHRD660, RHRD660S			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 6A, T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 6A, T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	µA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	µA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	µA
t_{RR}	$I_F = 1A, dI_F/dt = 200A/\mu s$	-	-	30	-	-	30	-	-	30	ns
	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	-	35	-	-	35	-	-	35	ns
t_A	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	16	-	-	16	-	-	16	-	ns
t_B	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	8.5	-	-	8.5	-	-	8.5	-	ns
Q_{RR}	$I_F = 6A, dI_F/dt = 200A/\mu s$	-	45	-	-	45	-	-	45	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	20	-	-	20	-	-	20	-	pF
$R_{\theta JC}$		-	-	3	-	-	3	-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

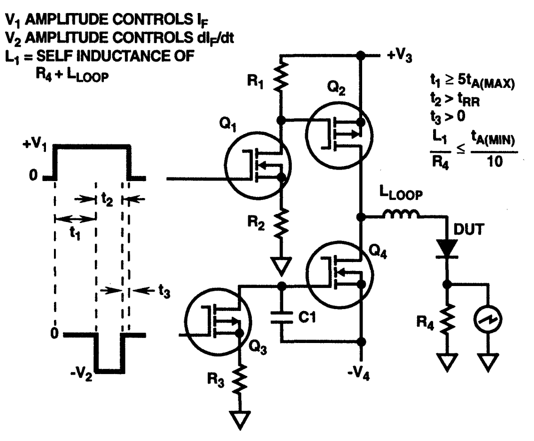


FIGURE 1. t_{RR} TEST CIRCUIT

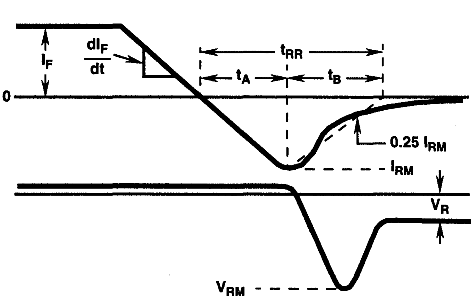


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

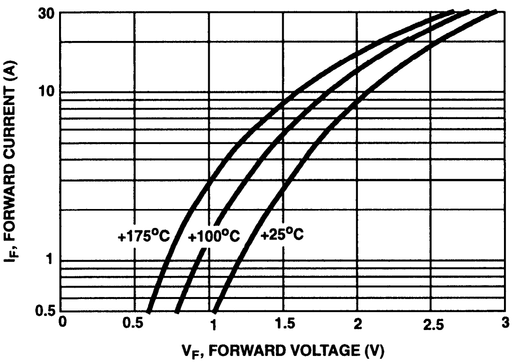


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

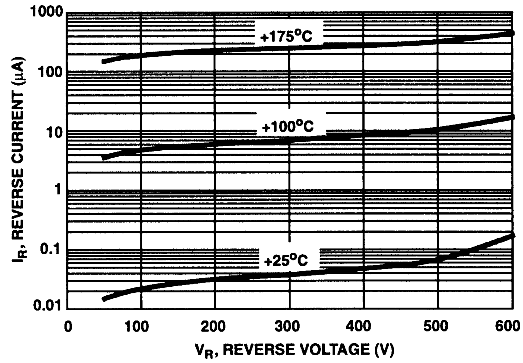


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

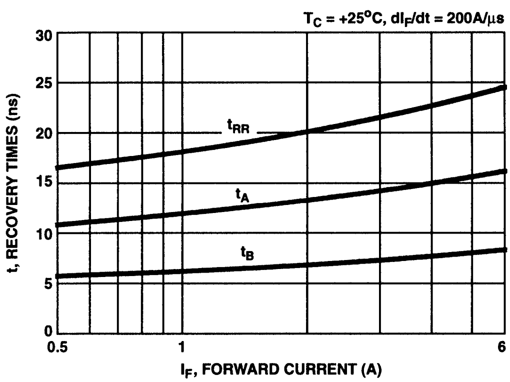


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

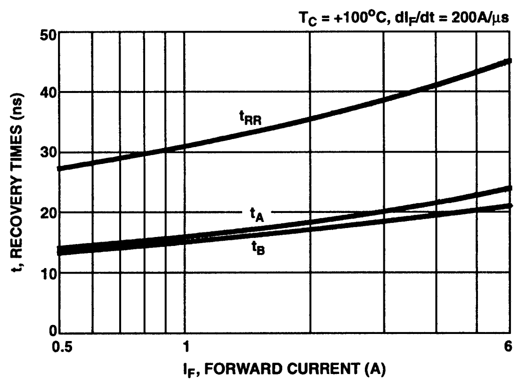


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

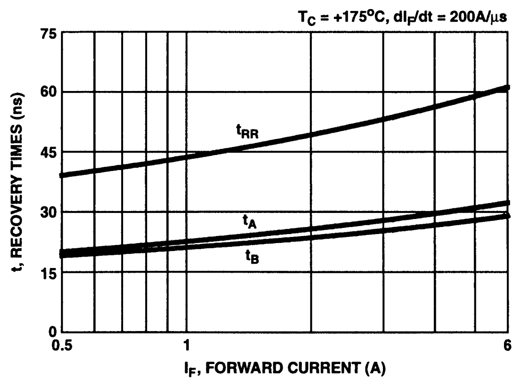


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

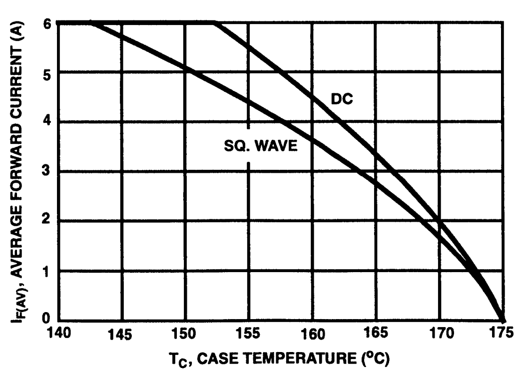


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

7

HYPERFAST SINGLE DIODES

Typical Performance Curves (Continued)

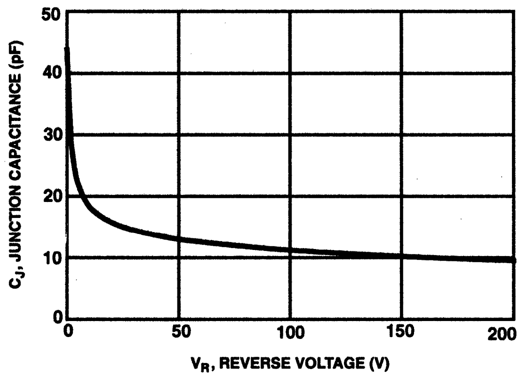


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveform

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

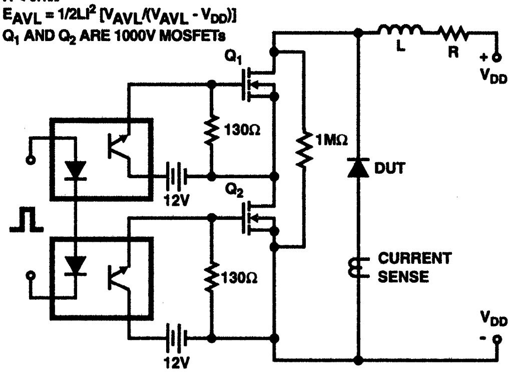


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

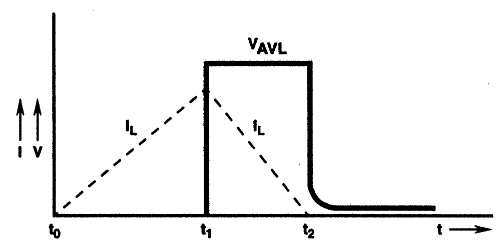


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRD6120, RHRD6120S

HARRIS SEMICONDUCTOR

March 1995

6A, 1200V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery .... <55ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRD6120 and RHRD6120S (TA49058) are hyperfast diodes with soft recovery characteristics (t_{RR} < 55ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

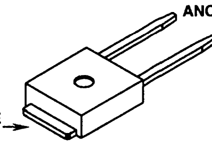
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRD6120	TO-251	HR6120
RHRD6120S	TO-252	HR6120

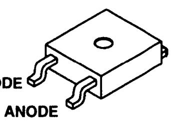
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-251



JEDEC STYLE TO-252



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRD6120 RHRD6120S	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 130°C)	$I_{F(AV)}$	6	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	12	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	60	A
Maximum Power Dissipation	P_D	50	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	10	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number 3981

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 6A, T_C = +25°C	-	-	3.2	V
	I_F = 6A, T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	55	ns
	I_F = 6A, dI_F/dt = 200A/µs	-	-	65	ns
t_A	I_F = 6A, dI_F/dt = 200A/µs	-	33	-	ns
t_B	I_F = 6A, dI_F/dt = 200A/µs	-	22	-	ns
Q_{RR}	I_F = 6A, dI_F/dt = 200A/µs	-	210	-	nC
C_J	V_R = 10V, I_F = 0A	-	22	-	pF
$R_{\theta JC}$		-	-	3	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of t_A + t_B.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

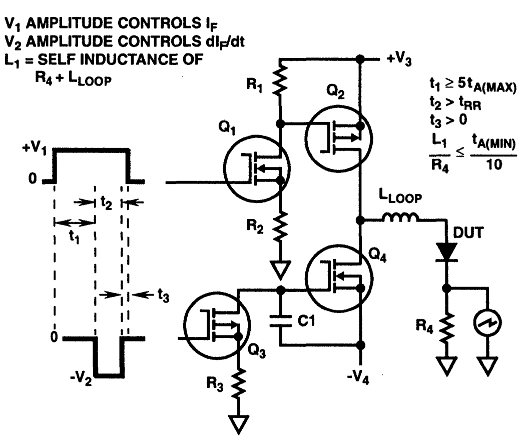


FIGURE 1. t_{RR} TEST CIRCUIT

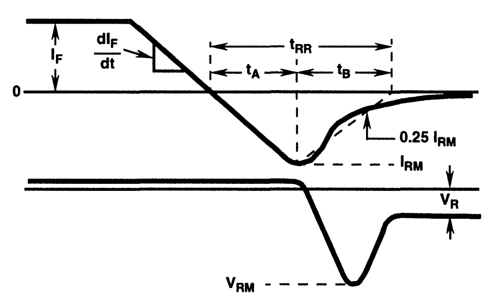


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

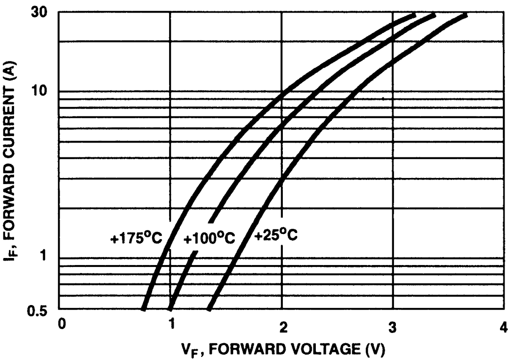


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

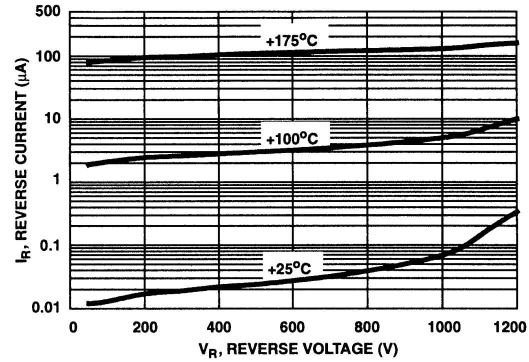


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

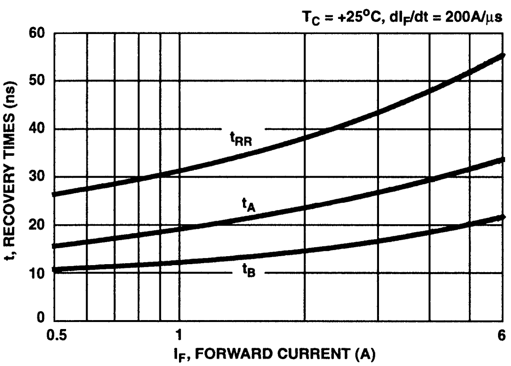


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

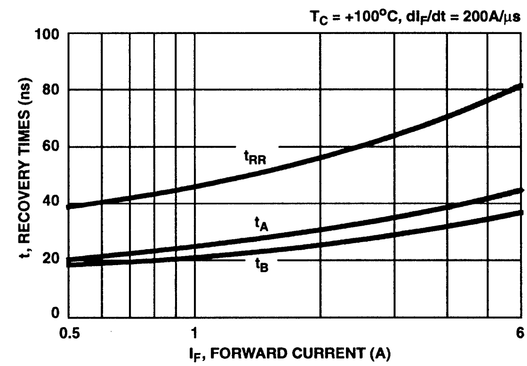


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

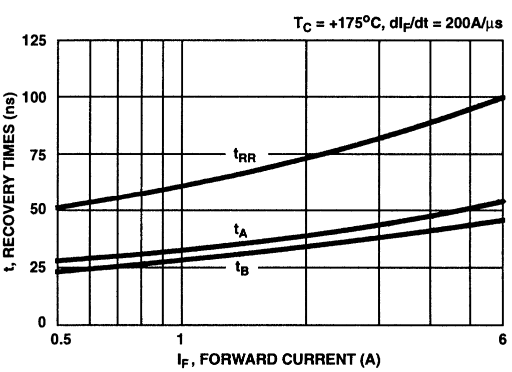


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

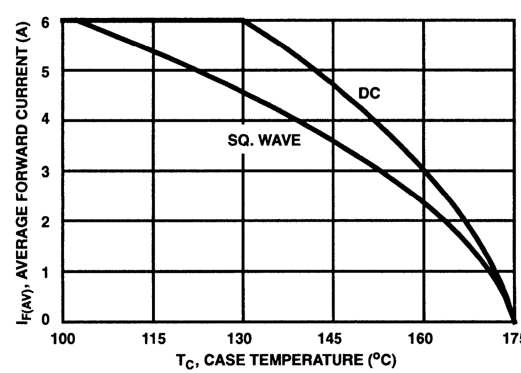


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

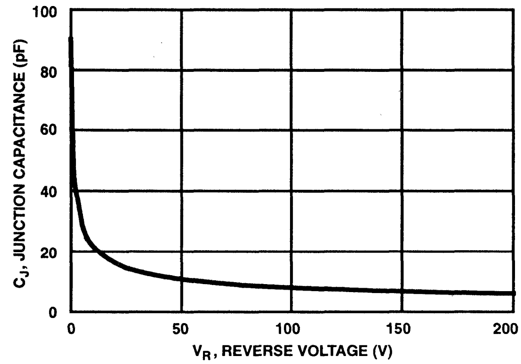


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

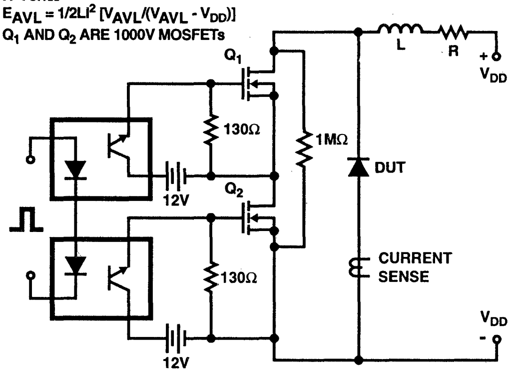


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

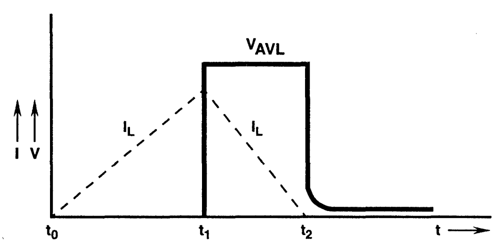


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRG3040, RHRG3050, RHRG3060

April 1995

30A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <40ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG3040, RHRG3050 and RHRG3060 (TA49063) are hyperfast diodes with soft recovery characteristics (t_{RR} < 40ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

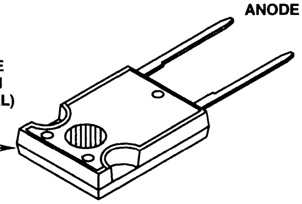
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG3040	TO-247	RHRG3040
RHRG3050	TO-247	RHRG3050
RHRG3060	TO-247	RHRG3060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRG3040	RHRG3050	RHRG3060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +120°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG3040			RHRG3050			RHRG3060			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A, T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 30A, T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	1.0	-	-	-	-	-	-	mA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	1.0	-	-	-	mA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	40	-	-	40	-	-	40	ns
	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	-	45	-	-	45	-	-	45	ns
t_A	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	22	-	-	22	-	-	22	-	ns
t_B	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	20	-	-	20	-	-	20	-	ns
Q_{RR}	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	50	-	-	50	-	-	50	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	85	-	-	85	-	-	85	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

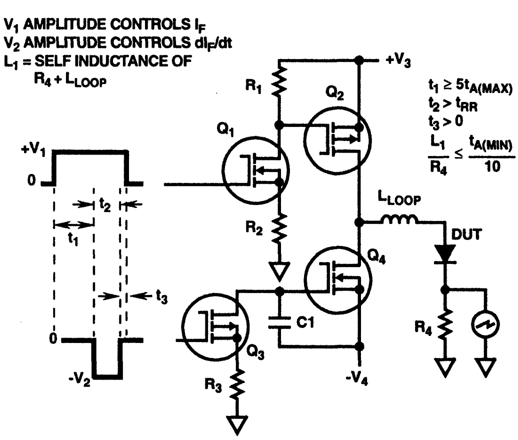


FIGURE 1. t_{RR} TEST CIRCUIT

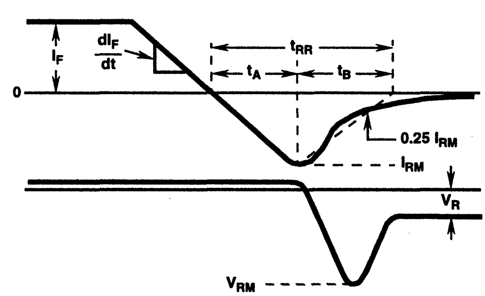


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

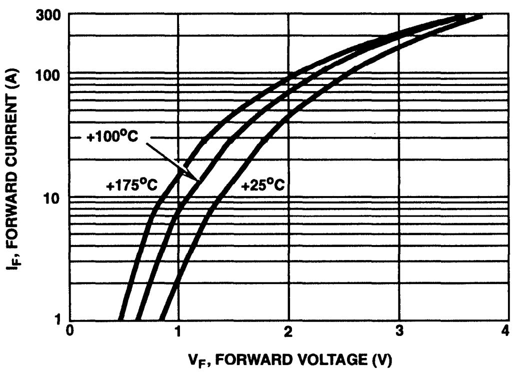


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

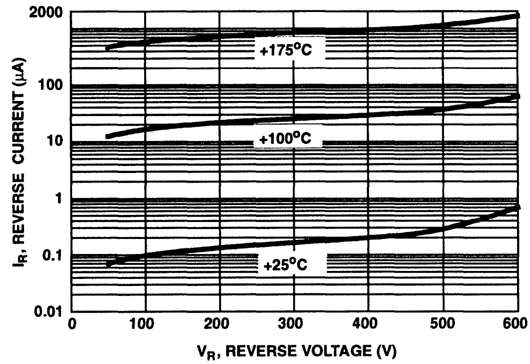


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

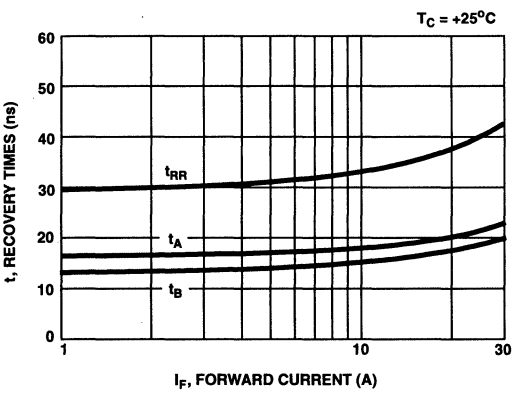


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

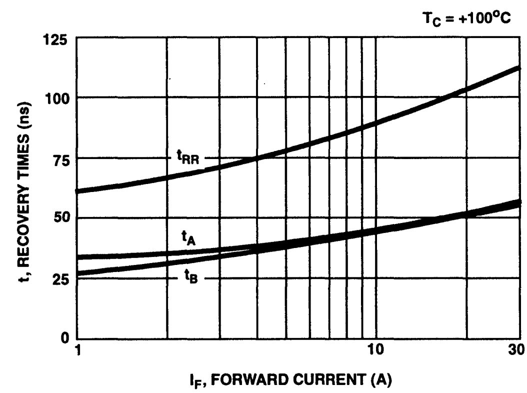


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

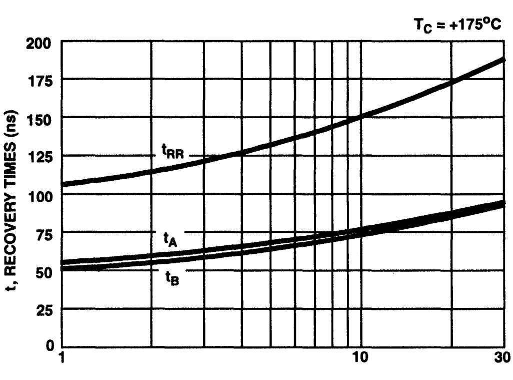


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

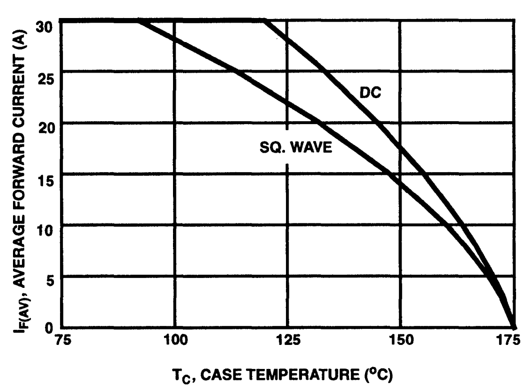


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

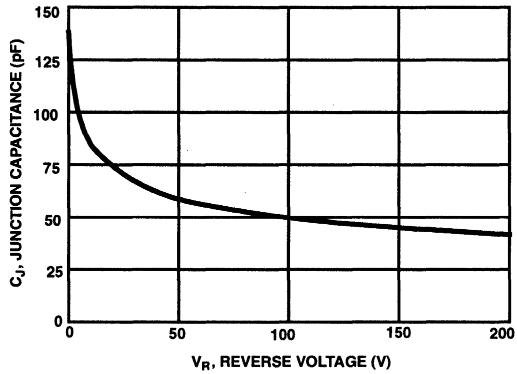


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

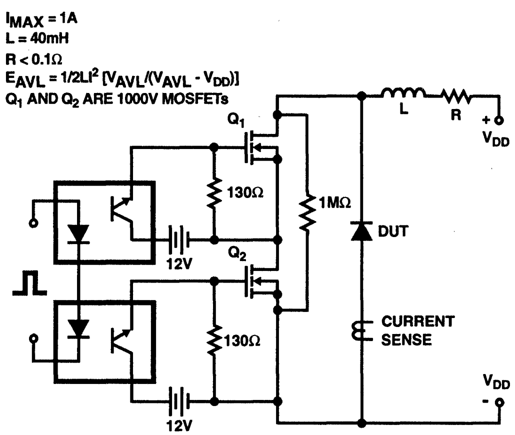


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

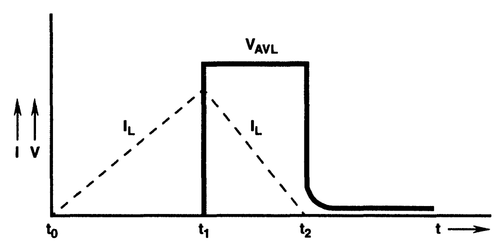


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG3070, RHRG3080, RHRG3090, RHRG30100

April 1995

30A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <65ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG3070, RHRG3080, RHRG3090 and RHRG30100 (TA49064) are hyperfast diodes with soft recovery characteristics (t_{RR} < 65ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

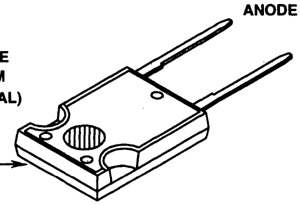
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG3070	TO-247	RHRG3070
RHRG3080	TO-247	RHRG3080
RHRG3090	TO-247	RHRG3090
RHRG30100	TO-247	RHRG30100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		RHRG3070	RHRG3080	RHRG3090	RHRG30100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current ($T_C = +95°C$)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3941.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG3070			RHRG3080			RHRG3090			RHRG30100			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 30A, T_C = +25^oC$	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	$I_F = 30A, T_C = +150^oC$	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	$V_R = 700V, T_C = +25^oC$	-	-	250	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +25^oC$							-	-	500				μA
	$V_R = 1000V, T_C = +25^oC$	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 700V, T_C = +150^oC$	-	-	1.0	-	-	-	-	-	-	-	-	-	mA
	$V_R = 800V, T_C = +150^oC$	-	-	-	-	-	1.0	-	-	-	-	-	-	mA
	$V_R = 900V, T_C = +150^oC$							-	-	1.0				mA
	$V_R = 1000V, T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	65	-	-	65	-	-	65	-	-	65	ns
	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	-	75	-	-	75	-	-	75	-	-	75	ns
t_A	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	35	-	-	35	-	-	35	-	-	35	-	ns
t_B	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	33	-	-	33	-	-	33	-	-	33	-	ns
Q_{RR}	$I_F = 30A, dI_F/dt = 100A/\mu s$	-	200	-	-	200	-	-	200	-	-	200	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	100	-	-	100	-	-	100	-	-	100	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2			1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

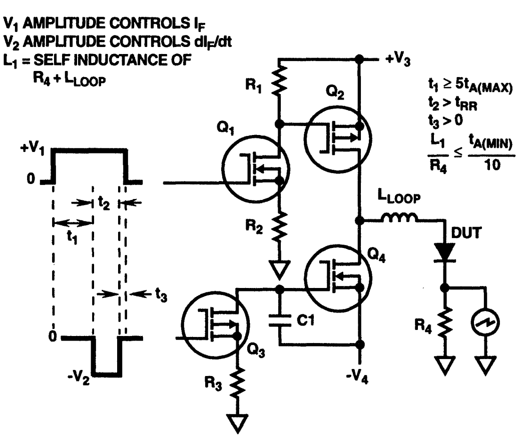


FIGURE 1. t_{RR} TEST CIRCUIT

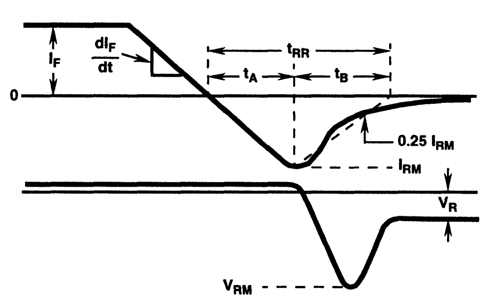


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

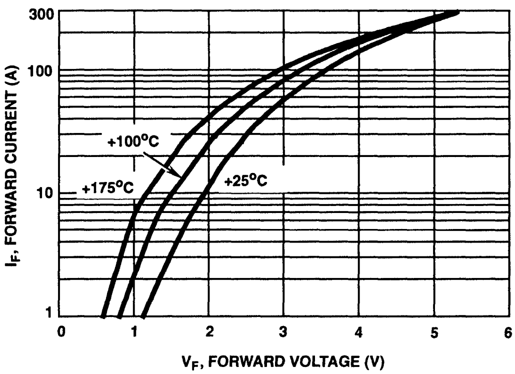


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

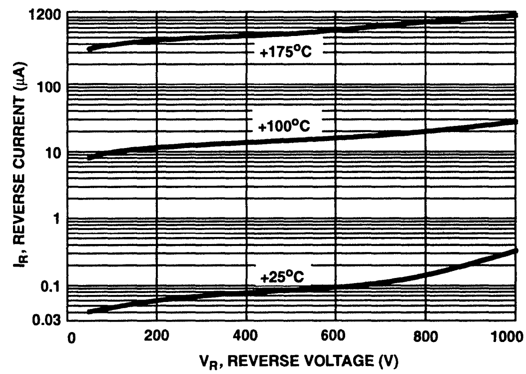


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

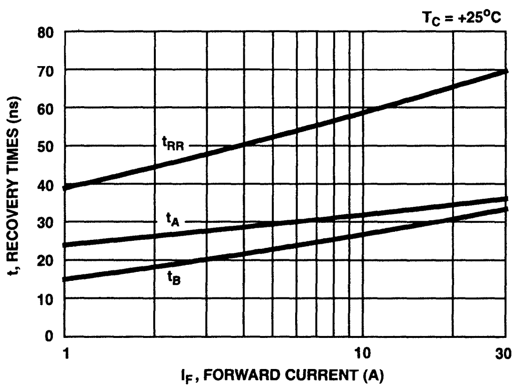


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

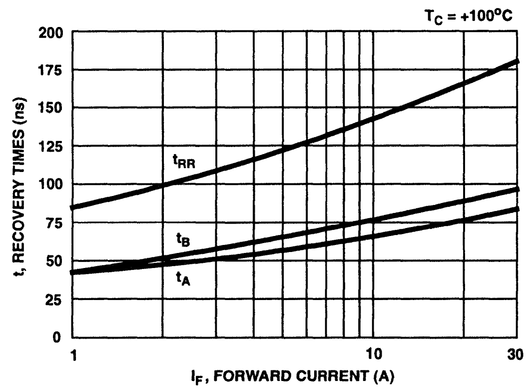


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

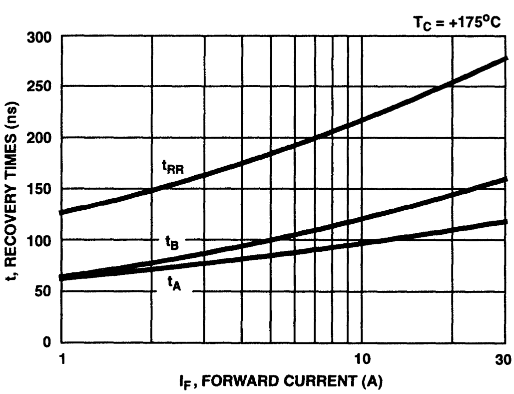


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

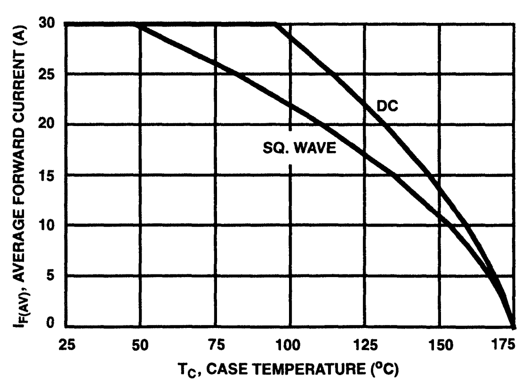


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

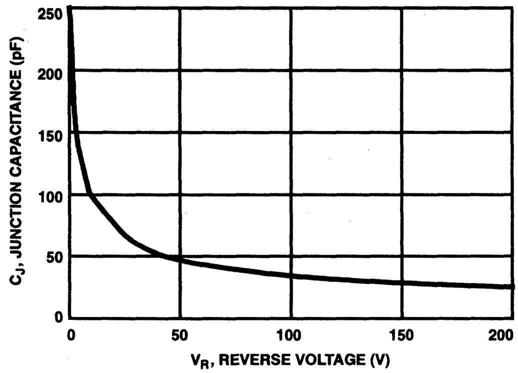


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

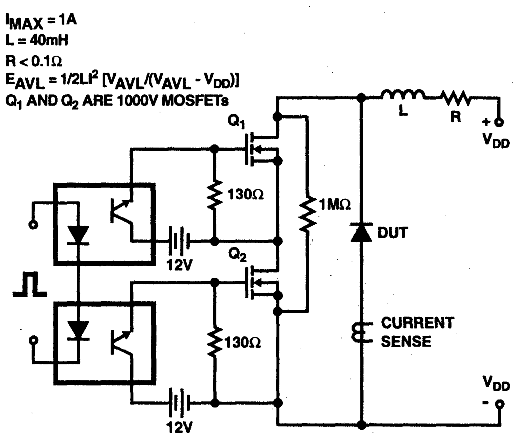


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

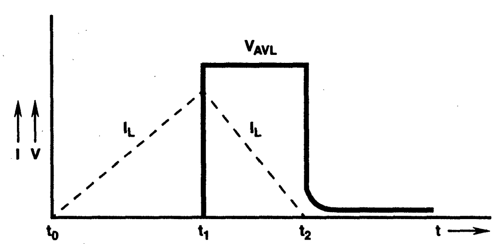


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG30120

April 1995

30A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <65ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRG30120 (TA49041) is a hyperfast diode with soft recovery characteristics (t_{RR} < 65ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of high frequency switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

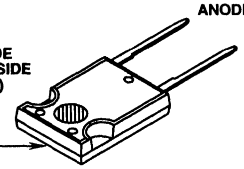
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG30120	TO-247	RHRG30120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

HYPERFAST SINGLE DIODES

7

Absolute Maximum Ratings $T_C = +25°C$

		RHRG30120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current ($T_C = +78°C$)	$I_{F(AV)}$	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	A
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 30A		-	-	3.2	V
V_F	I_F = 30A	T_C = +150°C	-	-	2.6	
I_R	V_R = 1200V		-	-	500	μA
I_R	V_R = 1200V	T_C = +150°C	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	65	ns
t_{RR}	I_F = 30A, dI_F/dt = 100A/μs		-	-	75	
t_A	I_F = 30A, dI_F/dt = 100A/μs		-	48	-	
t_B	I_F = 30A, dI_F/dt = 100A/μs		-	22	-	
$R_{\theta JC}$			-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

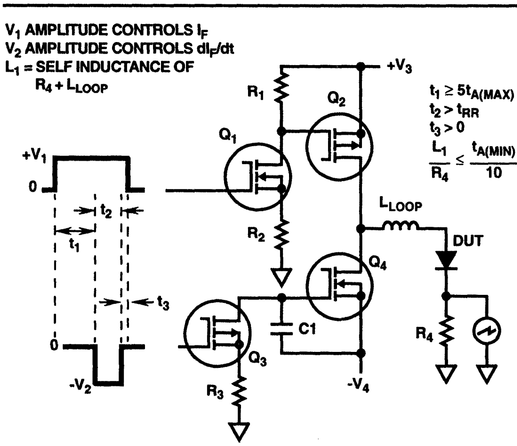


FIGURE 1. t_{RR} TEST CIRCUIT

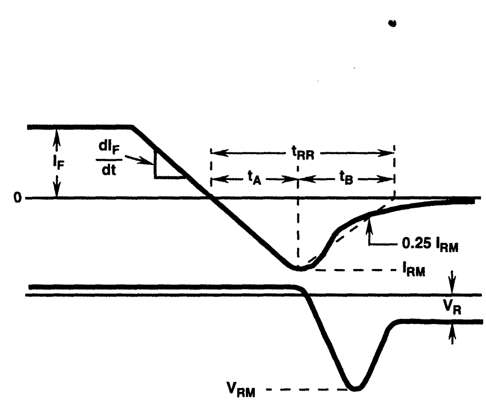


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

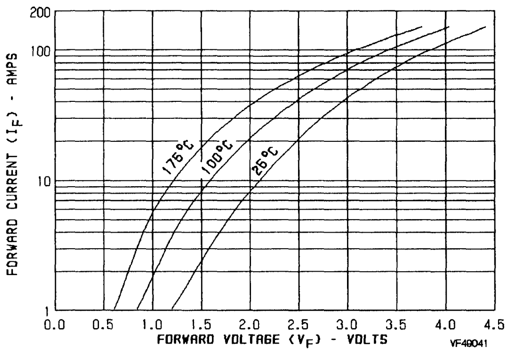


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

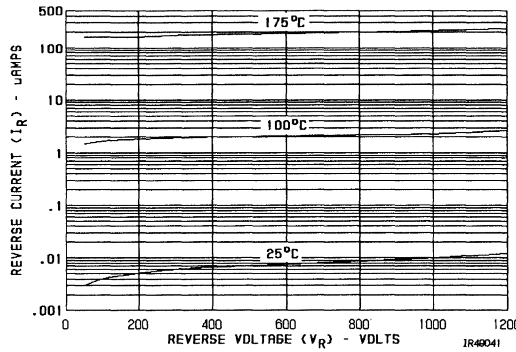


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

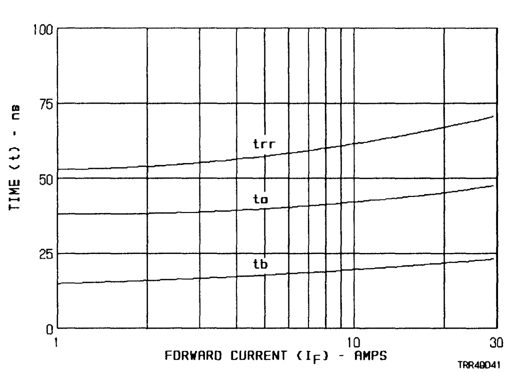


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

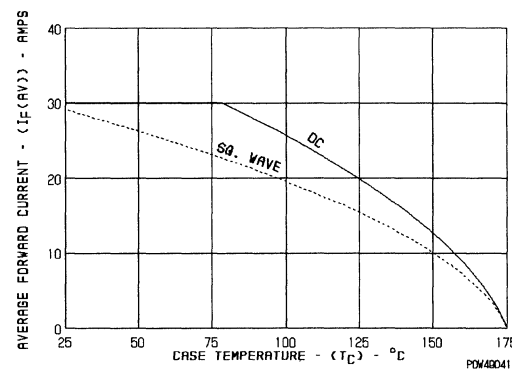


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

$I_{MAX} = 1A$
$L = 40mH$
$R < 0.1\Omega$
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

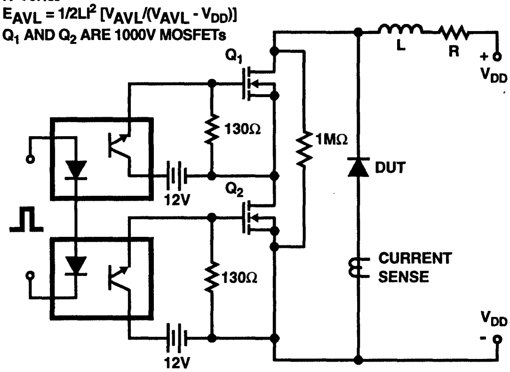


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

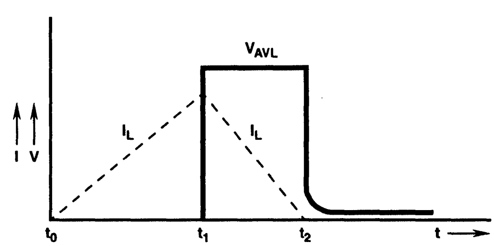


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG5040, RHRG5050, RHRG5060

April 1995

50A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <45ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG5040, RHRG5050 and RHRG5060 (TA49065) are hyperfast diodes with soft recovery characteristics (t_{RR} <45ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

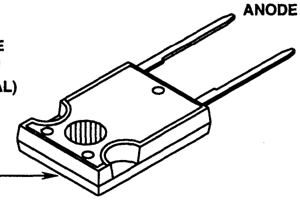
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG5040	TO-247	RHRG5040
RHRG5050	TO-247	RHRG5050
RHRG5060	TO-247	RHRG5060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	RHRG5040	RHRG5050	RHRG5060	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	400	500	600	V
Working Peak Reverse Voltage . . . . V_{RWM}	400	500	600	V
DC Blocking Voltage . . . . V_R	400	500	600	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ (T_C = +93°C)	50	50	50	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	100	100	100	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	500	500	500	A
Maximum Power Dissipation . . . . P_D	150	150	150	W
Avalanche Energy (L = 40mH) . . . . E_{AVL}	40	40	40	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG5040			RHRG5050			RHRG5060			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 50A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
	I_F = 50A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = +150°C	-	-	1.5	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	1.5	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	45	-	-	45	-	-	45	ns
	I_F = 50A, dI_F/dt = 100A/µs	-	-	50	-	-	50	-	-	50	ns
t_A	I_F = 50A, dI_F/dt = 100A/µs	-	25	-	-	25	-	-	25	-	ns
t_B	I_F = 50A, dI_F/dt = 100A/µs	-	20	-	-	20	-	-	20	-	ns
Q_{RR}	I_F = 50A, dI_F/dt = 100A/µs	-	65	-	-	65	-	-	65	-	nC
C_J	V_R = 10V, I_F = 0A	-	140	-	-	140	-	-	140	-	pF
$R_{\theta JC}$		-	-	1.0	-	-	1.0	-	-	1.0	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = Duty cycle.

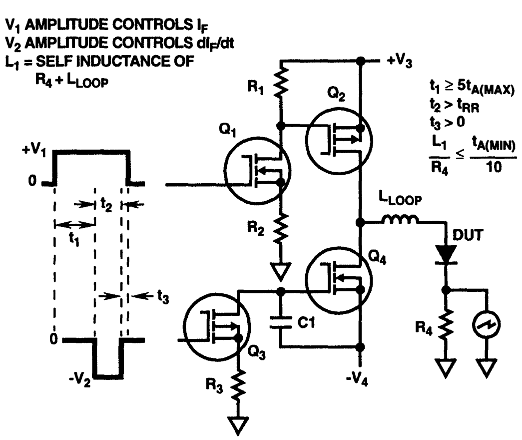


FIGURE 1. t_{RR} TEST CIRCUIT

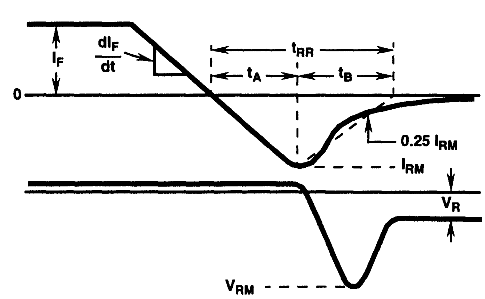


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

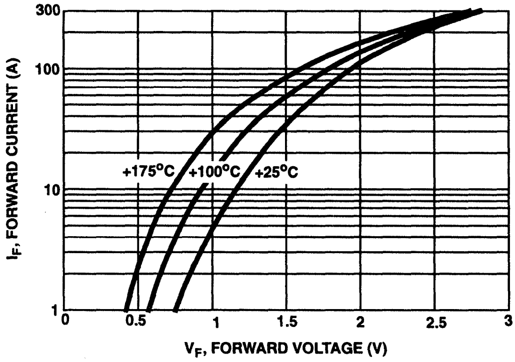


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

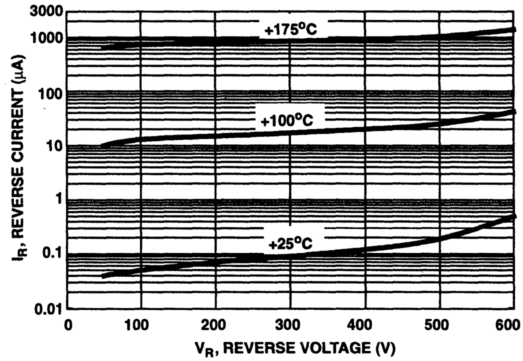


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

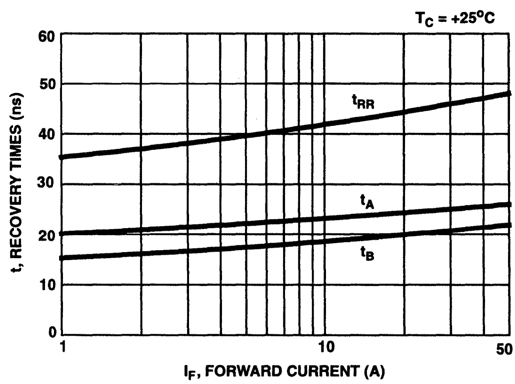


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

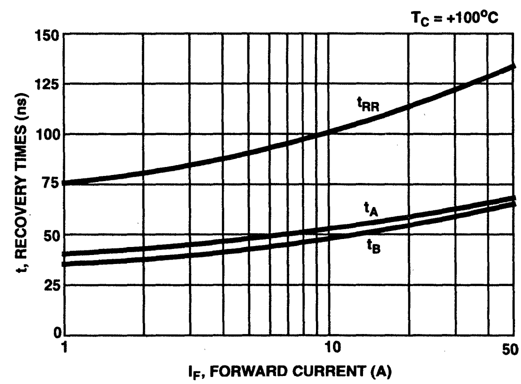


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

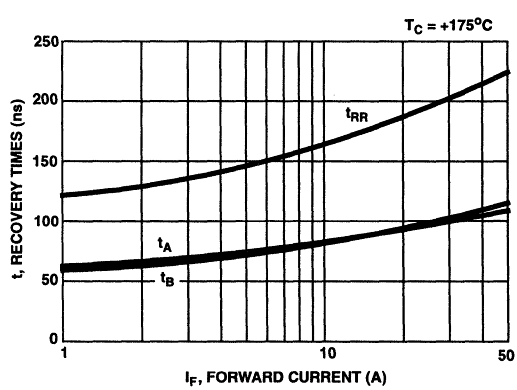


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

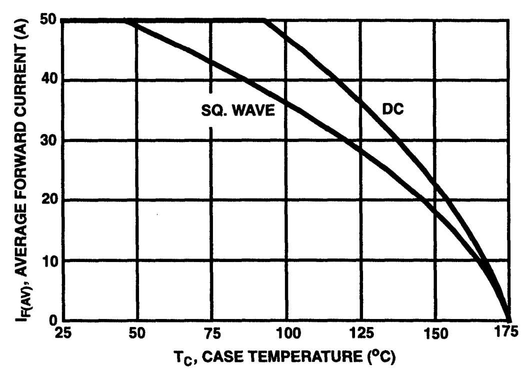


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

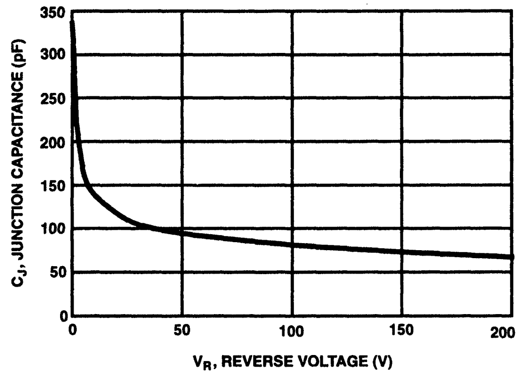


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

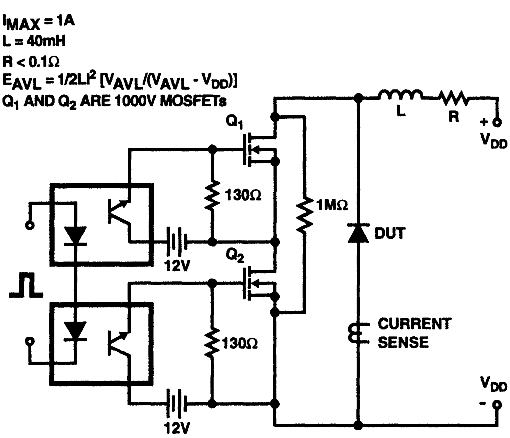


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

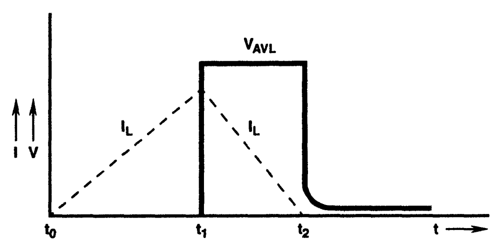


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG5070, RHRG5080, RHRG5090, RHRG50100

April 1995

50A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <75ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG5070, RHRG5080, RHRG5090 and RHRG50100 (TA49066) are hyperfast diodes with soft recovery characteristics (t_{RR} < 75ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

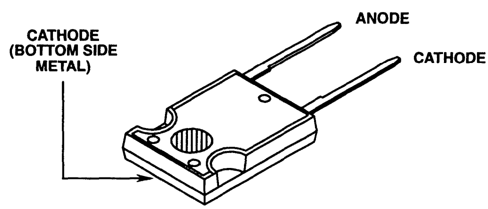
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG5070	TO-247	RHRG5070
RHRG5080	TO-247	RHRG5080
RHRG5090	TO-247	RHRG5090
RHRG50100	TO-247	RHRG50100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE 2 LEAD TO-247



Symbol

Absolute Maximum Ratings $T_C = +25^oC$

		RHRG5070	RHRG5080	RHRG5090	RHRG50100
Peak Repetitive Reverse Voltage	V_{RRM}	700V	800V	900V	1000V
Working Peak Reverse Voltage	V_{RWM}	700V	800V	900V	1000V
DC Blocking Voltage	V_R	700V	800V	900V	1000V
Average Rectified Forward Current ($T_C = +60^oC$)	$I_{F(AV)}$	50A	50A	50A	50A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100A	100A	100A	100A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500A	500A	500A	500A
Maximum Power Dissipation	P_D	150W	150W	150W	150W
Avalanche Energy (L = 40mH)	E_{AVL}	40mj	40mj	40mj	40mj
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RHRG5070 LIMITS MIN	TYP	MAX	RHRG5080 LIMITS MIN	TYP	MAX	RHRG5090 LIMITS MIN	TYP	MAX	RHRG50100 LIMITS MIN	TYP	MAX	UNITS
V_F	$I_F = 50A$		-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
V_F	$I_F = 50A$	$T_C = +150^oC$	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	$V_R = 700V$		-	-	500	-	-	-		-	-	-	-	-	μA
	$V_R = 800V$		-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V$		-	-	-	-	-	-	-	-	500	-	-	-	μA
	$V_R = 1000V$		-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 700V$	$T_C = +150^oC$	-	-	3.0	-	-	-	-	-	-	-	-	-	mA
	$V_R = 800V$	$T_C = +150^oC$	-	-	-	-	-	3.0	-	-	-	-	-	-	mA
	$V_R = 900V$	$T_C = +150^oC$	-	-	-	-	-	-	-	-	3.0	-	-	-	mA
	$V_R = 1000V$	$T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	3.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$		-	-	75	-	-	75	-	-	75	-	-	75	ns
t_{RR}	$I_F = 50A$, $dI_F/dt = 100A/\mu s$		-	-	95	-	-	95	-	-	95	-	-	95	ns
t_A	$I_F = 50A$, $dI_F/dt = 100A/\mu s$		-	54	-	-	54	-	-	54	-	-	54	-	ns
t_B	$I_F = 50A$, $dI_F/dt = 100A/\mu s$		-	32	-	-	32	-	-	32	-	-	32	-	ns
$R_{\theta JC}$			-	-	1.0	-	-	1.0	-	-	1.0	-	-	1.0	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

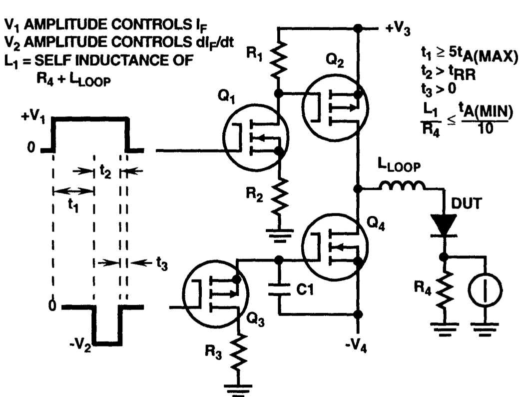


FIGURE 1. t_{RR} TEST CIRCUIT

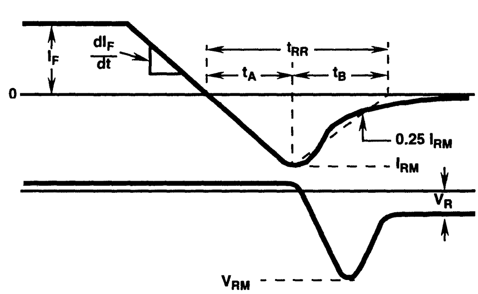


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

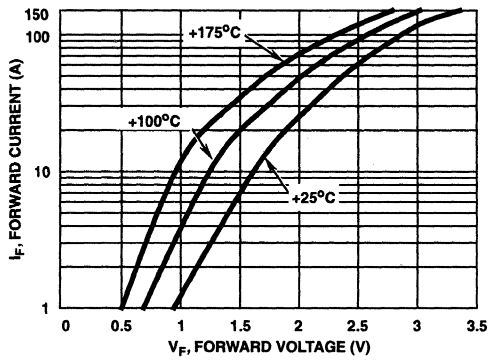


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

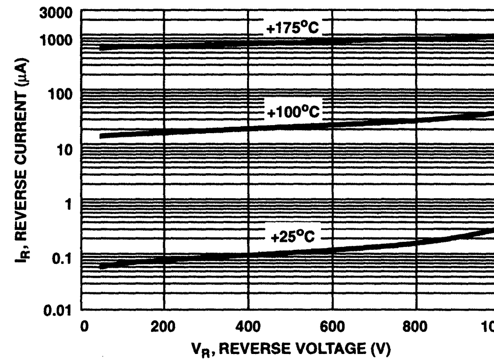


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

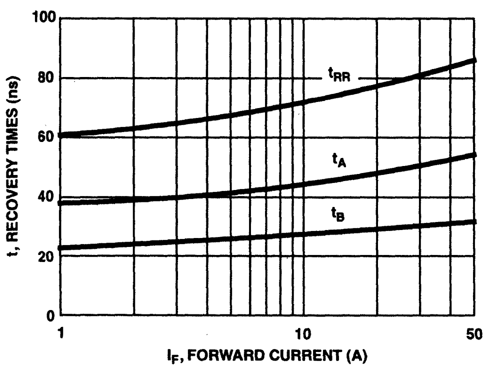


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

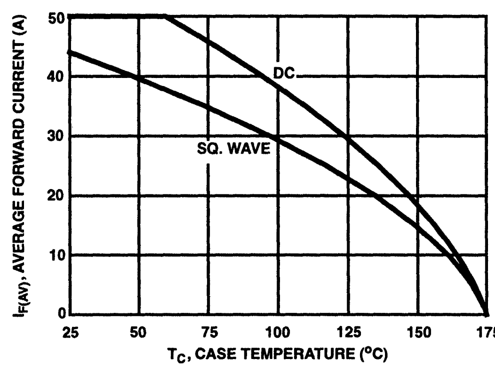


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

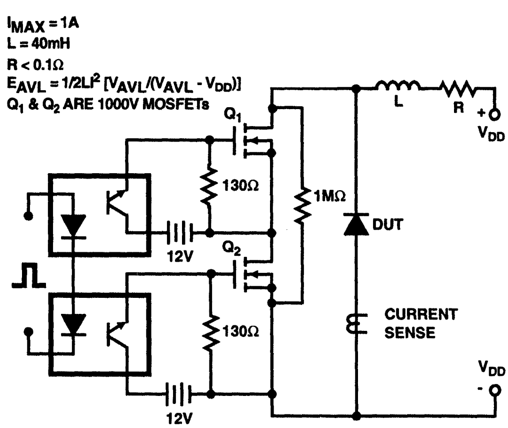


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

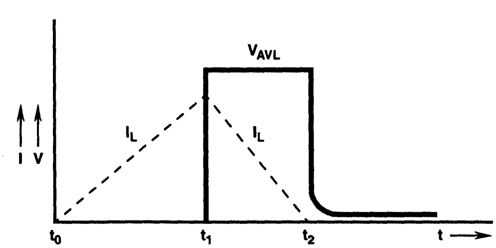


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG50120

April 1995

50A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRG50120 (TA49100) are hyperfast diodes with soft recovery characteristics (t_{RR} < 85ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

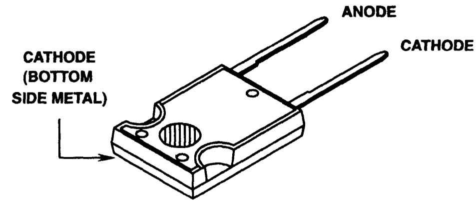
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG50120	TO-247	RHRG50120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRG50120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 50°C)	$I_{F(AV)}$	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	150	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3947.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
V_F	$I_F = 50A$, $T_C = +25^oC$	-	-	3.2	V
	$I_F = 50A$, $T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	500	µA
	$V_R = 1200V$, $T_C = +150^oC$	-	-	1.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	85	ns
	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	-	100	ns
t_A	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	50	-	ns
t_B	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	40	-	ns
Q_{RR}	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	240	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	150	-	pF
$R_{\theta JC}$		-	-	1.0	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

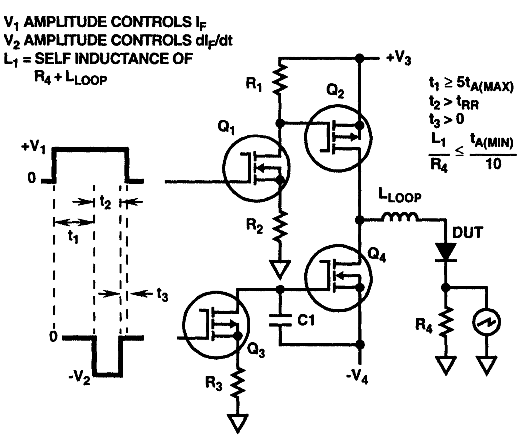


FIGURE 1. t_{RR} TEST CIRCUIT

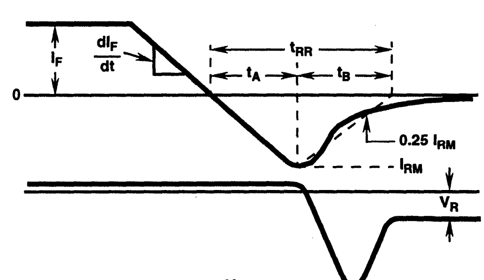


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

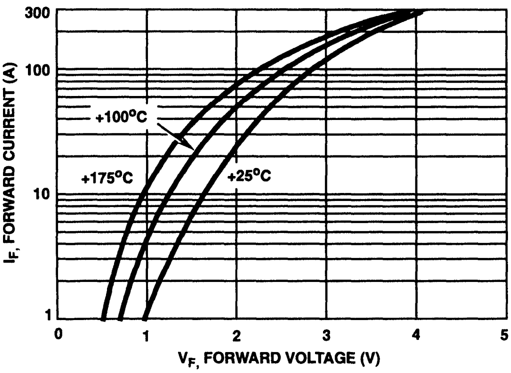


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

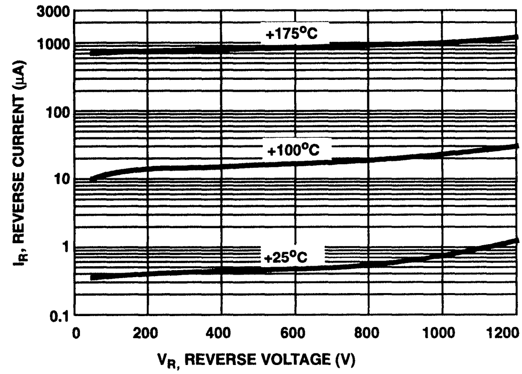


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

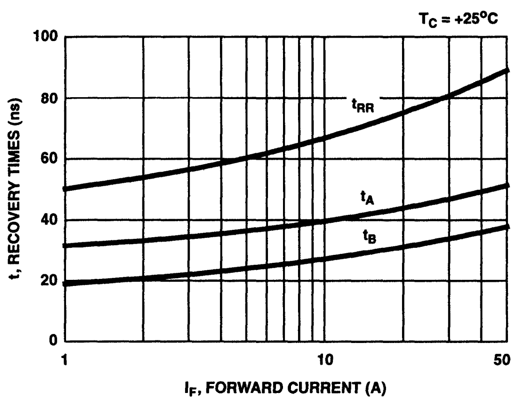


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

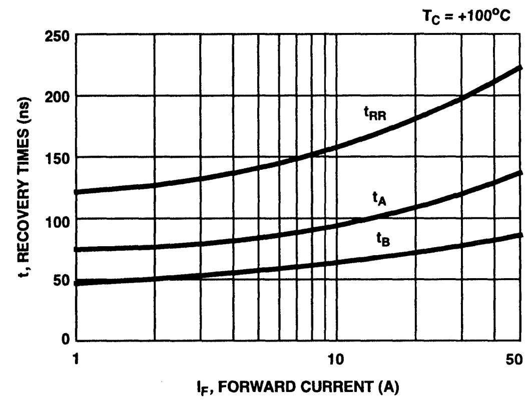


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

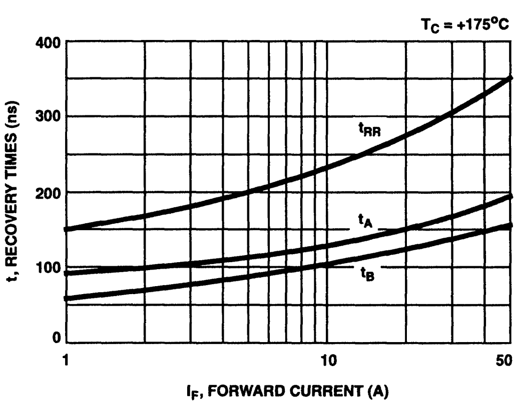


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

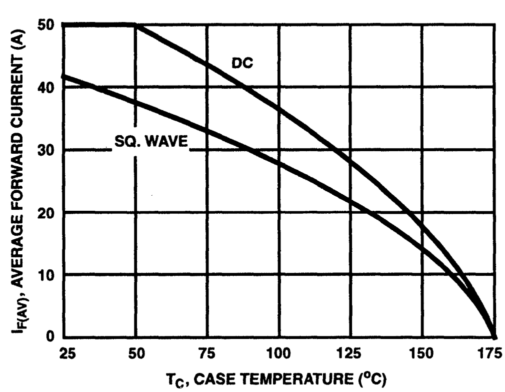


FIGURE 8. CURRENT DERATING CURVE

7

HYPERFAST SINGLE DIODES

Typical Performance Curves (Continued)

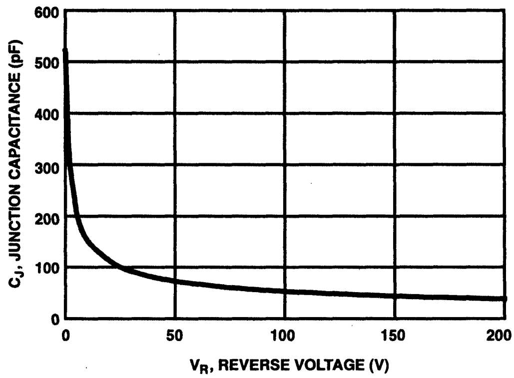


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

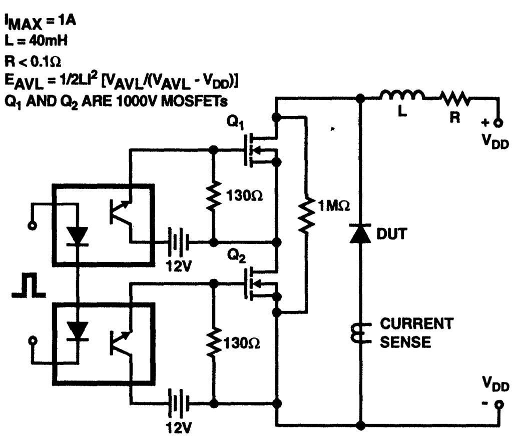


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

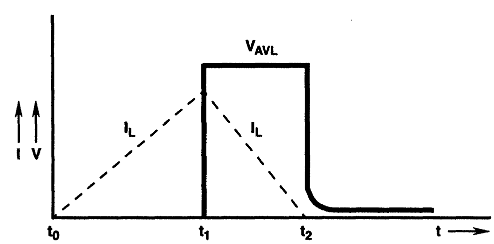


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRG7540, RHRG7550, RHRG7560

April 1995

75A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG7540, RHRG7550 and RHRG7560 are hyperfast diodes with soft recovery characteristics (t_{RR} < 55ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGING AVAILABILITY

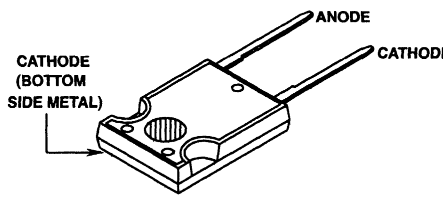
PART NUMBER	PACKAGE	BRAND
RHRG7540	TO-247	RHRG7540
RHRG7550	TO-247	RHRG7550
RHRG7560	TO-247	RHRG7560

NOTE: When ordering, use the entire part number.

Formerly developmental type TA49067.

Package

JEDEC STYLE TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRG7540	RHRG7550	RHRG7560	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +80°C)	$I_{F(AV)}$	75	75	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	150	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	750	750	750	A
Maximum Power Dissipation	P_D	190	190	190	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG7540			RHRG7550			RHRG7560			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 75A$, $T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 75A$, $T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V$, $T_C = +25^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V$, $T_C = +25^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V$, $T_C = +25^oC$	-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 400V$, $T_C = +150^oC$	-	-	2.0	-	-	-	-	-	-	mA
	$V_R = 500V$, $T_C = +150^oC$	-	-	-	-	-	2.0	-	-	-	mA
	$V_R = 600V$, $T_C = +150^oC$	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	-	55	-	-	55	-	-	55	ns
	$I_F = 75A$, $dI_F/dt = 200A/\mu s$	-	-	60	-	-	60	-	-	60	ns
t_A	$I_F = 75A$, $dI_F/dt = 200A/\mu s$	-	27	-	-	27	-	-	27	-	ns
t_B	$I_F = 75A$, $dI_F/dt = 200A/\mu s$	-	23	-	-	23	-	-	23	-	ns
Q_{RR}	$I_F = 75A$, $dI_F/dt = 200A/\mu s$	-	140	-	-	140	-	-	140	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	200	-	-	200	-	-	200	-	pF
$R_{\theta JC}$		-	-	0.8	-	-	0.8	-	-	0.8	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current .

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

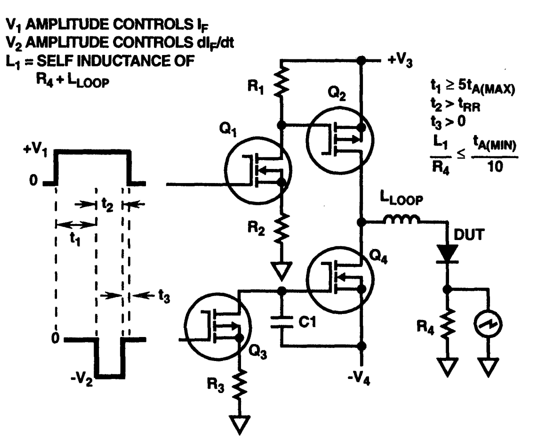


FIGURE 1. t_{RR} TEST CIRCUIT

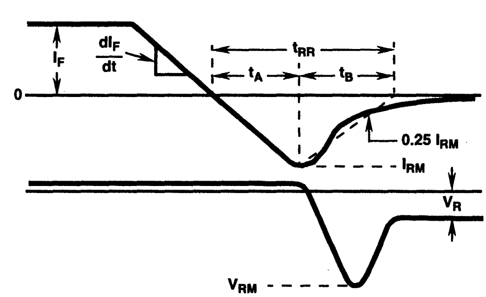


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

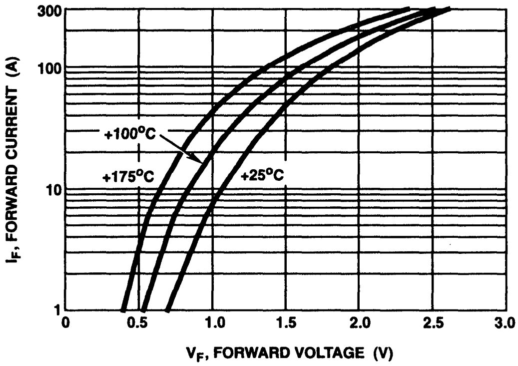


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

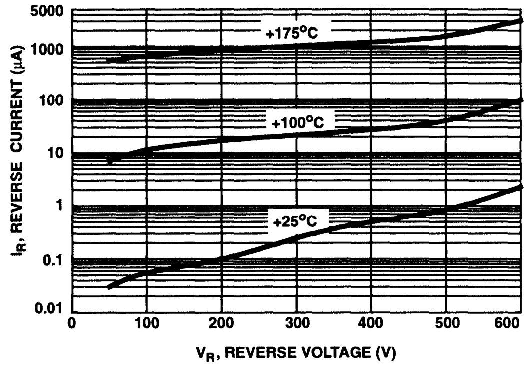


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

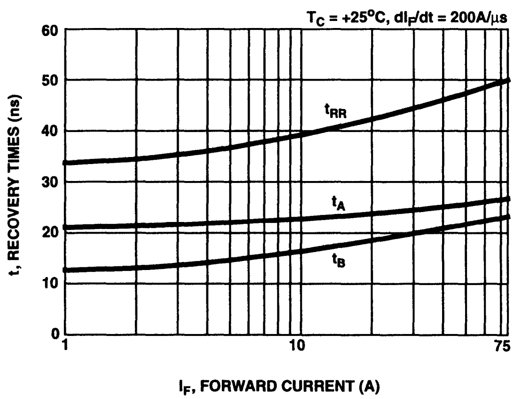


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

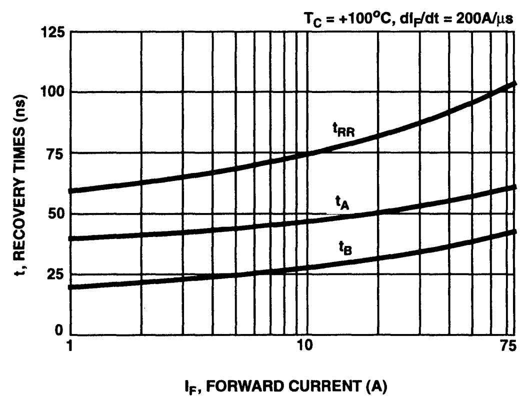


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

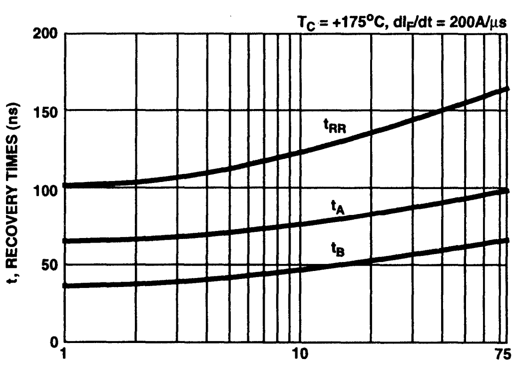


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

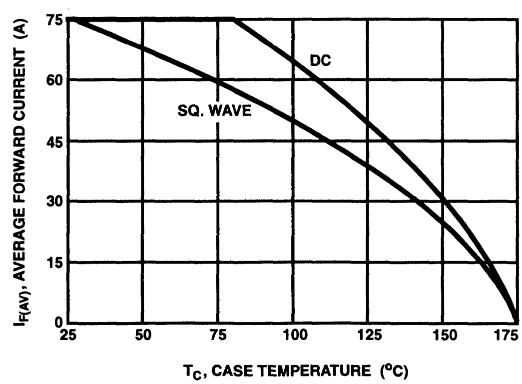


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

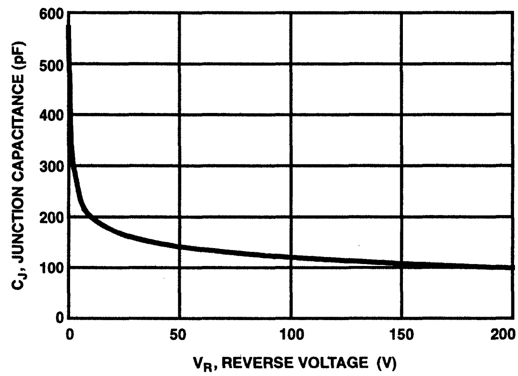


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

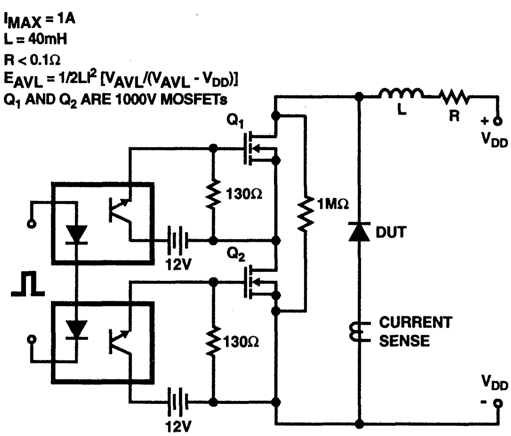


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

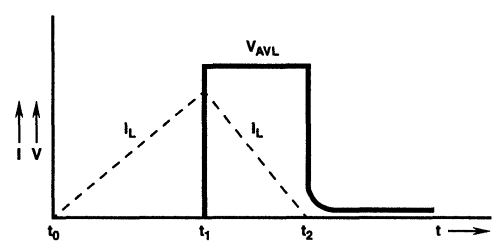


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRG7570, RHRG7580, RHRG7590, RHRG75100

April 1995

75A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery .... <85ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG7570, RHRG7580, RHRG7590 and RHRG75100 (TA49068) are hyperfast diodes with soft recovery characteristics (t_{RR} < 85ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

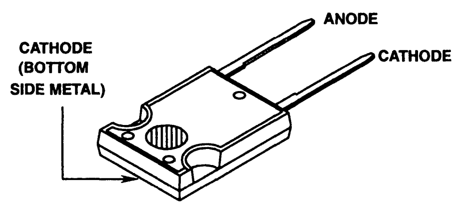
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG7570	TO-247	RHRG7570
RHRG7580	TO-247	RHRG7580
RHRG7590	TO-247	RHRG7590
RHRG75100	TO-247	RHRG75100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	RHRG7570	RHRG7580	RHRG7590	RHRG75100	UNITS
Peak Repetitive Reverse Voltage ..... V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage ..... V_{RWM}	700	800	900	1000	V
DC Blocking Voltage ..... V_R	700	800	900	1000	V
Average Rectified Forward Current ..... $I_{F(AV)}$ (T_C = +52°C)	75	75	75	75	A
Repetitive Peak Surge Current ..... I_{FSM} (Square Wave, 20kHz)	150	150	150	150	A
Nonrepetitive Peak Surge Current ..... I_{FSM} (Halfwave, 1 Phase, 60Hz)	750	750	750	750	A
Maximum Power Dissipation ..... P_D	190	190	190	190	W
Avalanche Energy (L = 40mH) (See Figures 10 and 11) ..... E_{AVL}	50	50	50	50	mj
Operating and Storage Temperature ..... T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3923.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		RHRG7570			RHRG7580			RHRG7590			RHRG75100			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 75A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 75A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	2.0	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	2.0	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	2.0	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	85	-	-	85	-	-	85	-	-	85	ns
	I_F = 75A, dI_F/dt = 100A/μs	-	-	100	-	-	100	-	-	100	-	-	100	ns
t_A	I_F = 75A, dI_F/dt = 100A/μs	-	55	-	-	55	-	-	55	-	-	55	-	ns
t_B	I_F = 75A, dI_F/dt = 100A/μs	-	40	-	-	40	-	-	40	-	-	40	-	ns
Q_{RR}	I_F = 75A, dI_F/dt = 100A/μs	-	240	-	-	240	-	-	240	-	-	240	-	nC
C_J	V_R = 10V, I_F = 0A	-	220	-	-	220	-	-	220	-	-	220	-	pF
$R_{\theta JC}$		-	-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

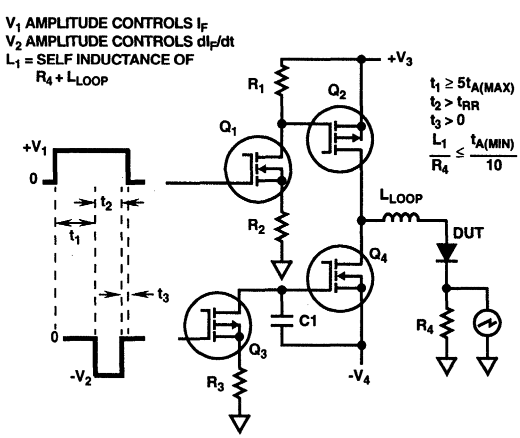


FIGURE 1. t_{RR} TEST CIRCUIT

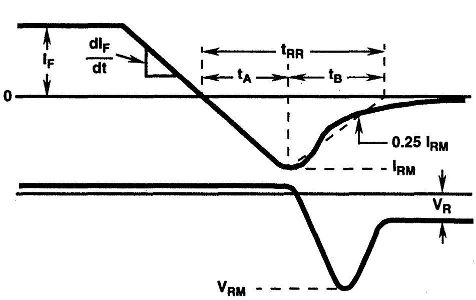


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

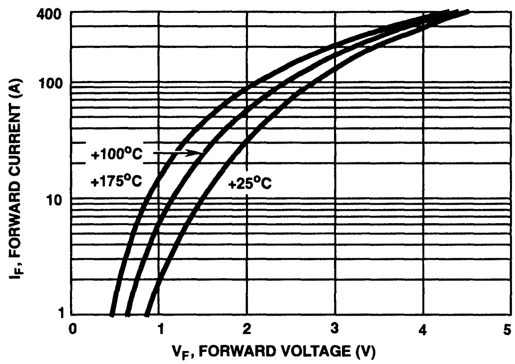


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

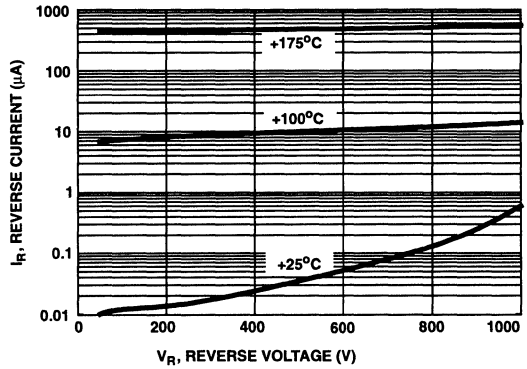


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

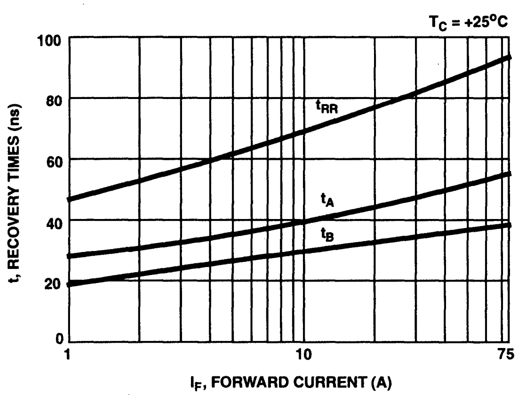


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

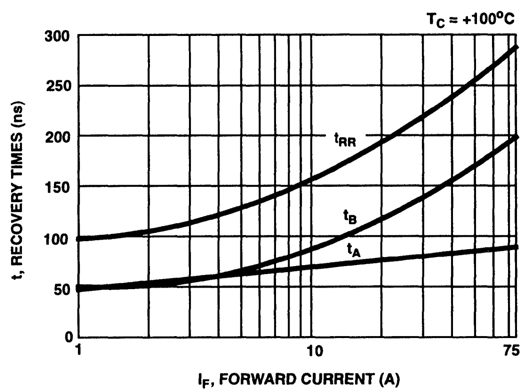


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

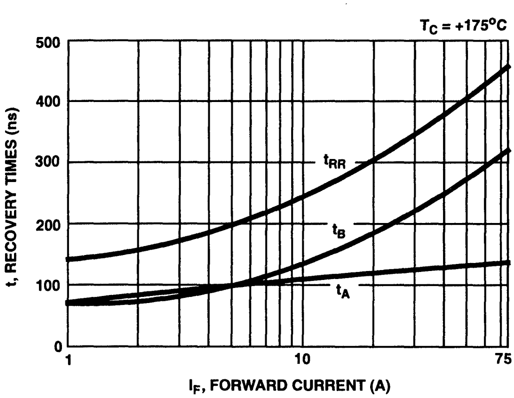


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

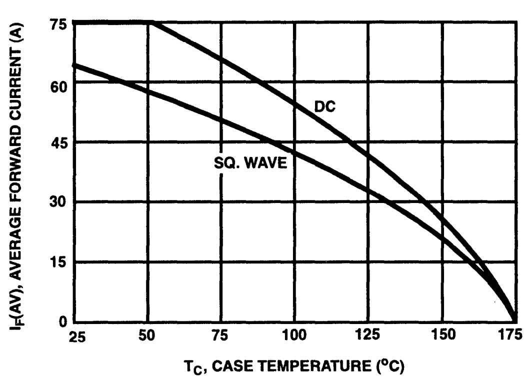


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

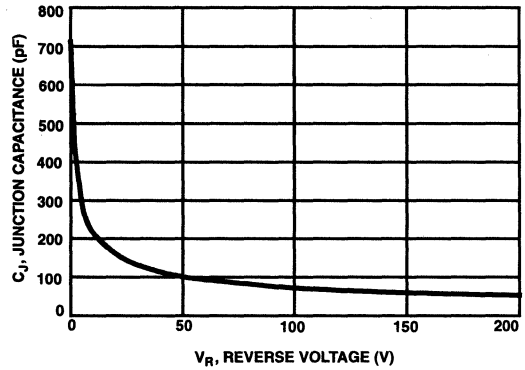


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

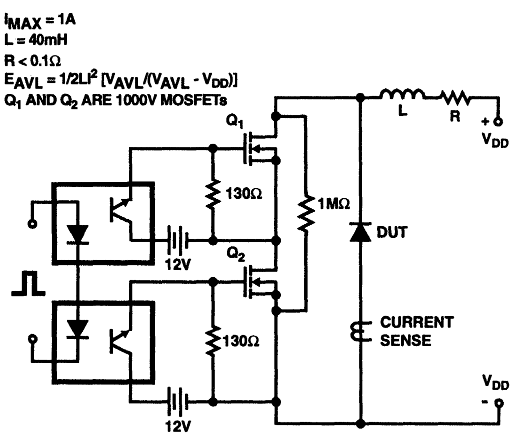


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

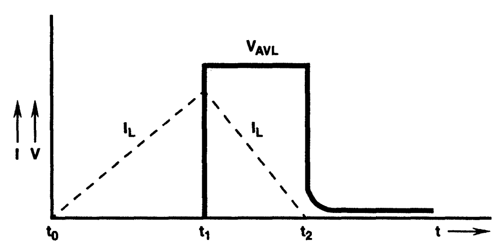


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

April 1995

75A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRG75120 (TA49042) is a hyperfast diode with soft recovery characteristics (t_{RR} < 85ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of high frequency switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery characteristic minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

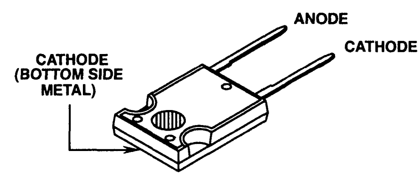
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG75120	TO-247	RHRG75120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol

Absolute Maximum Ratings T_C = +25°C

		RHRG75120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +41.3°C)	$I_{F(AV)}$	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	190	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS			UNITS
			MIN	TYP	MAX	
V_F	I_F = 75A		-	-	3.2	V
V_F	I_F = 75A	T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V		-	-	500	µA
I_R	V_R = 1200V	T_C = +150°C	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs		-	-	85	ns
t_{RR}	I_F = 75A, dI_F/dt = 100A/µs		-	-	100	ns
t_A	I_F = 75A, dI_F/dt = 100A/µs		-	60	-	ns
t_B	I_F = 75A, dI_F/dt = 100A/µs		-	25	-	ns
$R_{\theta JC}$			-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

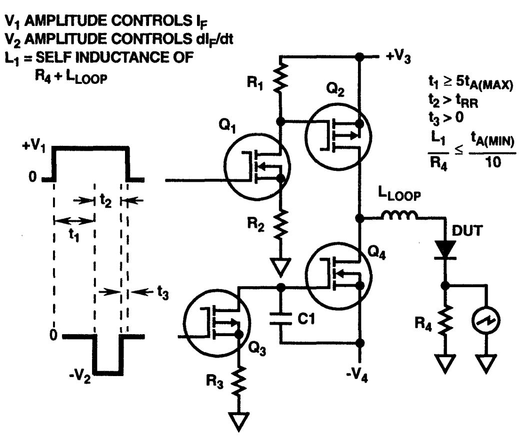


FIGURE 1. t_{RR} TEST CIRCUIT

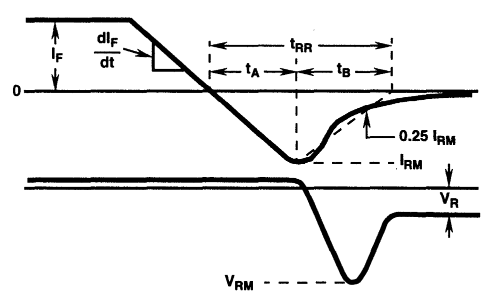


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

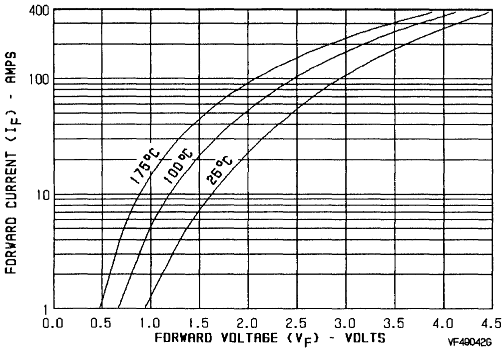


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

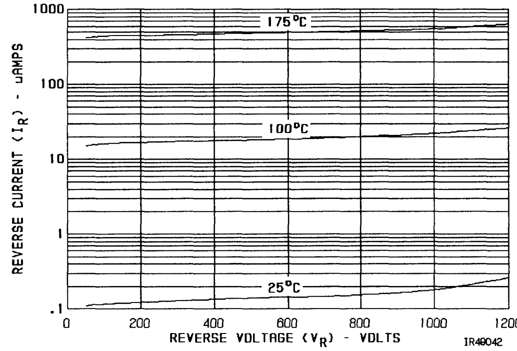


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

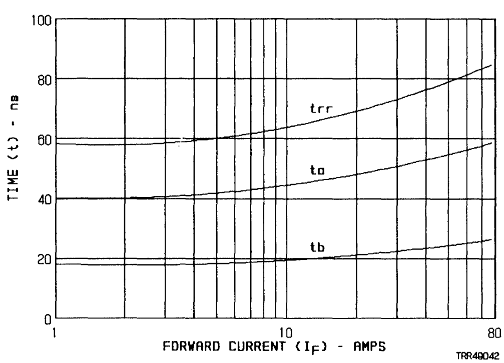


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

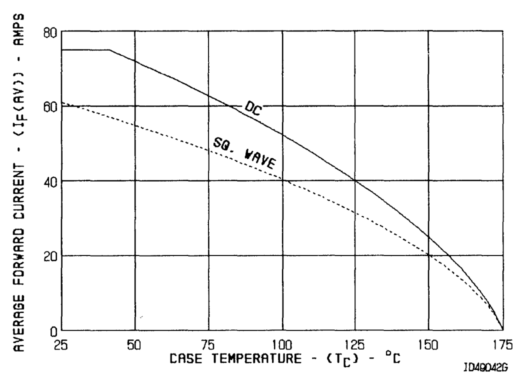


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

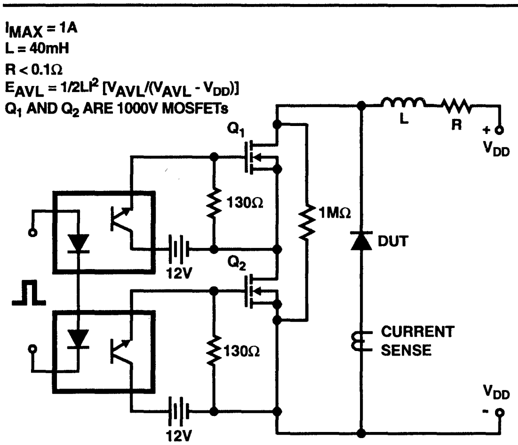


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

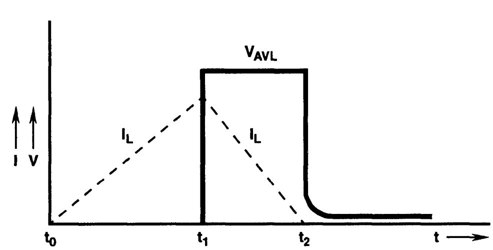


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP840, RHRP850, RHRP860

April 1995

8A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <30ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP840, RHRP850 and RHRP860 (TA49059) are hyperfast diodes with soft recovery characteristics (t_{RR} < 30ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

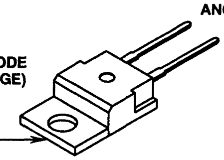
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP840	TO-220AC	RHRP840
RHRP850	TO-220AC	RHRP850
RHRP860	TO-220AC	RHRP860

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP840	RHRP850	RHRP860	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +150°C)	$I_{F(AV)}$	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	A
Maximum Power Dissipation	P_D	75	75	75	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRP840			RHRP850			RHRP860			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 8A, T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 8A, T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	μA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	μA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	μA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	μA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	μA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	μA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	30	-	-	30	-	-	30	ns
	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	-	35	-	-	35	-	-	35	ns
t_A	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	16	-	-	16	-	-	16	-	ns
t_B	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	11	-	-	11	-	-	11	-	ns
Q_{RR}	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	26	-	-	26	-	-	26	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	25	-	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	2	-	-	2	-	-	2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figure 10 and Figure 11).

pw = Pulse width.

D = Duty cycle.

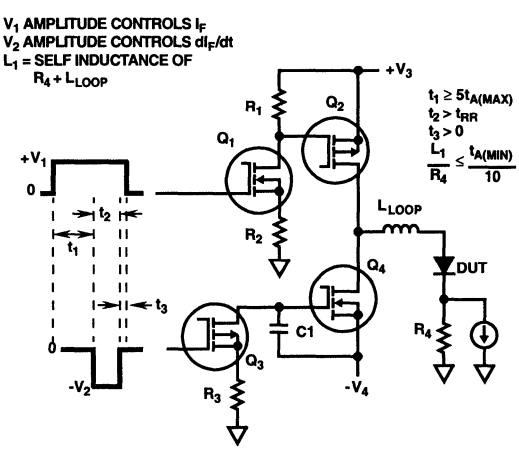


FIGURE 1. t_{RR} TEST CIRCUIT

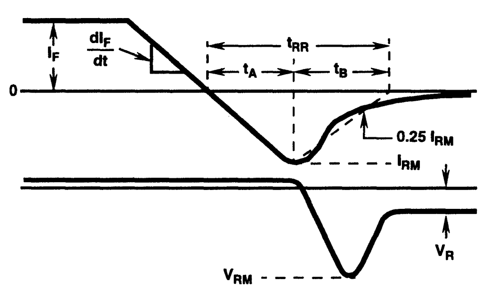


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

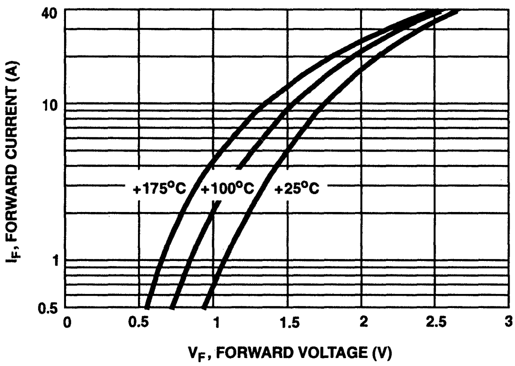


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

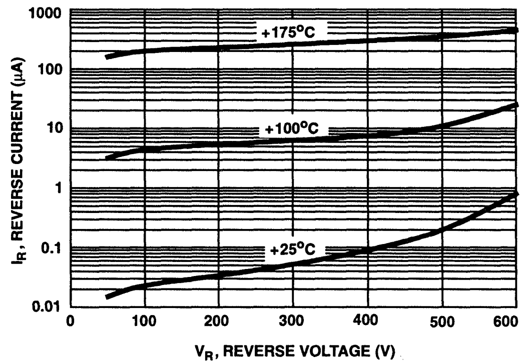


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

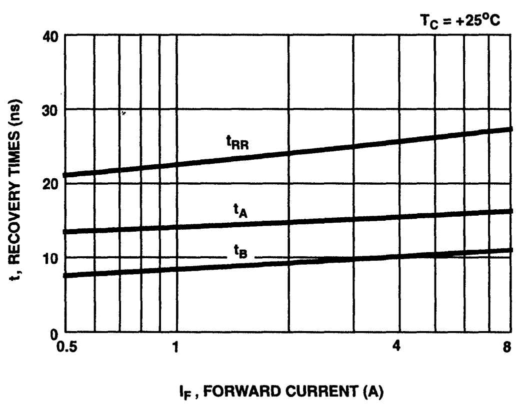


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

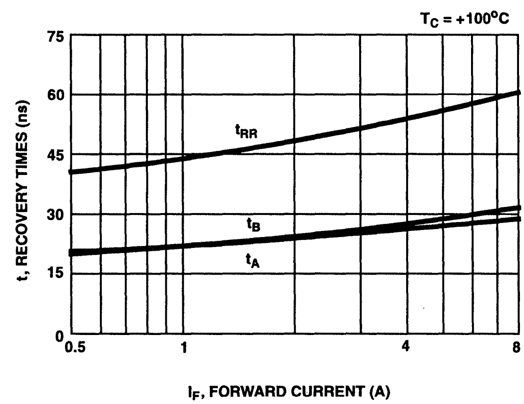


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

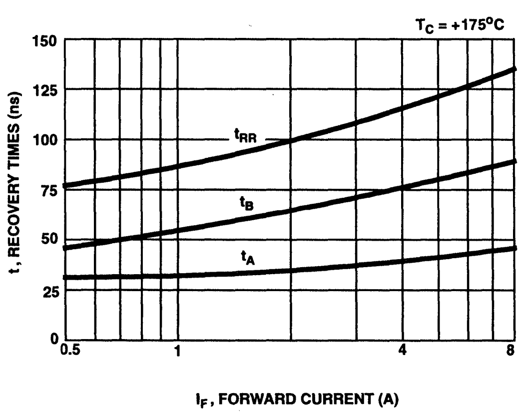


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

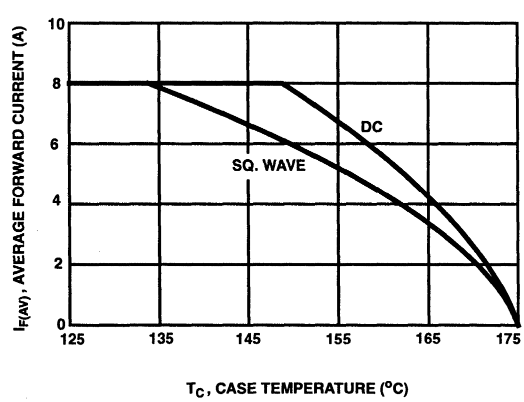


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

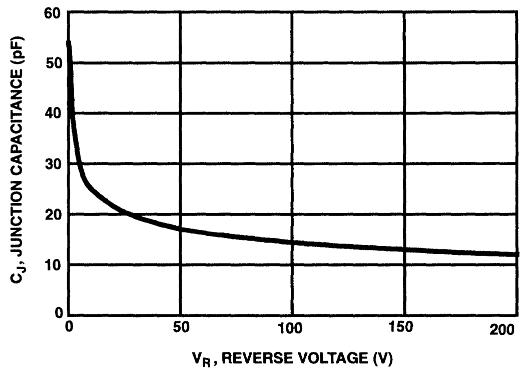


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$
Q1 AND Q2 ARE 1000V MOSFETS

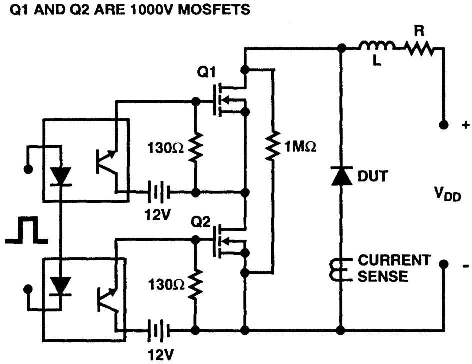


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

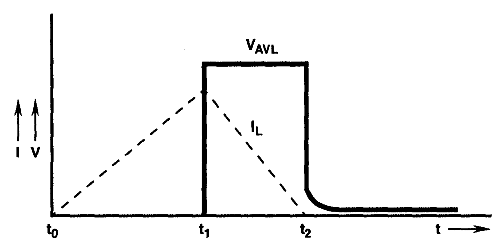


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP870, RHRP880, RHRP890, RHRP8100

April 1995

8A, 700V - 1000V Hyperfast Diodes

Features

- **Hyperfast with Soft Recovery . . . . <60ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage Up To 1000V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRP870, RHRP880, RHRP890 and RHRP8100 (TA49060) are hyperfast diodes with soft recovery characteristics (t_{RR} < 60ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

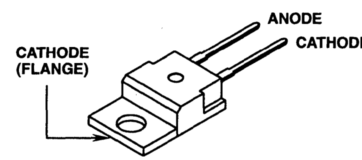
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP870	TO-220AC	RHRP870
RHRP880	TO-220AC	RHRP880
RHRP890	TO-220AC	RHRP890
RHRP8100	TO-220AC	RHRP8100

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP870	RHRP880	RHRP890	RHRP8100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	8	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	100	A
Maximum Power Dissipation	P_D	75	75	75	75	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3667.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRP870			RHRP880			RHRP890			RHRP8100			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 8A, T_C = +25^oC$	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	$I_F = 8A, T_C = +150^oC$	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	$V_R = 700V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	-	-	-	μA
	$V_R = 1000V, T_C = +25^oC$	-	-	-	-	-	-	-	-	-	-	-	100	μA
I_R	$V_R = 700V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	-	-	-	μA
	$V_R = 1000V, T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	500	μA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	60	-	-	60	-	-	60	-	-	60	ns
	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	-	65	-	-	65	-	-	65	-	-	65	ns
t_A	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	38	-	-	38	-	-	38	-	-	38	-	ns
t_B	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	21	-	-	21	-	-	21	-	-	21	-	ns
Q_{RR}	$I_F = 8A, dI_F/dt = 100A/\mu s$	-	130	-	-	130	-	-	130	-	-	130	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	30	-	-	30	-	-	30	-	-	30	-	pF
$R_{\theta JC}$		-	-	2.0	-	-	2.0	-	-	2.0	-	-	2.0	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figure 10 and Figure 11).

pw = pulse width.

D = duty cycle.

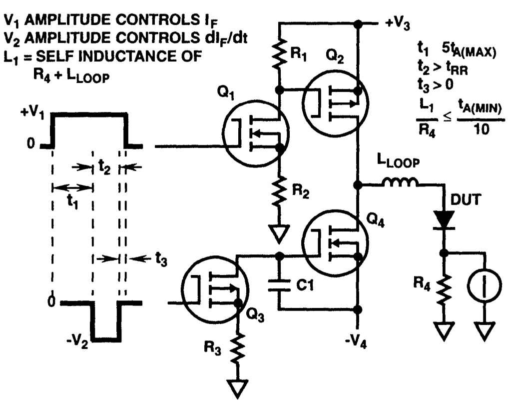


FIGURE 1. t_{RR} TEST CIRCUIT

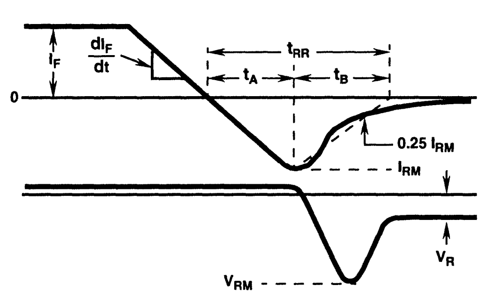


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

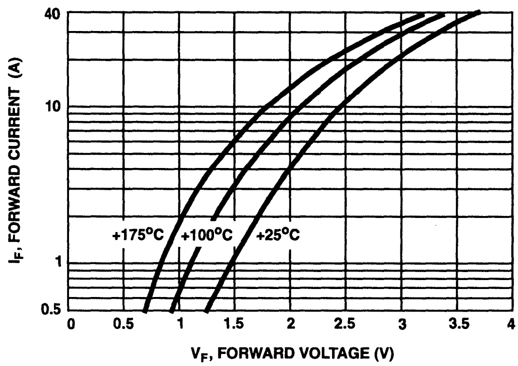


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

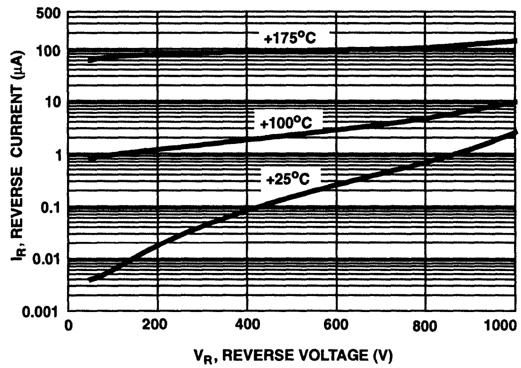


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

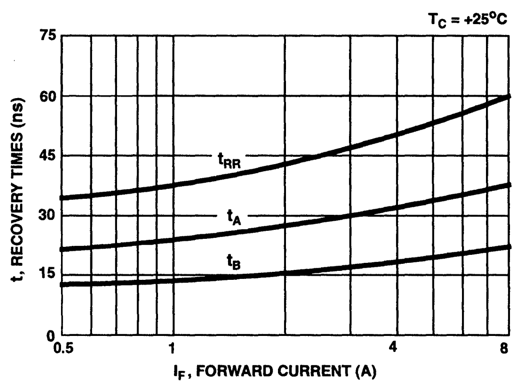


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

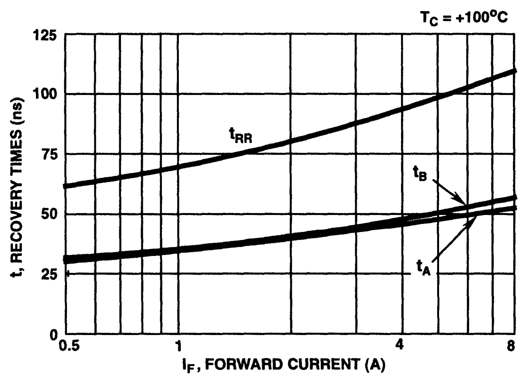


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

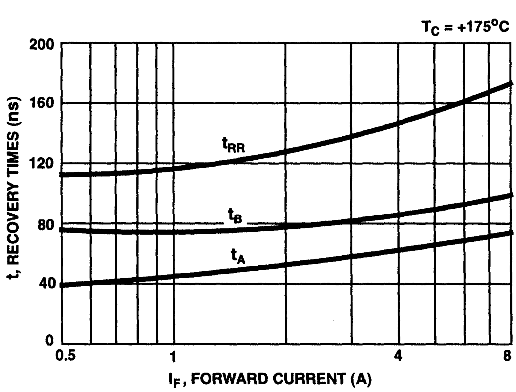


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

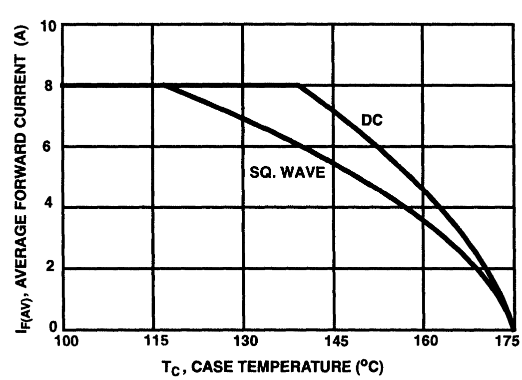


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

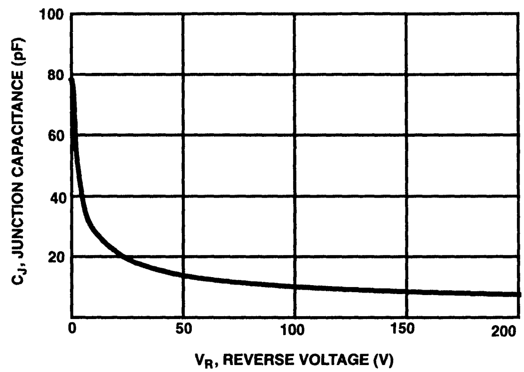


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2[V_{AVL}/(V_{AVL} - V_{DD})]$
Q1 AND Q2 ARE 1000V MOSFETS

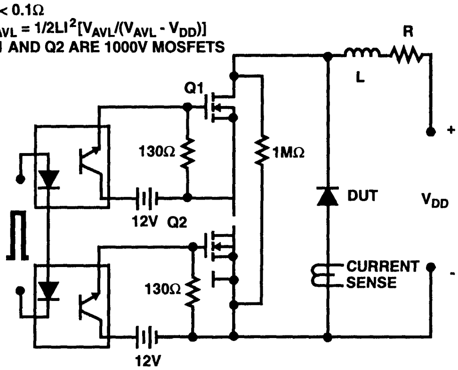


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

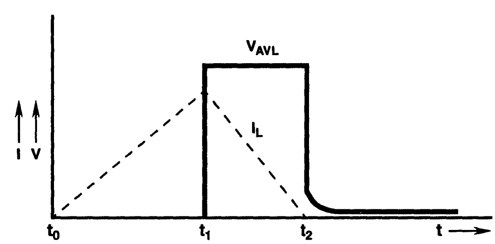


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP8120

April 1995

8A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery .... <55ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRP8120 (TA49096) are hyperfast diodes with soft recovery characteristics (t_{RR} < 55ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

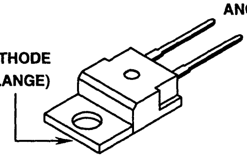
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP8120	TO-220AC	RHRP8120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP8120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +126°C)	$I_{F(AV)}$	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	A
Maximum Power Dissipation	P_D	75	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3660.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
V_F	I_F = 8A, T_C = +25°C	-	-	3.2	V
	I_F = 8A, T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	µA
	V_R = 1200V, T_C = +150°C	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	55	ns
	I_F = 8A, dI_F/dt = 100A/µs	-	-	70	ns
t_A	I_F = 8A, dI_F/dt = 100A/µs	-	34	-	ns
t_B	I_F = 8A, dI_F/dt = 100A/µs	-	30	-	ns
Q_{RR}	I_F = 8A, dI_F/dt = 100A/µs	-	130	-	nC
C_J	V_R = 10V, I_F = 0A	-	25	-	pF
$R_{\theta JC}$		-	-	2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

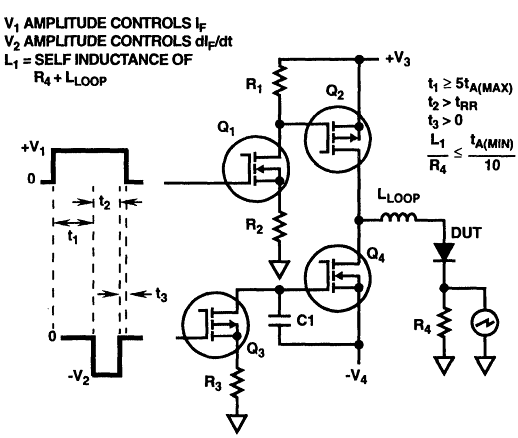


FIGURE 1. t_{RR} TEST CIRCUIT

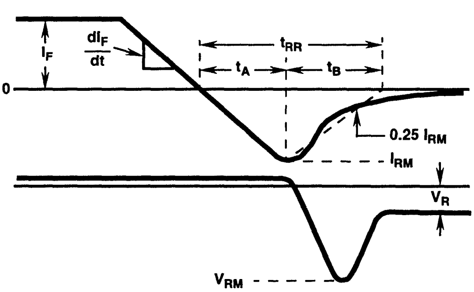


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

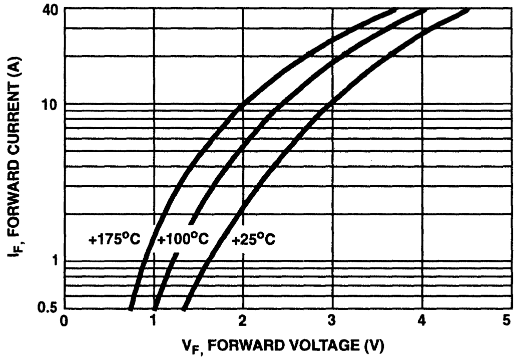


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

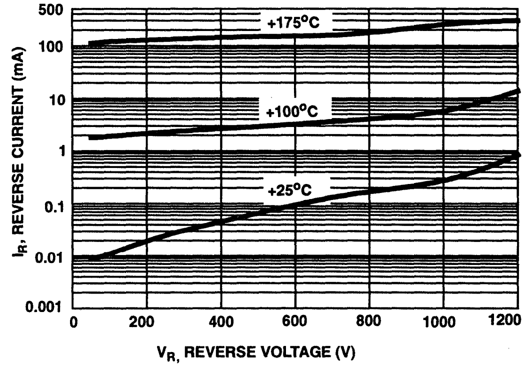


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

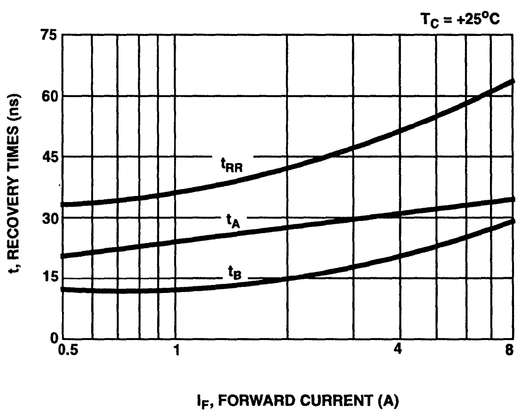


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

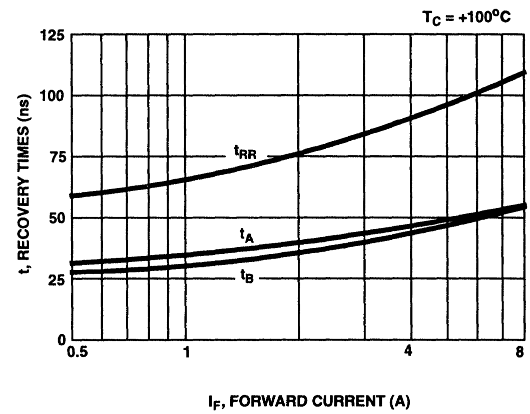


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

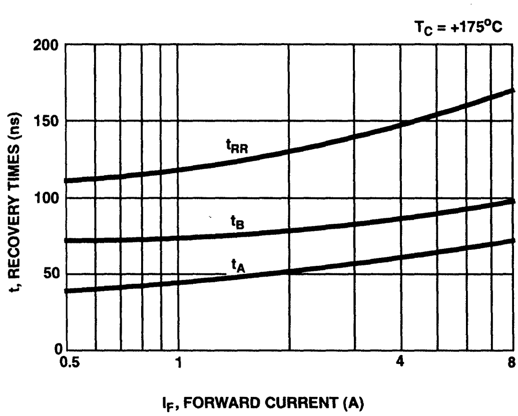


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

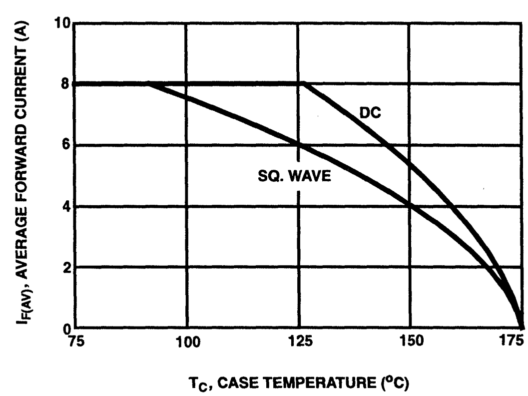


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

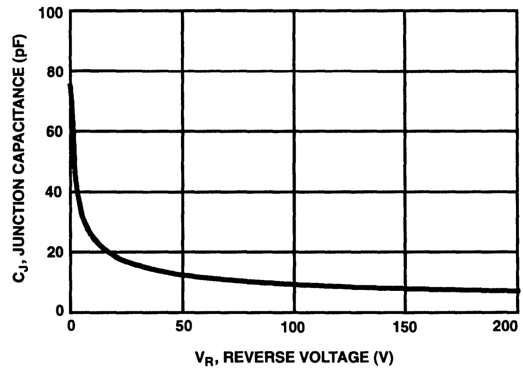


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

$I_{MAX} = 1A$
$L = 40mH$
$R < 0.1\Omega$
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 AND Q_2 ARE 1000V MOSFETs

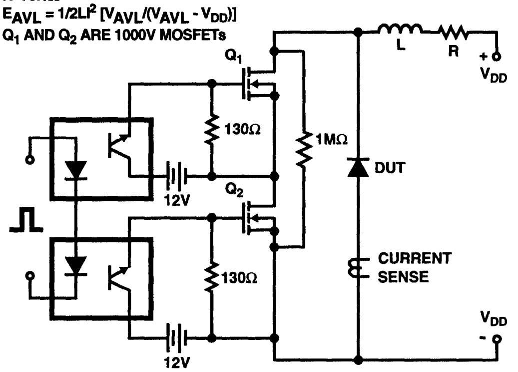


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

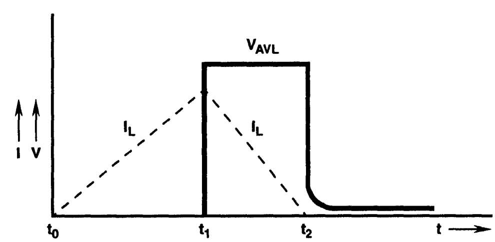


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

7

HYPERFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

RHRP1540, RHRP1550, RHRP1560

April 1995

15A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <35ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP1540, RHRP1550 and RHRP1560 (TA49061) are hyperfast diodes with soft recovery characteristics (t_{RR} < 35ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

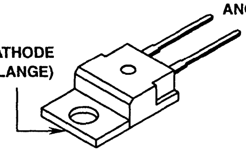
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP1540	TO-220AC	RHRP1540
RHRP1550	TO-220AC	RHRP1550
RHRP1560	TO-220AC	RHRP1560

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP1540	RHRP1550	RHRP1560	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	15	15	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	30	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	200	200	A
Maximum Power Dissipation	P_D	100	100	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number 3685.1

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		LIMITS									
		RHRP1540			RHRP1550			RHRP1560			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 15A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
	I_F = 15A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	100	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	100	-	-	-	μA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 400V, T_C = +150°C	-	-	500	-	-	-	-	-	-	μA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	35	-	-	35	-	-	35	ns
	I_F = 15A, dI_F/dt = 100A/μs	-	-	40	-	-	40	-	-	40	ns
t_A	I_F = 15A, dI_F/dt = 100A/μs	-	20	-	-	20	-	-	20	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/μs	-	15	-	-	15	-	-	15	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/μs	-	40	-	-	40	-	-	40	-	nC
C_J	V_R = 10V, I_F = 0A	-	60	-	-	60	-	-	60	-	pF
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current .

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

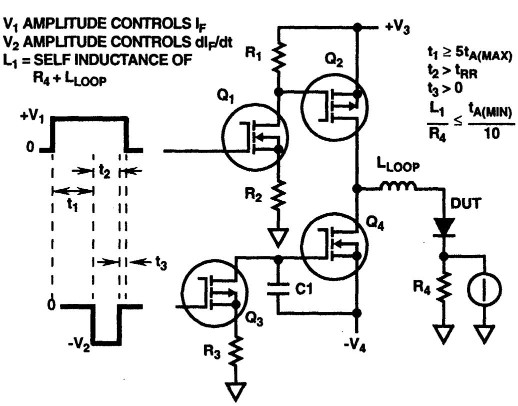


FIGURE 1. t_{RR} TEST CIRCUIT

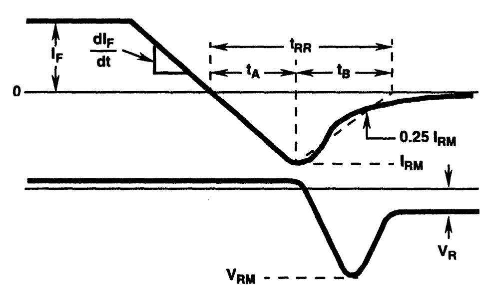


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

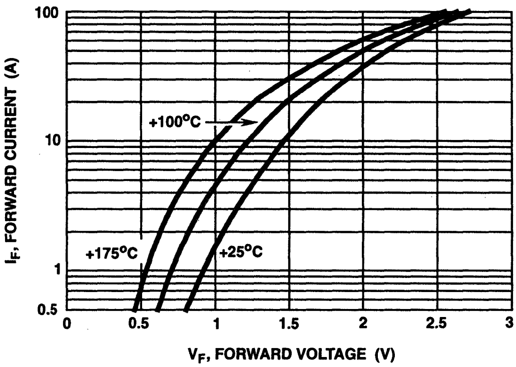


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

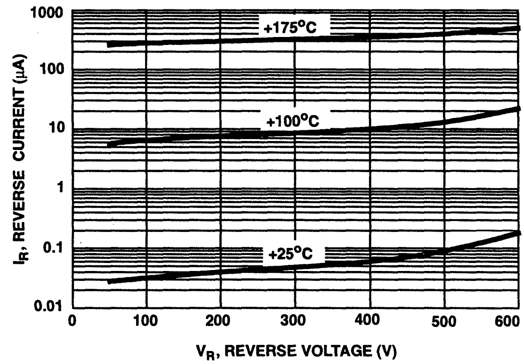


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

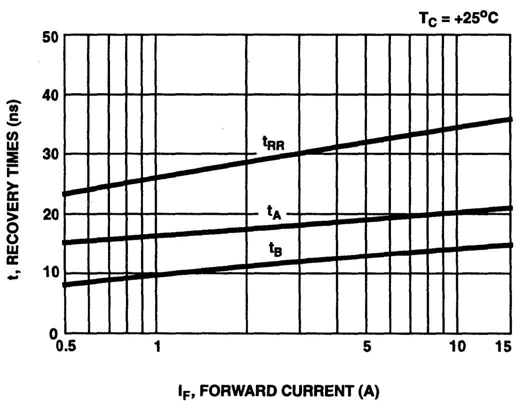


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

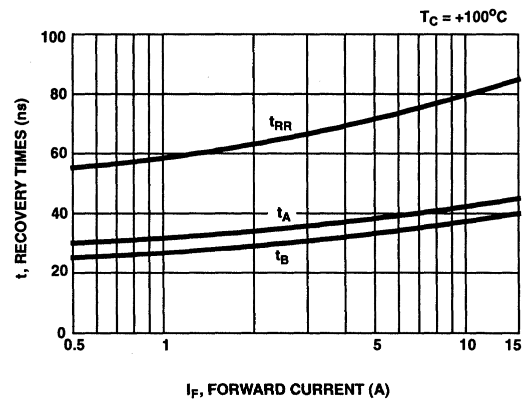


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

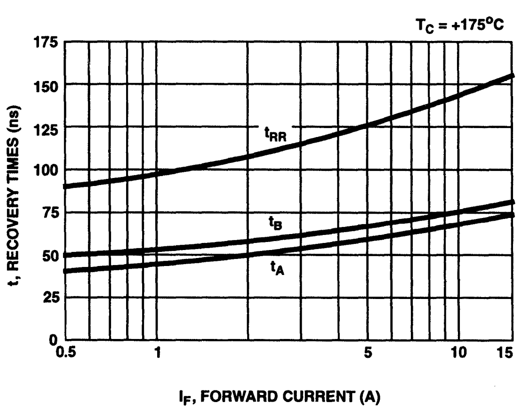


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

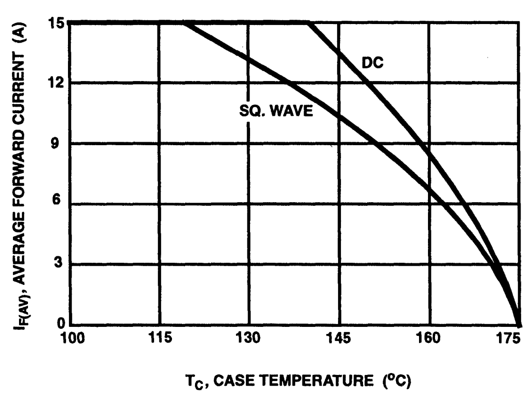


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

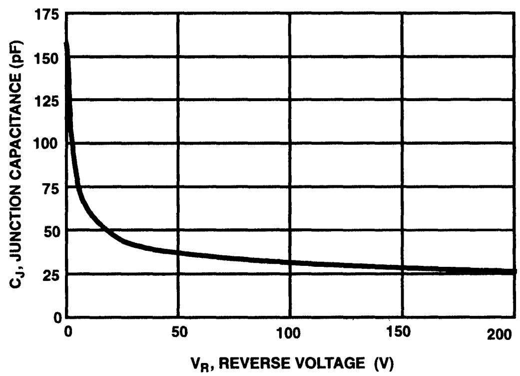


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

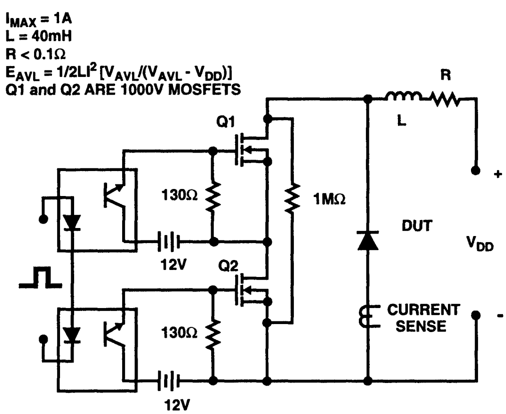


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

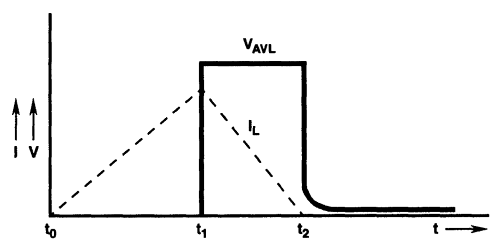


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRP1570, RHRP1580, RHRP1590, RHRP15100

April 1995

15A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <60ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP1570, RHRP1580, RHRP1590 and RHRP15100 (TA49062) are hyperfast diodes with soft recovery characteristics (t_{RR} < 60ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

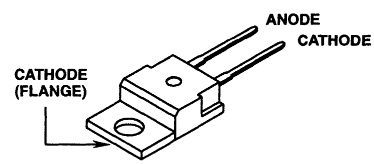
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP1570	TO-220AC	RHRP1570
RHRP1580	TO-220AC	RHRP1580
RHRP1590	TO-220AC	RHRP1590
RHRP15100	TO-220AC	RHR15100

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP1570	RHRP1580	RHRP1590	RHRP15100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +130°C)	$I_{F(AV)}$	15	15	15	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	30	30	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	200	200	200	A
Maximum Power Dissipation	P_D	100	100	100	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3692.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRP1570			RHRP1580			RHRP1590			RHRP15100			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 15A, T_C = +25^oC$	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	$I_F = 15A, T_C = +150^oC$	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	$V_R = 700V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	-	-	-	μA
	$V_R = 1000V, T_C = +25^oC$	-	-	-	-	-	-	-	-	-	-	-	100	μA
I_R	$V_R = 700V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	-	-	-	μA
	$V_R = 1000V, T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	500	μA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	60	-	-	60	-	-	60	-	-	60	ns
	$I_F = 15A$, $dI_F/dt = 100A/\mu s$	-	-	70	-	-	70	-	-	70	-	-	70	ns
t_A	$I_F = 15A$, $dI_F/dt = 100A/\mu s$	-	40	-	-	40	-	-	40	-	-	40	-	ns
t_B	$I_F = 15A$, $dI_F/dt = 100A/\mu s$	-	25	-	-	25	-	-	25	-	-	25	-	ns
Q_{RR}	$I_F = 15A$, $dI_F/dt = 100A/\mu s$	-	160	-	-	160	-	-	160	-	-	160	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	66	-	-	66	-	-	66	-	-	66	-	pF
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

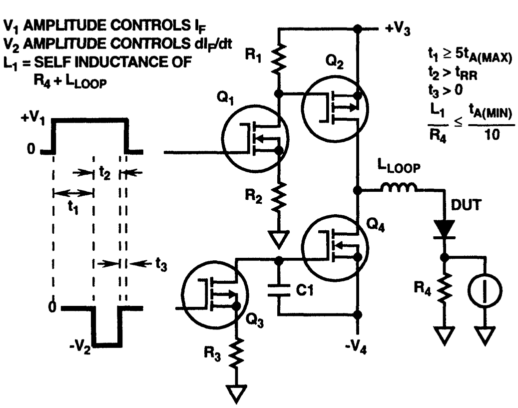


FIGURE 1. t_{RR} TEST CIRCUIT

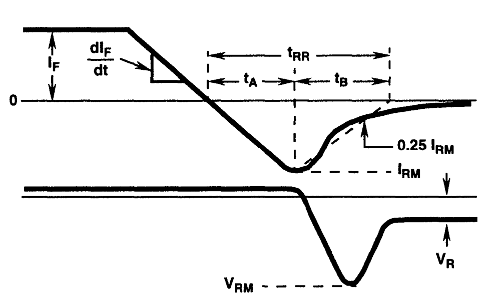


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

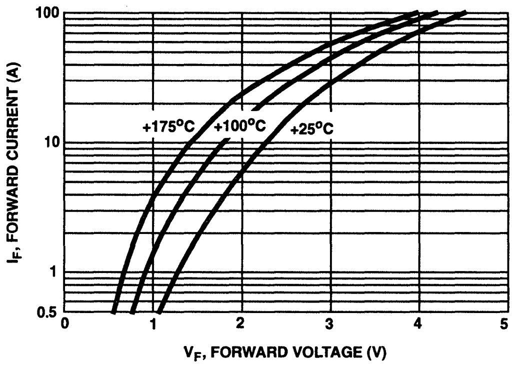


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

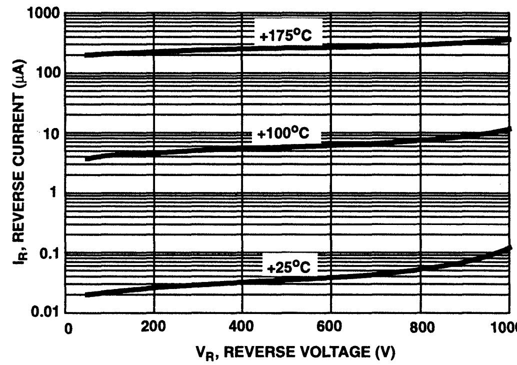


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

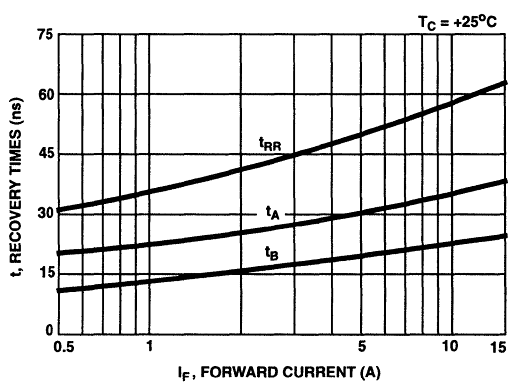


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

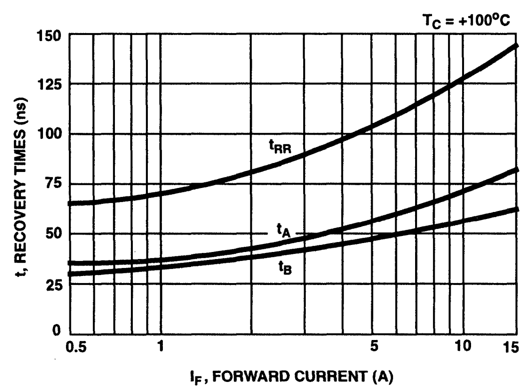


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

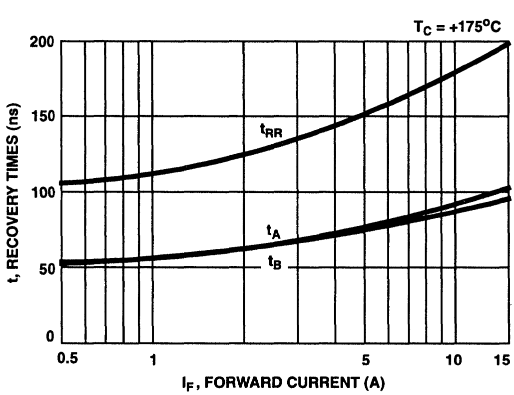


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

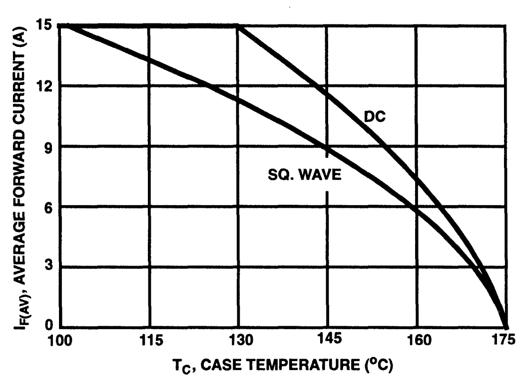


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

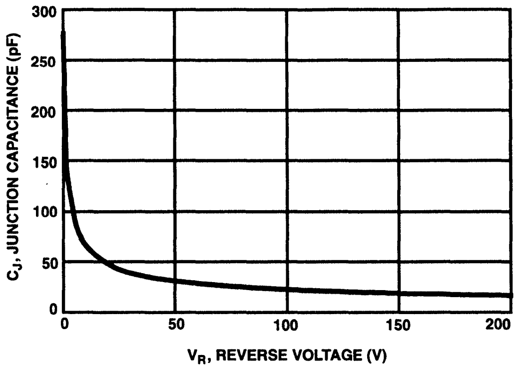


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

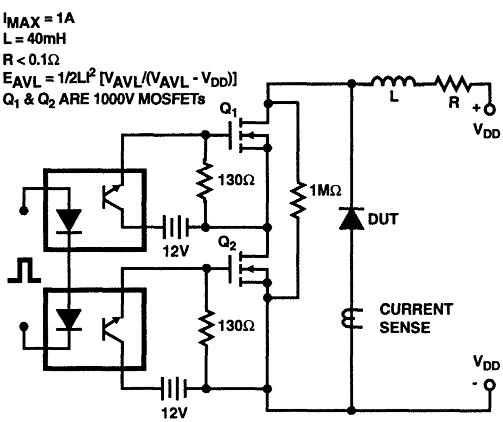


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

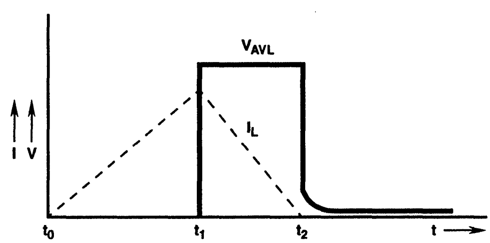


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP15120

April 1995

15A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery .... <65ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRP15120 (TA49098) are hyperfast diodes with soft recovery characteristics (t_{RR} < 65ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

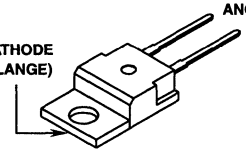
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP15120	TO-220AC	RHR15120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP15120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 130°C)	$I_{F(AV)}$	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	A
Maximum Power Dissipation	P_D	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Characteristics $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRP15120 LIMITS			UNITS
		MIN	TYP	MAX	
V_F	I_F = 15A, $T_C = +25^oC$	-	-	3.2	V
	I_F = 15A, $T_C = +150^oC$	-	-	2.6	V
I_R	V_R = 1200V, $T_C = +25^oC$	-	-	100	µA
	V_R = 1200V, $T_C = +150^oC$	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	65	ns
	I_F = 15A, dI_F/dt = 100A/µs	-	-	75	ns
t_A	I_F = 15A, dI_F/dt = 100A/µs	-	36	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/µs	-	28	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/µs	-	150	-	nC
C_J	V_R = 10V, I_F = 0A	-	55	-	pF
$R_{\theta JC}$		-	-	1.5	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

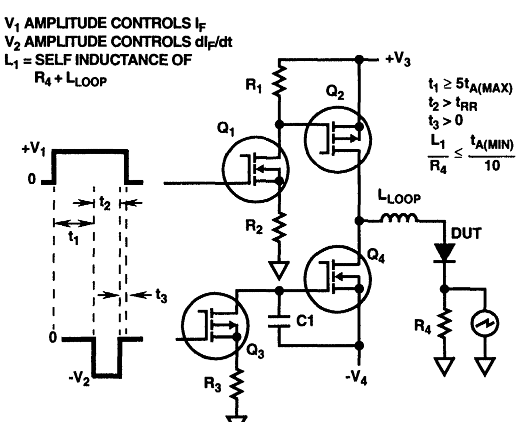


FIGURE 1. t_{RR} TEST CIRCUIT

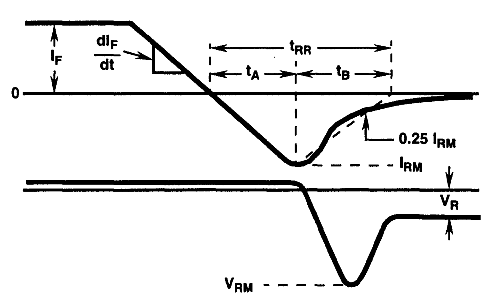


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

7
HYPERFAST SINGLE DIODES

Typical Performance Curves

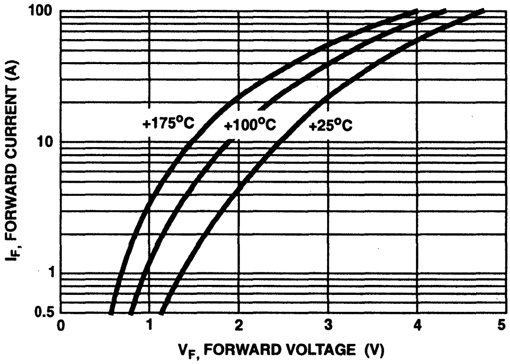


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

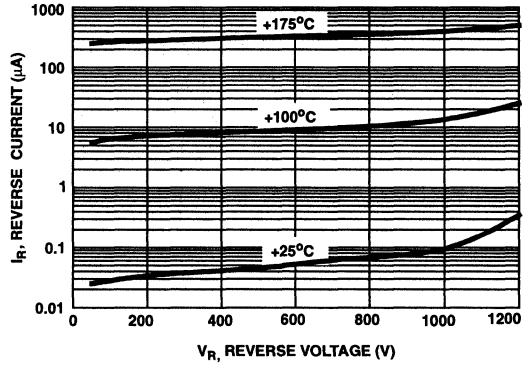


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

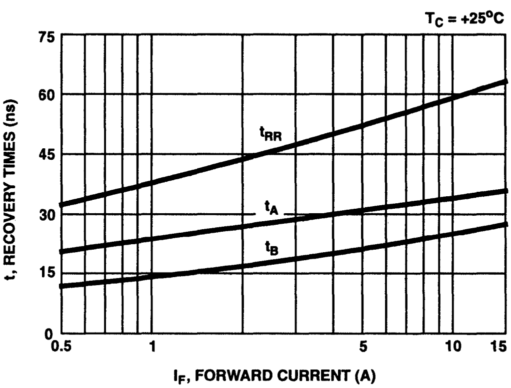


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

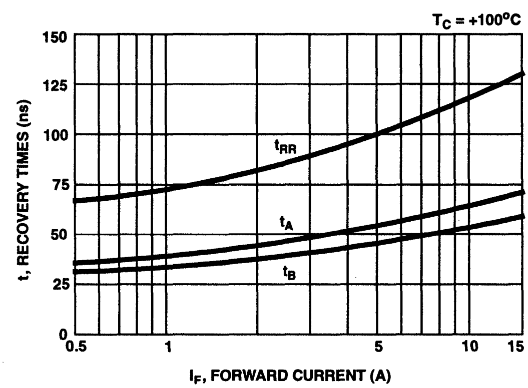


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

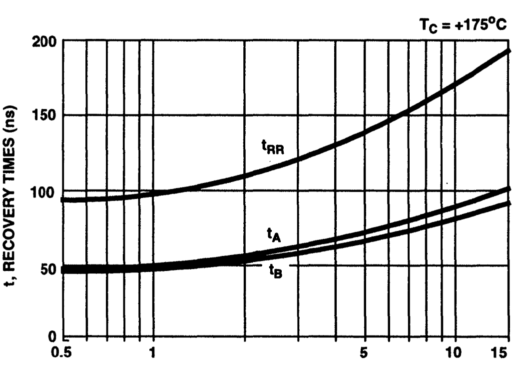


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

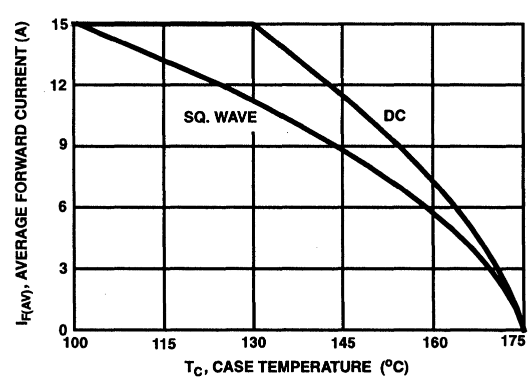


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

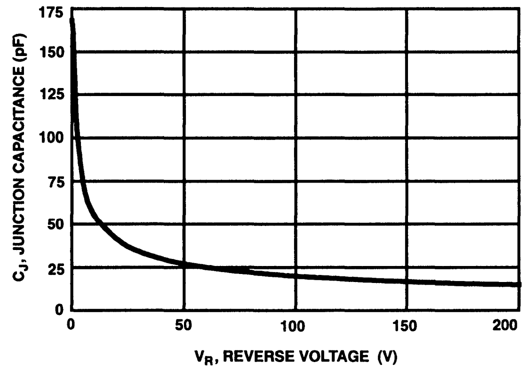


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

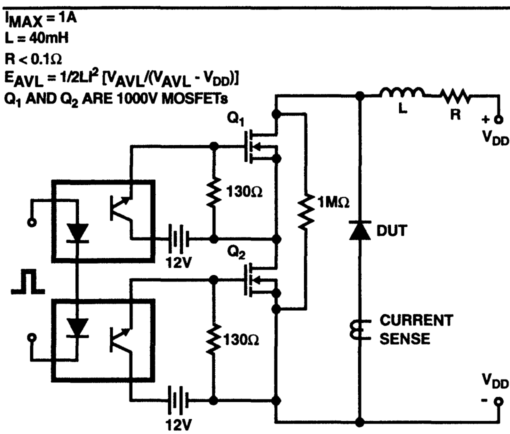


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

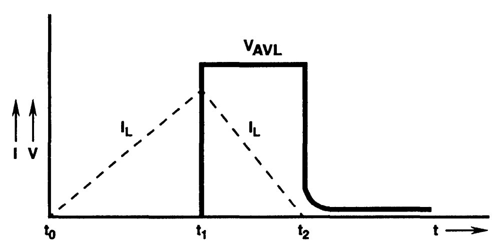


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP3040, RHRP3050, RHRP3060

April 1995

30A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery .... <40ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP3040, RHRP3050 and RHRP3060 (TA49063) are hyperfast diodes with soft recovery characteristics (t_{RR} < 40ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/ clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

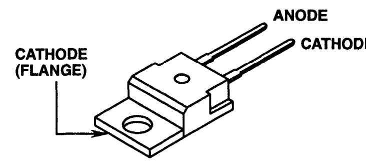
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP3040	TO-220AC	RHRP3040
RHRP3050	TO-220AC	RHRP3050
RHRP3060	TO-220AC	RHRP3060

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP3040	RHRP3050	RHRP3060	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +120°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		RHRP3040			RHRP3050			RHRP3060			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 30A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
	I_F = 30A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = +150°C	-	-	1.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	1.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	40	-	-	40	-	-	40	ns
	I_F = 30A, dI_F/dt = 100A/µs	-	-	45	-	-	45	-	-	45	ns
t_A	I_F = 30A, dI_F/dt = 100A/µs	-	22	-	-	22	-	-	22	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs	-	20	-	-	20	-	-	20	-	ns
Q_{RR}	I_F = 30A, dI_F/dt = 100A/µs	-	50	-	-	50	-	-	50	-	nC
C_J	V_R = 10V, I_F = 0A	-	85	-	-	85	-	-	85	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current .
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

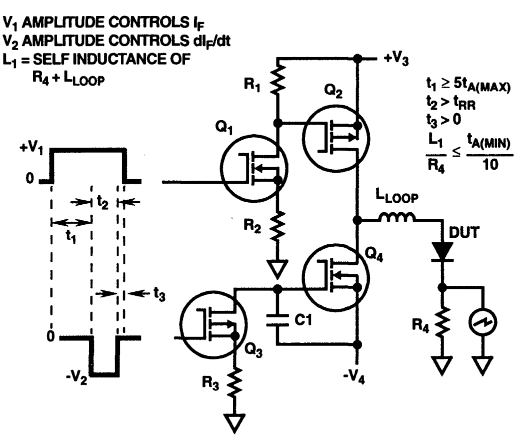


FIGURE 1. t_{RR} TEST CIRCUIT

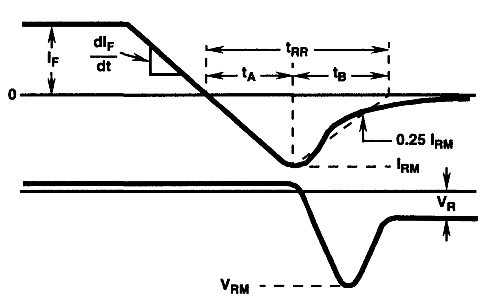


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

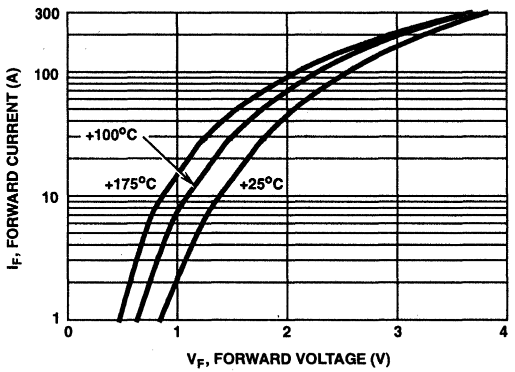


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

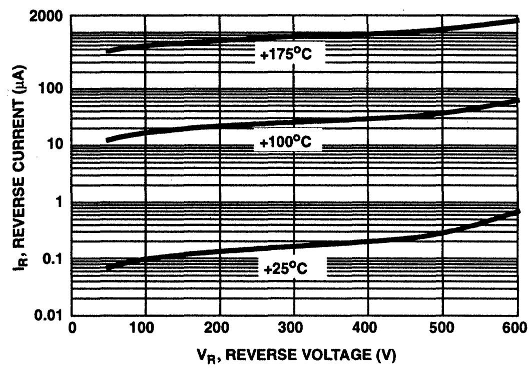


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

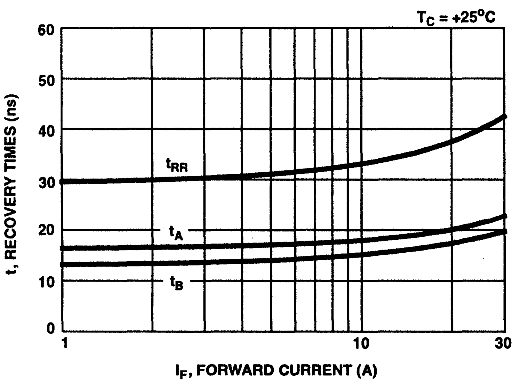


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

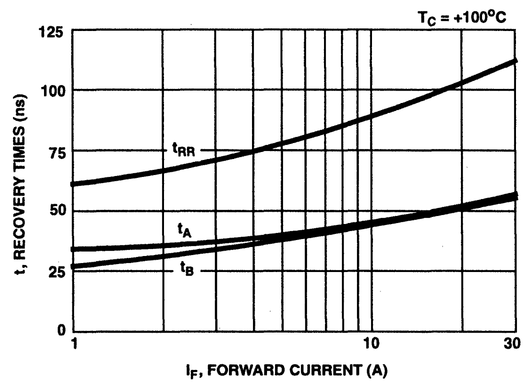


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

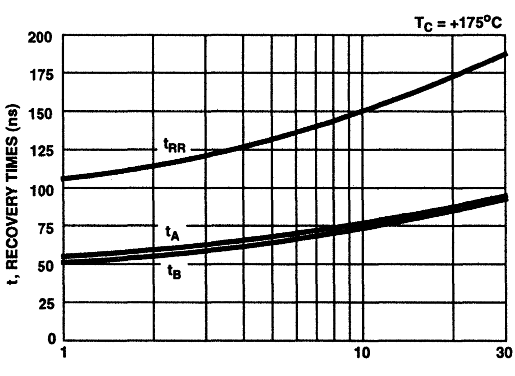


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

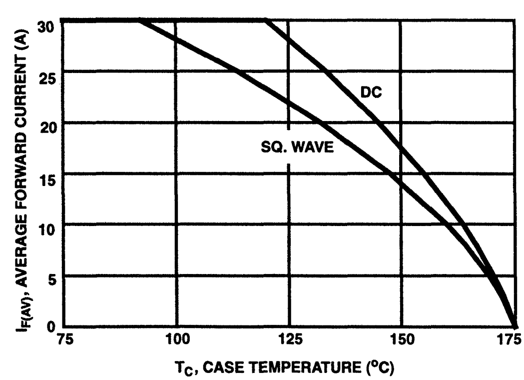


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

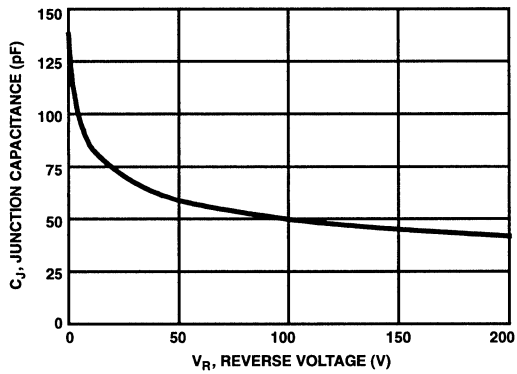


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

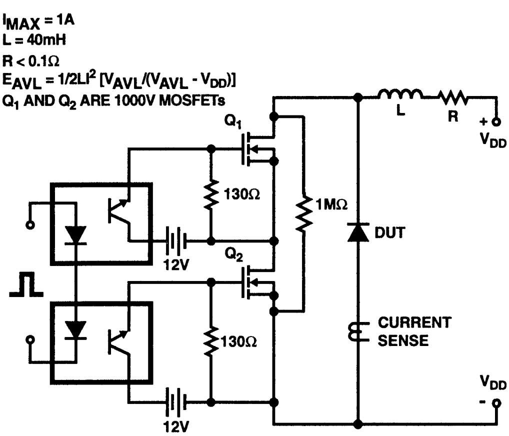


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

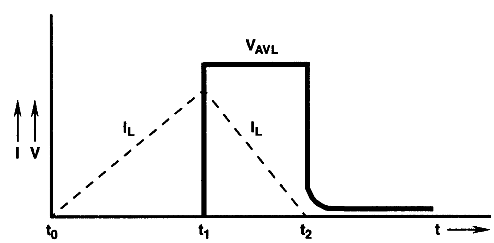


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRP3070, RHRP3080, RHRP3090, RHRP30100

HARRIS SEMICONDUCTOR

April 1995

30A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery .... <65ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP3070, RHRP3080, RHRP3090 and RHRP30100 (TA49064) are hyperfast diodes with soft recovery characteristics (t_{RR} < 65ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

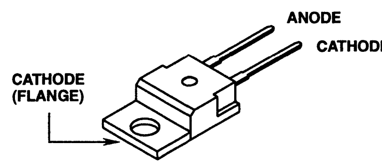
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP3070	TO-220AC	RHRP3070
RHRP3080	TO-220AC	RHRP3080
RHRP3090	TO-220AC	RHRP3090
RHRP30100	TO-220AC	RHR30100

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRP3070	RHRP3080	RHRP3090	RHRP30100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +95°C)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

		RHRP3070			RHRP3080			RHRP3090			RHRP30100			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	I_F = 30A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 30A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V, T_C = +25°C							-	-	500				µA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 700V, T_C = +150°C	-	-	1.0	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	1.0	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C							-	-	1.0				mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	65	-	-	65	-	-	65	-	-	65	ns
	I_F = 30A, dI_F/dt = 100A/µs	-	-	75	-	-	75	-	-	75	-	-	75	ns
t_A	I_F = 30A, dI_F/dt = 100A/µs	-	35	-	-	35	-	-	35	-	-	35	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs	-	33	-	-	33	-	-	33	-	-	33	-	ns
Q_{RR}	I_F = 30A, dI_F/dt = 100A/µs	-	200	-	-	200	-	-	200	-	-	200	-	nC
C_J	V_R = 10V, I_F = 0A	-	100	-	-	100	-	-	100	-	-	100	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2			1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

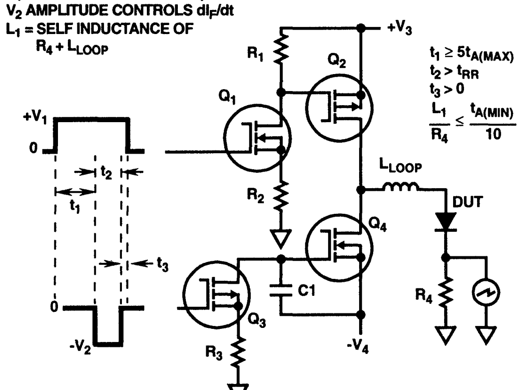


FIGURE 1. t_{RR} TEST CIRCUIT

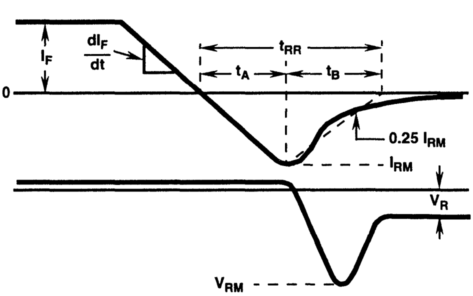


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

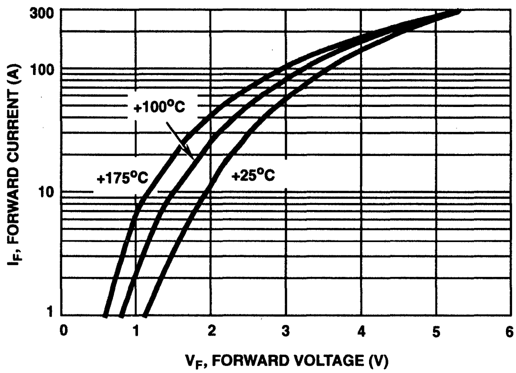


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

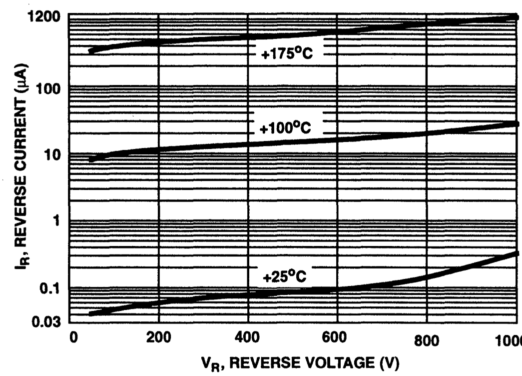


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

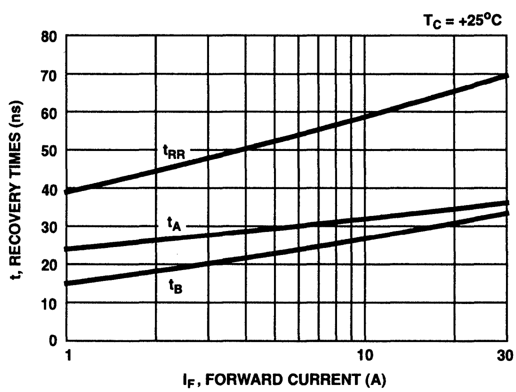


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

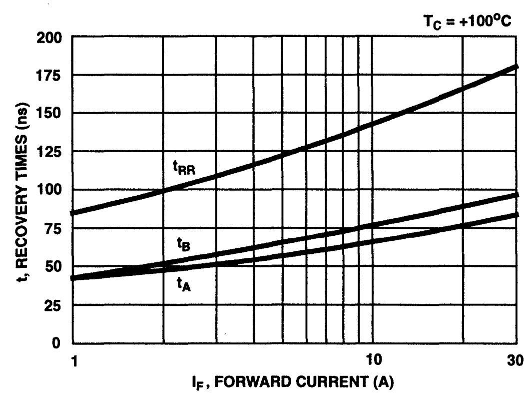


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

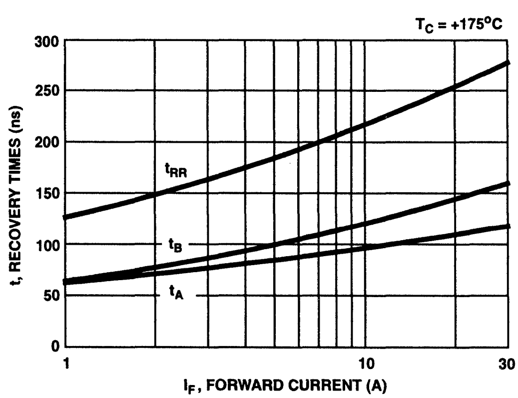


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

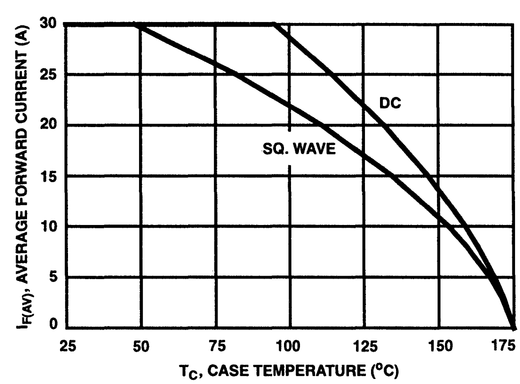


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

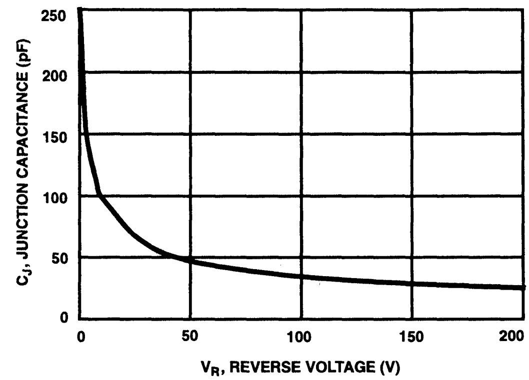


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

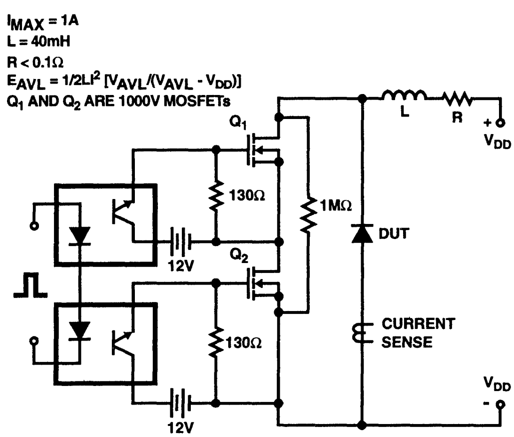


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

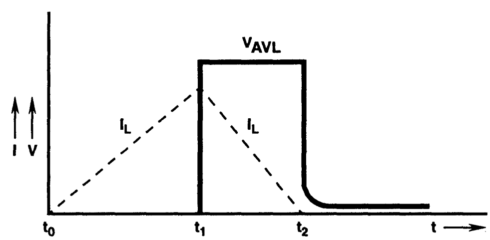


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS
SEMICONDUCTOR

RHRP30120

April 1995

30A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <65ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRP30120 (TA49041) is a hyperfast diode with soft recovery characteristics (t_{RR} < 65ns).It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of high frequency switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

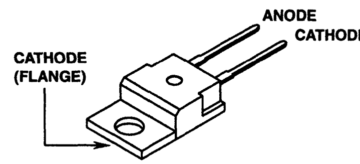
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP30120	TO-220AC	RHR30120

NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AC



Symbol

Absolute Maximum Ratings T_C = +25°C

		RHRP30120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +78°C)	$I_{F(AV)}$	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	60	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	A
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3409.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 30A		-	-	3.2	V
V_F	I_F = 30A	T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V		-	-	500	µA
I_R	V_R = 1200V	T_C = +150°C	-	-	1	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs		-	-	65	ns
t_{RR}	I_F = 30A, dI_F/dt = 100A/µs		-	-	75	ns
t_A	I_F = 30A, dI_F/dt = 100A/µs		-	48	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/µs		-	22	-	ns
$R_{\theta JC}$			-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

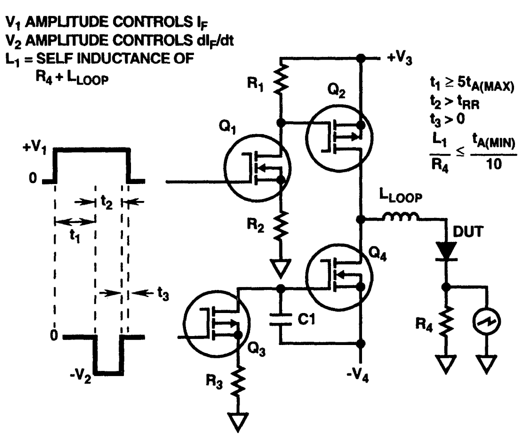


FIGURE 1. t_{RR} TEST CIRCUIT

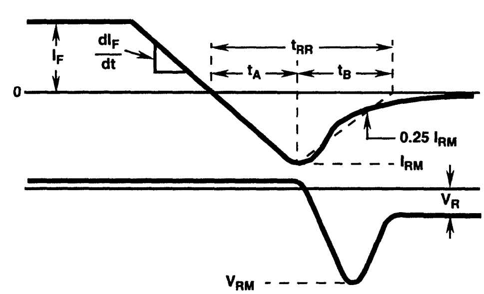


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

7 HYPERFAST SINGLE DIODES

Typical Performance Curves

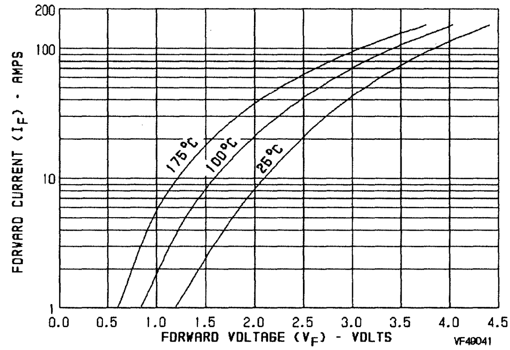


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

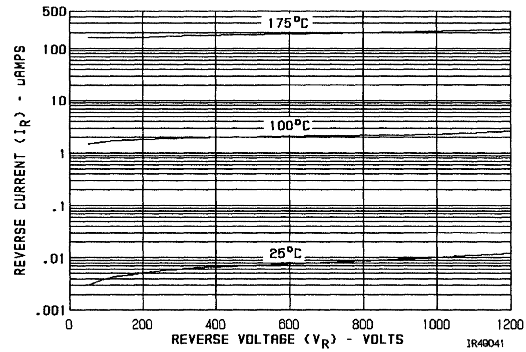


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

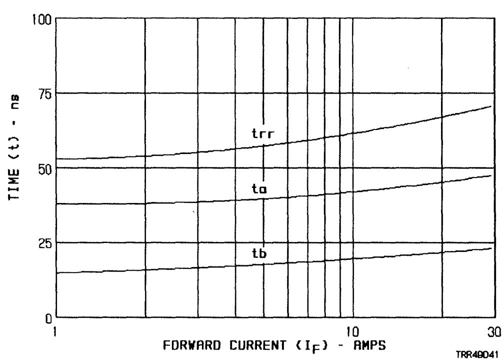


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

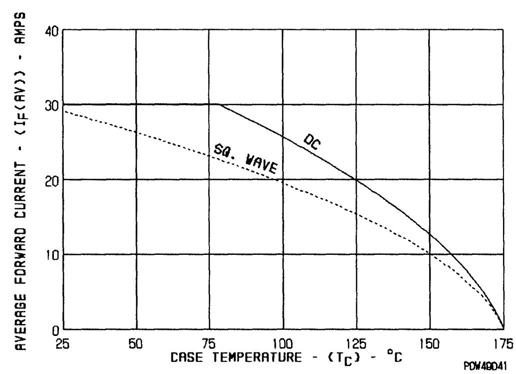


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPE

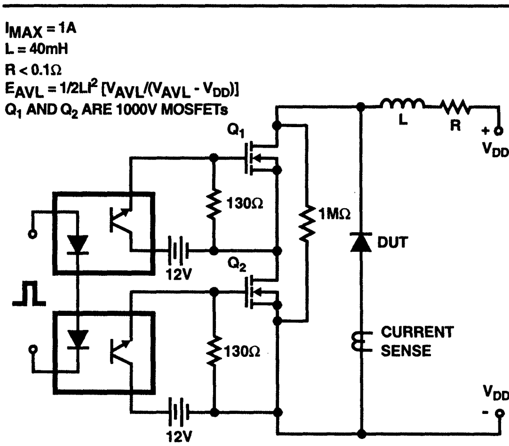


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

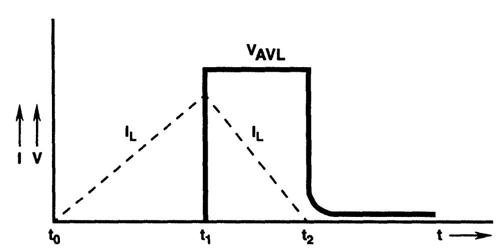


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU5040, RHRU5050, RHRU5060

April 1995

50A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <45ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU5040, RHRU5050 and RHRU5060 (TA49065) are hyperfast diodes with soft recovery characteristics (t_{RR} < 45ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

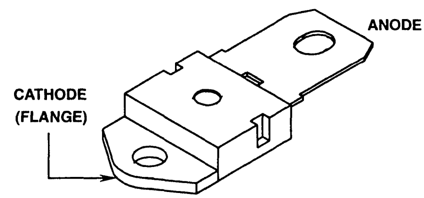
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU5040	TO-218	RHRU5040
RHRU5050	TO-218	RHRU5050
RHRU5060	TO-218	RHRU5060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

	RHRU5040	RHRU5050	RHRU5060	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	400	500	600	V
Working Peak Reverse Voltage . . . . V_{RWM}	400	500	600	V
DC Blocking Voltage . . . . V_R	400	500	600	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ (T_C = +93°C)	50	50	50	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	100	100	100	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	500	500	500	A
Maximum Power Dissipation . . . . P_D	150	150	150	W
Avalanche Energy (L = 40mH) . . . . E_{AVL}	40	40	40	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU5040			RHRU5050			RHRU5060			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 50A$, $T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 50A$, $T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V$, $T_C = +25^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V$, $T_C = +25^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V$, $T_C = +25^oC$	-	-	-	-	-	-	-	-	500	µA
I_R	$V_R = 400V$, $T_C = +150^oC$	-	-	1.5	-	-	-	-	-	-	mA
	$V_R = 500V$, $T_C = +150^oC$	-	-	-	-	-	1.5	-	-	-	mA
	$V_R = 600V$, $T_C = +150^oC$	-	-	-	-	-	-	-	-	1.5	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	45	-	-	45	-	-	45	ns
	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	-	50	-	-	50	-	-	50	ns
t_A	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	25	-	-	25	-	-	25	-	ns
t_B	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	20	-	-	20	-	-	20	-	ns
Q_{RR}	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	65	-	-	65	-	-	65	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	140	-	-	140	-	-	140	-	pF
$R_{\theta JC}$		-	-	1.0	-	-	1.0	-	-	1.0	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

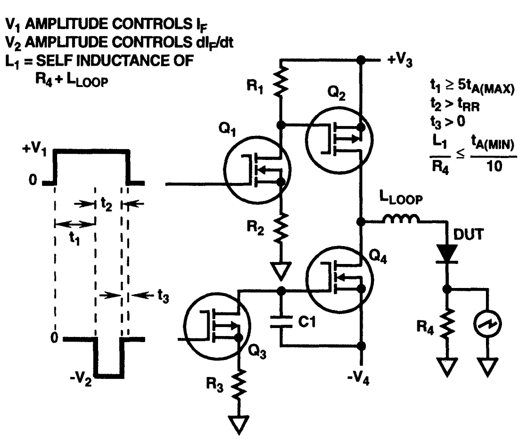


FIGURE 1. t_{RR} TEST CIRCUIT

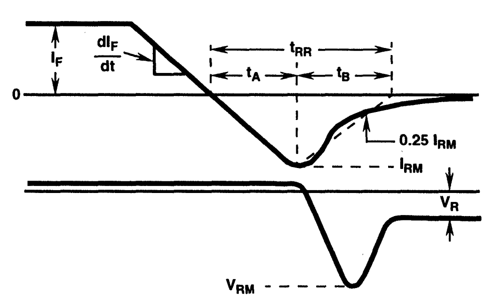


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

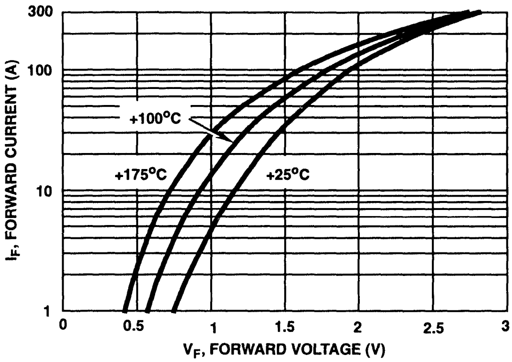


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

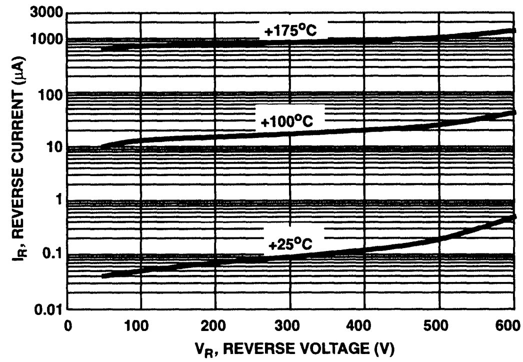


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

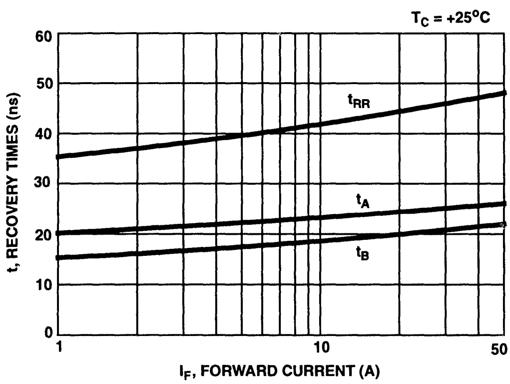


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

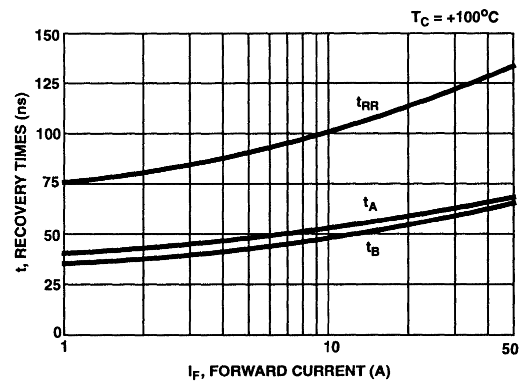


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

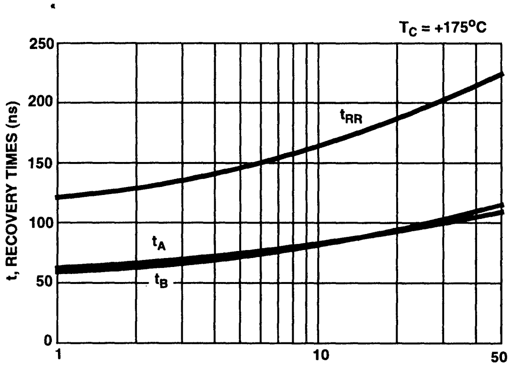


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

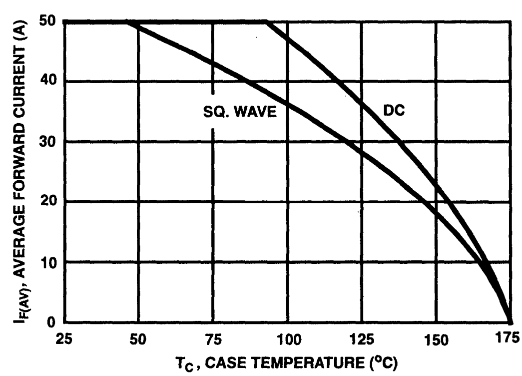


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

7

HYPERFAST SINGLE DIODES

Typical Performance Curves (Continued)

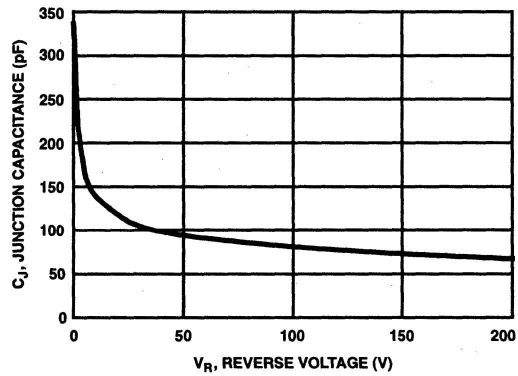


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

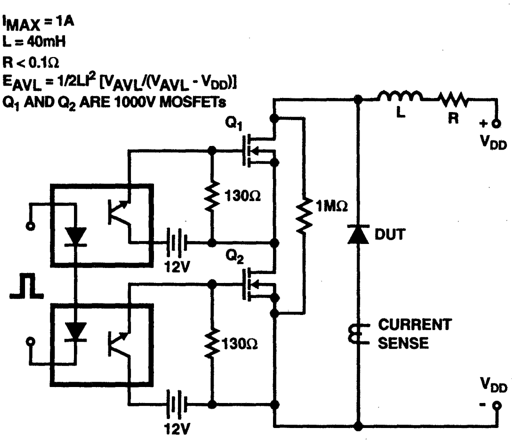


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

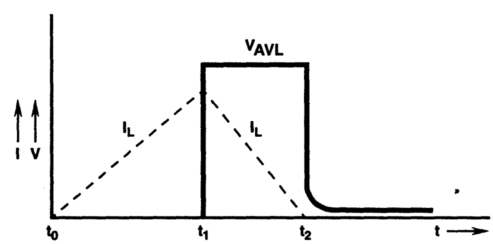


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRU5070, RHRU5080, RHRU5090 RHRU50100

HARRIS SEMICONDUCTOR

April 1995

50A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <75ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU5070, RHRU5080, RHRU5090 and RHRU50100 (TA49066) are hyperfast diodes with soft recovery characteristics (t_{RR} < 75ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

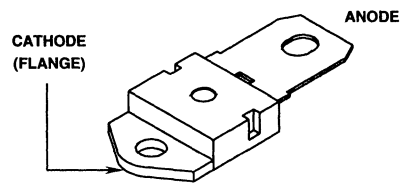
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU5070	TO-218	RHRU5070
RHRU5080	TO-218	RHRU5080
RHRU5090	TO-218	RHRU5090
RHRU50100	TO-218	RHRU50100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU5070	RHRU5080	RHRU5090	RHRU50100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +65°C)	$I_{F(AV)}$	50	50	50	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	100	100	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	500	500	500	A
Maximum Power Dissipation	P_D	150	150	150	150	W
Avalanche Energy (L = 40mH)	E_{AVL}	40	40	40	40	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU5070			RHRU5080			RHRU5090			RHRU50100			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 50A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 50A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	3.0	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	3.0	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	3.0	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	3.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	75	-	-	75	-	-	75	-	-	75	ns
	I_F = 50A, dI_F/dt = 100A/μs	-	-	95	-	-	95	-	-	95	-	-	95	ns
t_A	I_F = 50A, dI_F/dt = 100A/μs	-	54	-	-	54	-	-	54	-	-	54	-	ns
t_B	I_F = 50A, dI_F/dt = 100A/μs	-	32	-	-	32	-	-	32	-	-	32	-	ns
Q_{RR}	I_F = 50A, dI_F/dt = 100A/μs	-	125	-	-	125	-	-	125	-	-	125	-	nC
C_J	V_R = 10V, I_F = 0A	-	150	-	-	150	-	-	150	-	-	150	-	pF
$R_{\theta JC}$		-	-	1.0	-	-	1.0	-	-	1.0	-	-	1.0	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figure 10 and Figure 11).

pw = Pulse width.

D = Duty cycle.

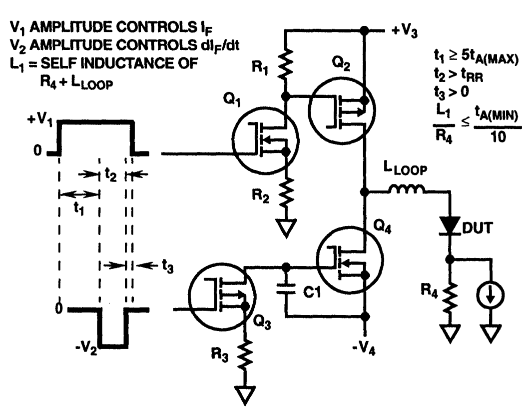


FIGURE 1. t_{RR} TEST CIRCUIT

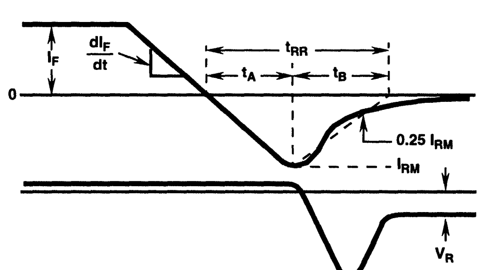


FIGURE 2. WAVEFORMS AND DEFINITIONS

Typical Performance Curves

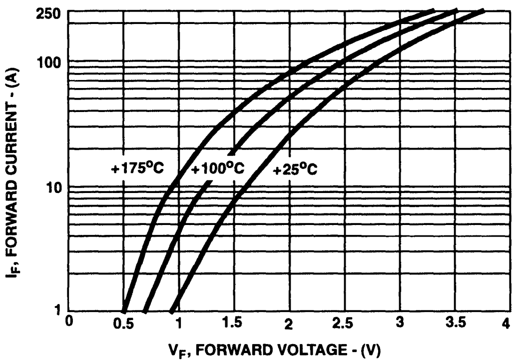


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

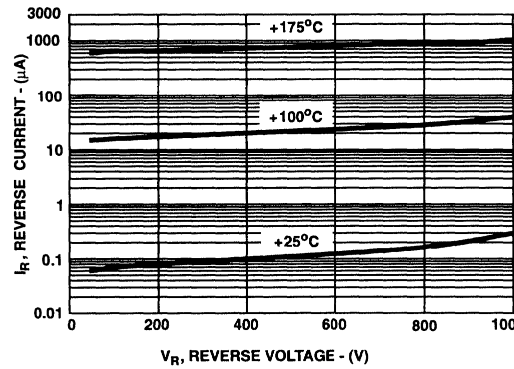


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

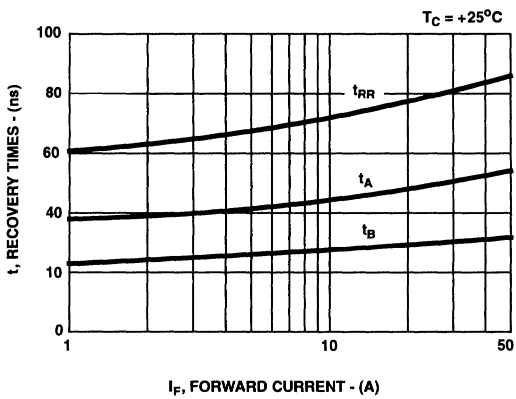


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

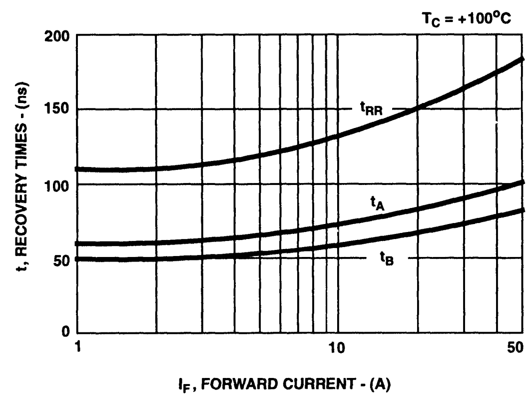


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

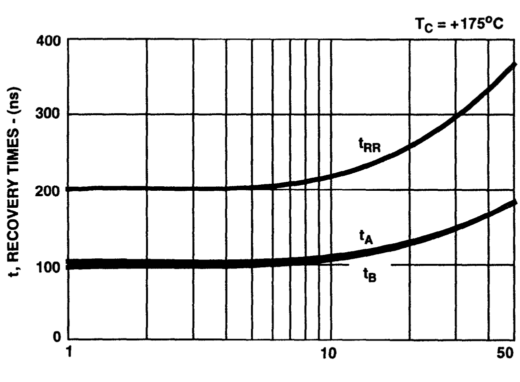


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

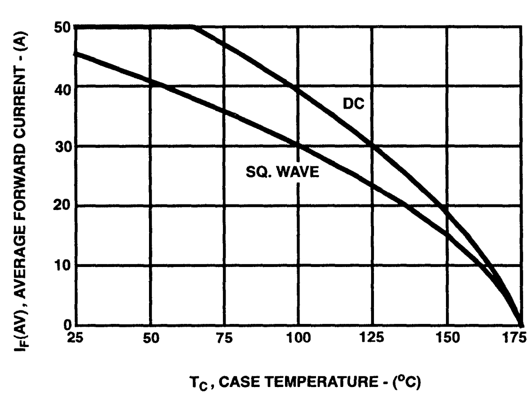


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

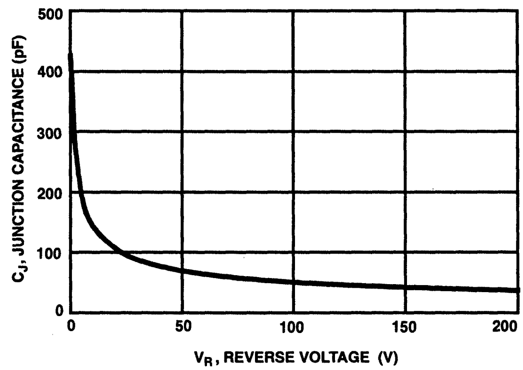


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

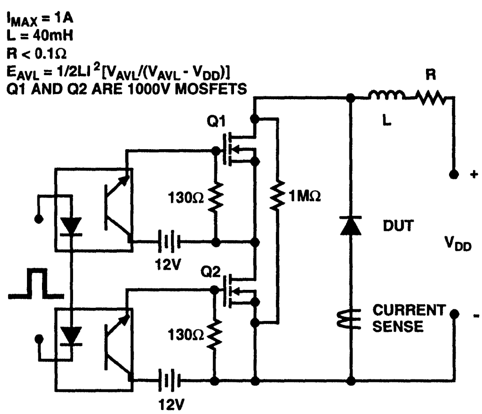


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

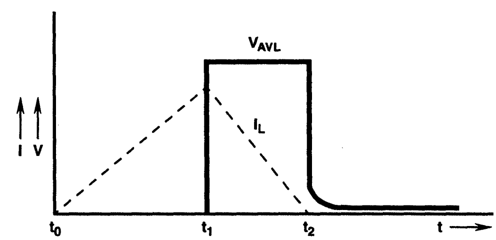


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

RHRU50120

April 1995

50A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRU50120 (TA49100) are hyperfast diodes with soft recovery characteristics (t_{RR} < 85ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

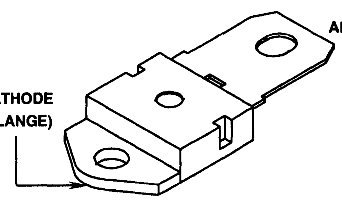
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU50120	TO-218	RHRU50120

NOTE: When ordering, use the entire part number.

Package

SINGLE LEAD JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU50120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 50°C)	$I_{F(AV)}$	50	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	100	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	150	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU50120 LIMITS MIN	TYP	MAX	UNITS
V_F	$I_F = 50A$, $T_C = +25^oC$	-	-	3.2	V
	$I_F = 50A$, $T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	500	μA
	$V_R = 1200V$, $T_C = +150^oC$	-	-	1.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$	-	-	85	ns
	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	-	100	ns
t_A	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	50	-	ns
t_B	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	40	-	ns
Q_{RR}	$I_F = 50A$, $dI_F/dt = 100A/\mu s$	-	240	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	150	-	pF
$R_{\theta JC}$		-	-	1.0	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

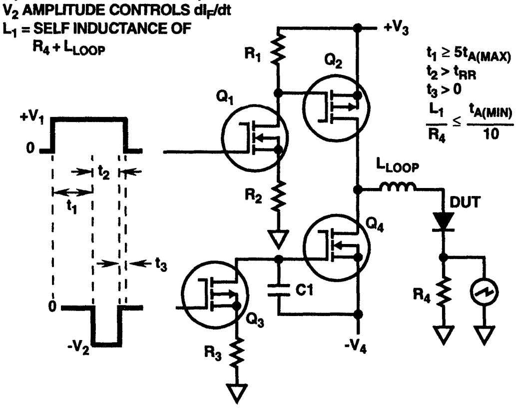


FIGURE 1. t_{RR} TEST CIRCUIT

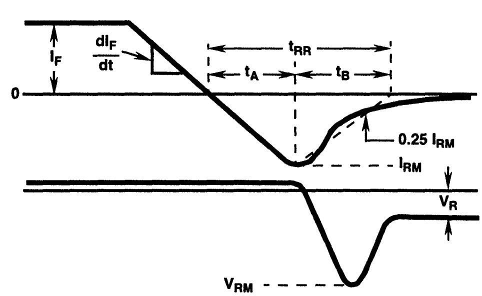


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

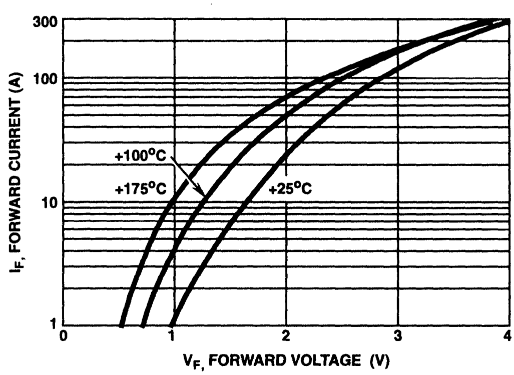


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

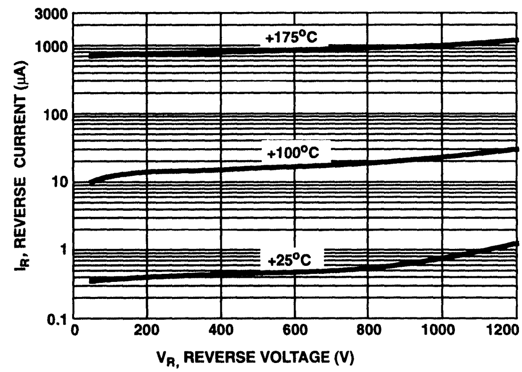


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

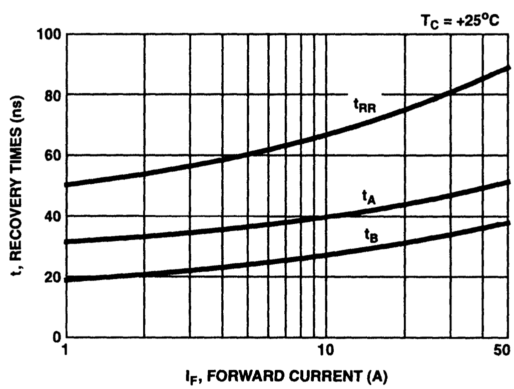


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

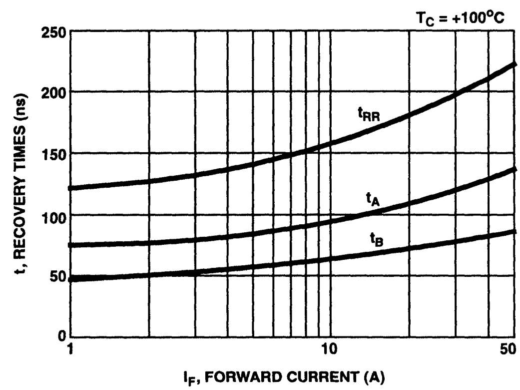


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

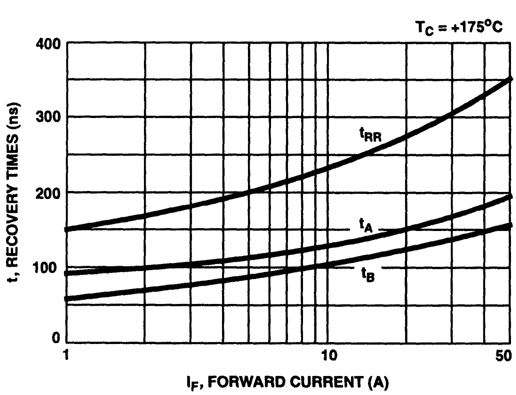


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

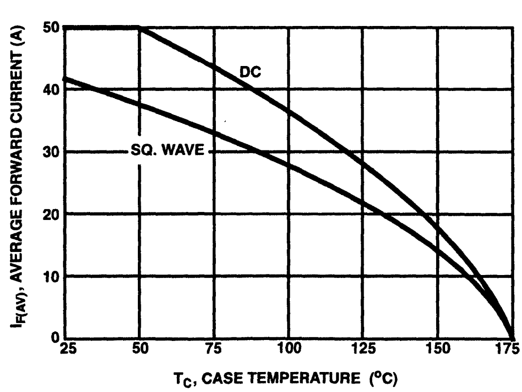


FIGURE 8. CURRENT DERATING CURVE

7

HYPERFAST SINGLE DIODES

Typical Performance Curves (Continued)

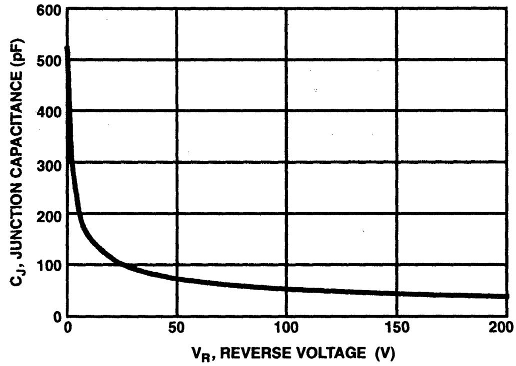


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

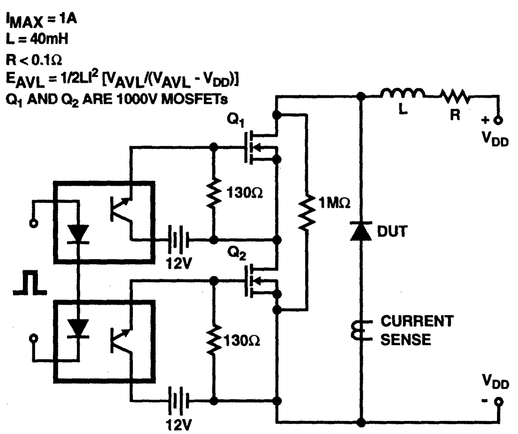


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

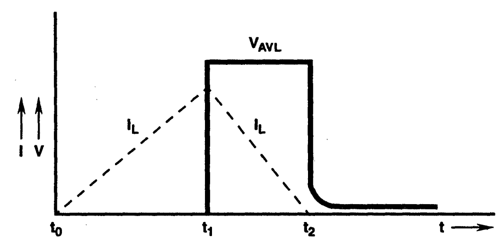


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU7540, RHRU7550, RHRU7560

April 1995

75A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <55ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU7540, RHRU7550 and RHRU7560 (TA49067) are hyperfast diodes with soft recovery characteristics (t_{RR} < 55ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

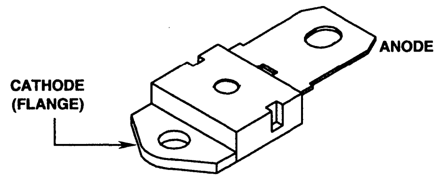
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU7540	TO-218	RHRU7540
RHRU7550	TO-218	RHRU7550
RHRU7560	TO-218	RHRU7560

NOTE: When ordering, use the entire part number.

Package

SINGLE LEAD JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU7540	RHRU7550	RHRU7560	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +80°C)	$I_{F(AV)}$	75	75	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	150	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	750	750	750	A
Maximum Power Dissipation	P_D	190	190	190	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3945.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU7540			RHRU7550			RHRU7560			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 75A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
	I_F = 75A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = +150°C	-	-	2.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	2.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/µs	-	-	55	-	-	55	-	-	55	ns
	I_F = 75A, dI_F/dt = 100A/µs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 75A, dI_F/dt = 100A/µs	-	35	-	-	35	-	-	35	-	ns
t_B	I_F = 75A, dI_F/dt = 100A/µs	-	18	-	-	18	-	-	18	-	ns
Q_{RR}	I_F = 75A, dI_F/dt = 100A/µs	-	90	-	-	90	-	-	90	-	nC
C_J	V_R = 10V, I_F = 0A	-	200	-	-	200	-	-	200	-	pF
$R_{\theta JC}$		-	-	0.8	-	-	0.8	-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

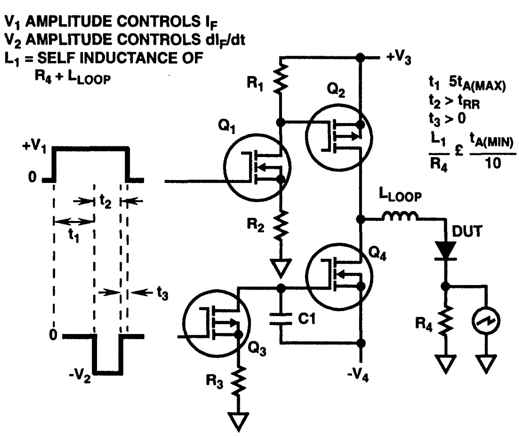


FIGURE 1. t_{RR} **TEST CIRCUIT**

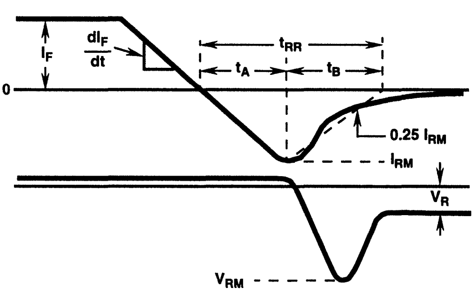


FIGURE 2. t_{RR} **WAVEFORMS AND DEFINITIONS**

Typical Performance Curves

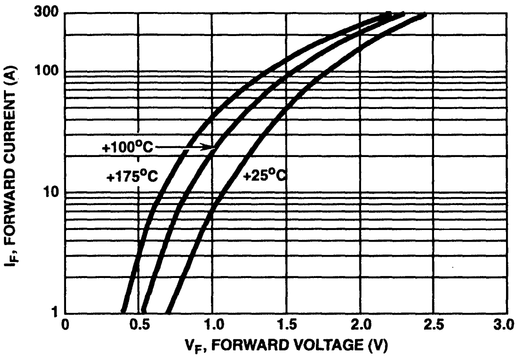


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

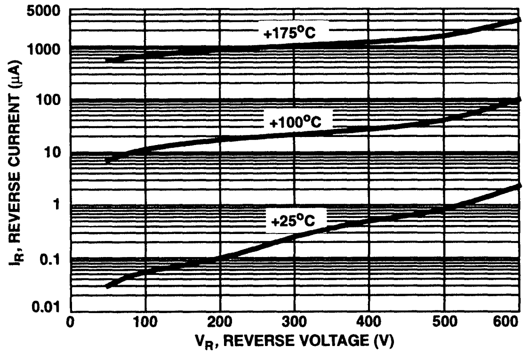


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

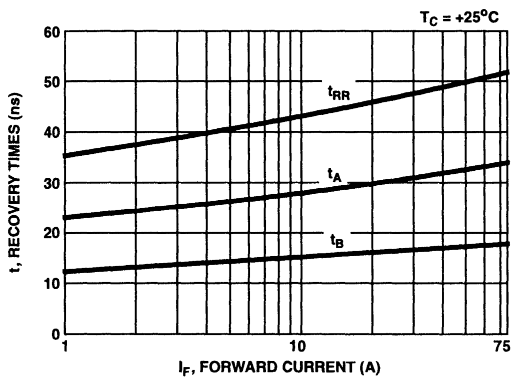


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

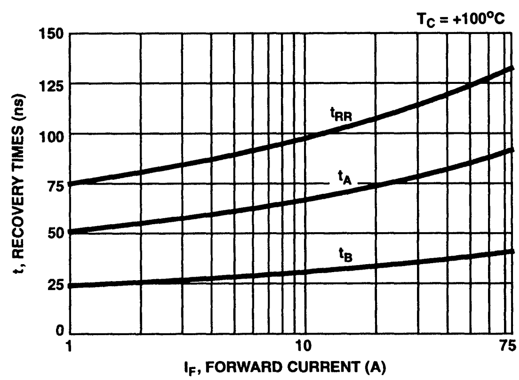


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

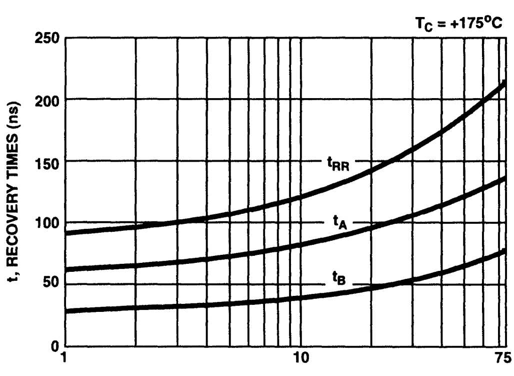


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

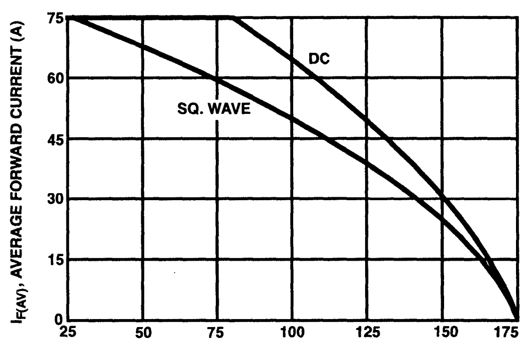


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

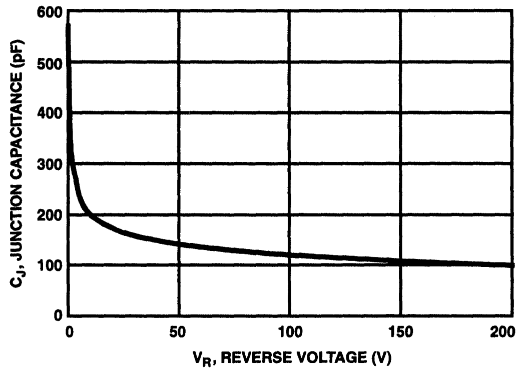


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

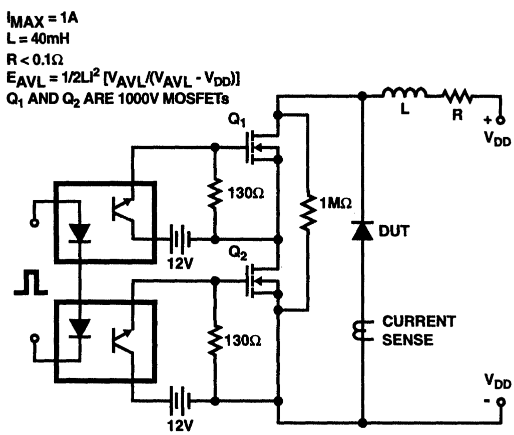


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

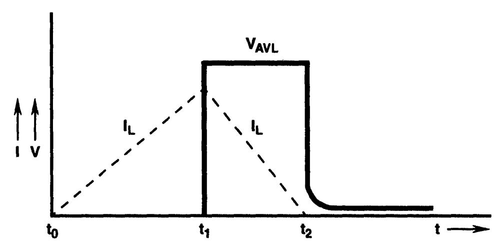


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORM

RHRU7570, RHRU7580, RHRU7590, RHRU75100

April 1995

75A, 700V - 1000V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU7570, RHRU7580, RHRU7590 and RHRU75100 (TA49068) are hyperfast diodes with soft recovery characteristics (t_{RR} < 85ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

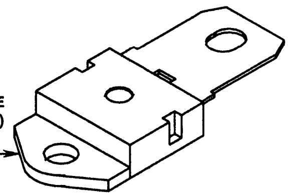
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU7570	TO-218	RHRU7570
RHRU7580	TO-218	RHRU7580
RHRU7590	TO-218	RHRU7590
RHRU75100	TO-218	RHRU75100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU7570	RHRU7580	RHRU7590	RHRU75100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +52°C)	$I_{F(AV)}$	75	75	75	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	150	150	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	750	750	750	750	A
Maximum Power Dissipation	P_D	190	190	190	190	W
Avalanche Energy (L = 40mH) (See Figures 10 and 11)	E_{AVL}	50	50	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU7570			RHRU7580			RHRU7590			RHRU75100			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 75A, T_C = +25^oC$	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	$I_F = 75A, T_C = +150^oC$	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	$V_R = 700V, T_C = +25^oC$	-	-	500	-	-	-	-	-	-	-	-	-	μA
	$V_R = 800V, T_C = +25^oC$	-	-	-	-	-	500	-	-	-	-	-	-	μA
	$V_R = 900V, T_C = +25^oC$	-	-	-	-	-	-	-	-	500	-	-	-	μA
	$V_R = 1000V, T_C = +25^oC$	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 700V, T_C = +150^oC$	-	-	2.0	-	-	-	-	-	-	-	-	-	mA
	$V_R = 800V, T_C = +150^oC$	-	-	-	-	-	2.0	-	-	-	-	-	-	mA
	$V_R = 900V, T_C = +150^oC$	-	-	-	-	-	-	-	-	2.0	-	-	-	mA
	$V_R = 1000V, T_C = +150^oC$	-	-	-	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	85	-	-	85	-	-	85	-	-	85	ns
	$I_F = 75A, dI_F/dt = 100A/\mu s$	-	-	100	-	-	100	-	-	100	-	-	100	ns
t_A	$I_F = 75A, dI_F/dt = 100A/\mu s$	-	55	-	-	55	-	-	55	-	-	55	-	ns
t_B	$I_F = 75A, dI_F/dt = 100A/\mu s$	-	40	-	-	40	-	-	40	-	-	40	-	ns
Q_{RR}	$I_F = 75A, dI_F/dt = 100A/\mu s$	-	240	-	-	240	-	-	240	-	-	240	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	220	-	-	220	-	-	220	-	-	220	-	pF
$R_{\theta JC}$		-	-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

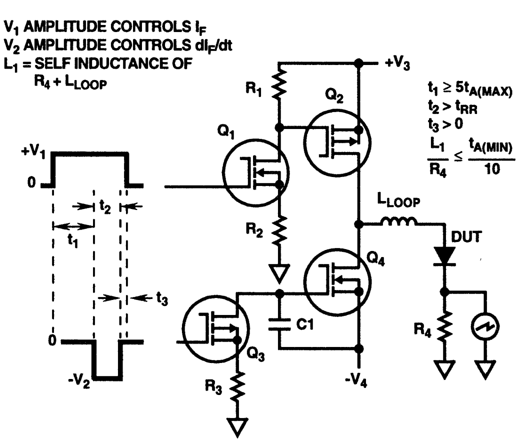


FIGURE 1. t_{RR} TEST CIRCUIT

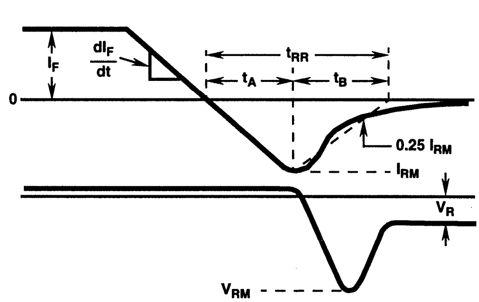


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

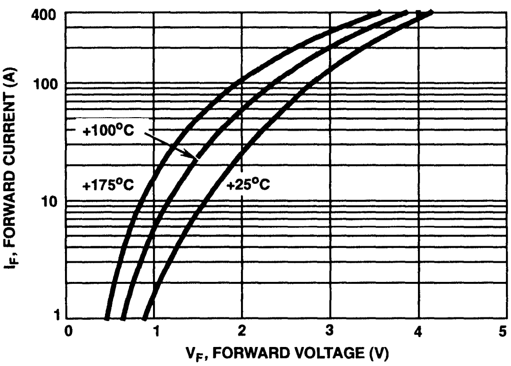


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

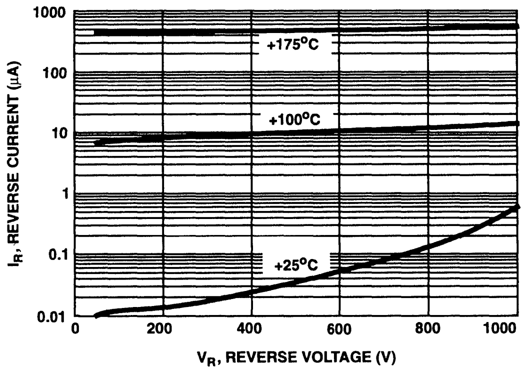


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

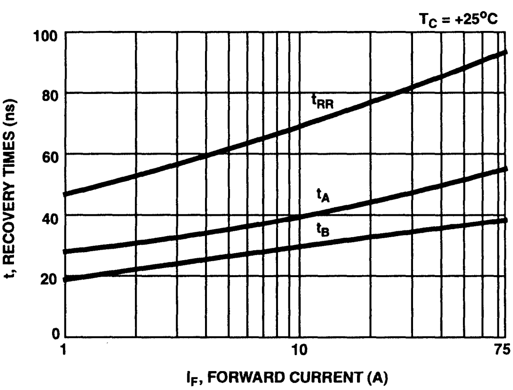


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

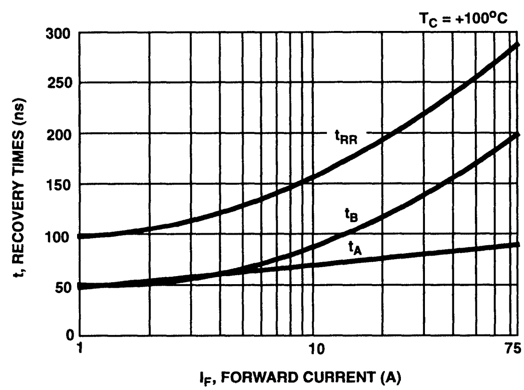


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

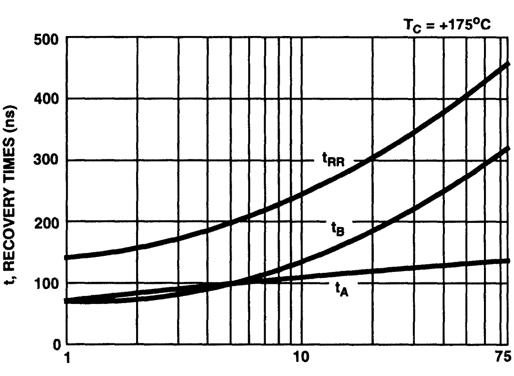


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

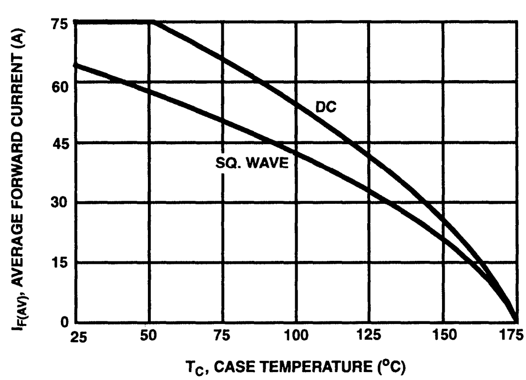


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

7

HYPERFAST SINGLE DIODES

Typical Performance Curves (Continued)

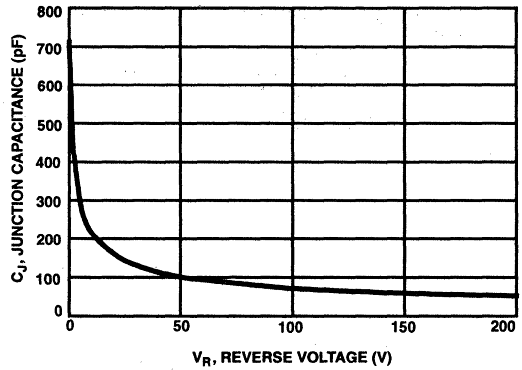


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

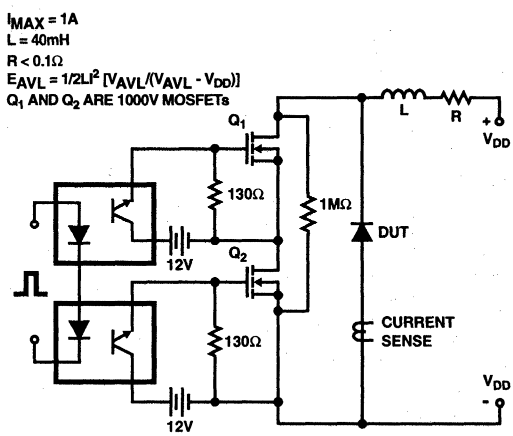


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

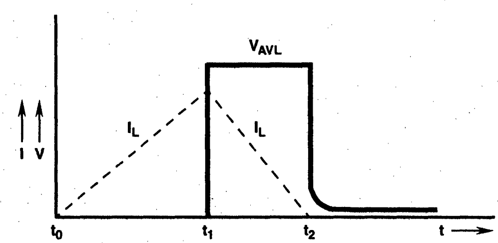


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU75120

April 1995

75A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery . . . . <85ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRU75120 (TA49042) is a hyperfast diode with soft recovery characteristics (t_{RR} < 85ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of high frequency switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

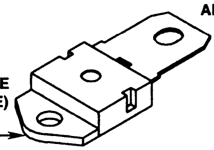
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU75120	TO-218	RHRU75120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings $T_C = +25°C$

		RHRU75120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +46°C)	$I_{F(AV)}$	75	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	150	A
Nonrepetitive Peak Surge Current (Halfwave, 1Phase, 60Hz)	I_{FSM}	500	A
Maximum Power Dissipation	P_D	190	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3408.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS			UNITS
			MIN	TYP	MAX	
V_F	I_F = 75A		-	-	3.2	V
V_F	I_F = 75A	T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V		-	-	500	μA
I_R	V_R = 1200V	T_C = +150°C	-	-	2	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs		-	-	85	ns
t_{RR}	I_F = 75A, dI_F/dt = 100A/μs		-	-	100	ns
t_A	I_F = 75A, dI_F/dt = 100A/μs		-	60	-	ns
t_B	I_F = 75A, dI_F/dt = 100A/μs		-	25	-	ns
$R_{\theta JC}$			-	-	0.8	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current at (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

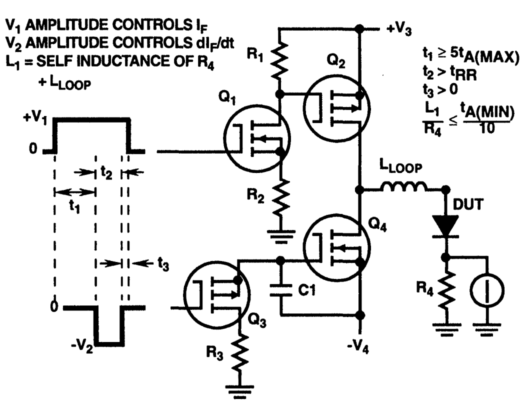


FIGURE 1. t_{RR} TEST CIRCUIT

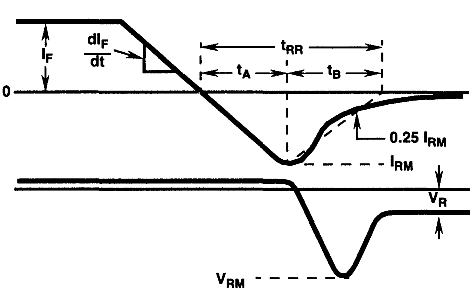


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

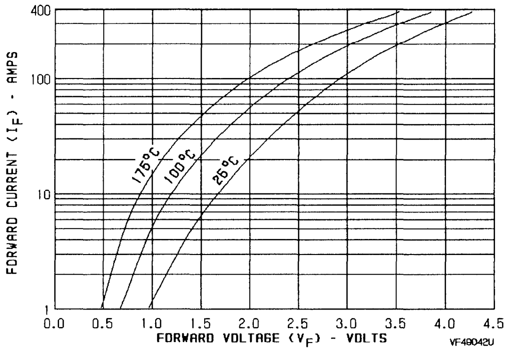


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

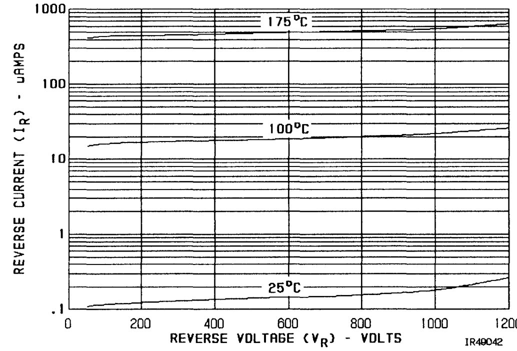


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

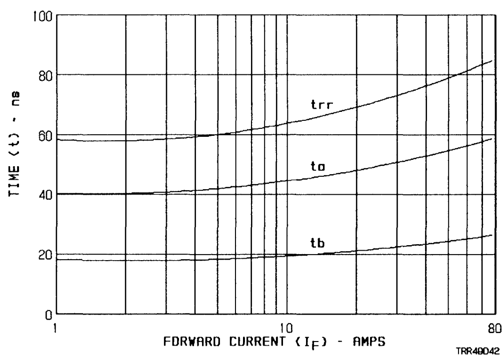


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

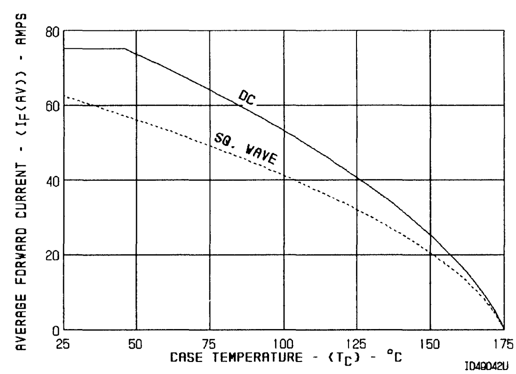


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

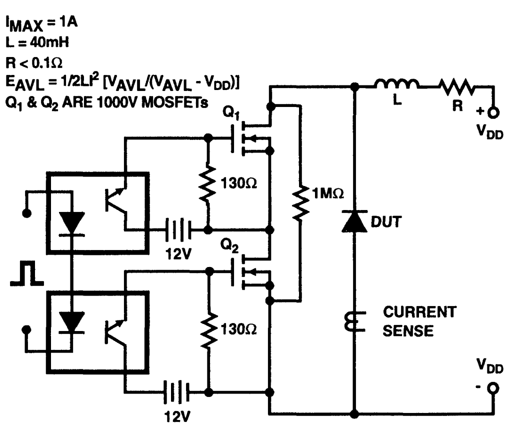


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

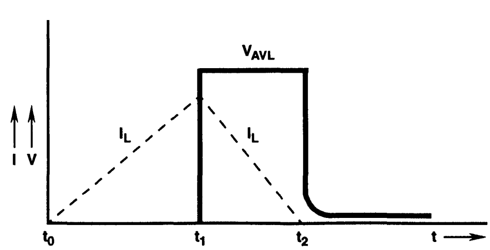


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU10040, RHRU10050, RHRU10060

April 1995

100A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . < 50ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up to 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU10040, RHRU10050 and RHRU10060 (TA49069) are hyperfast diodes with soft recovery characteristics (t_{RR} < 50ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

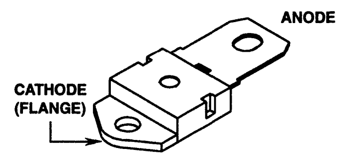
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU10040	TO-218	RHRU10040
RHRU10050	TO-218	RHRU10050
RHRU10060	TO-218	RHRU10060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings $T_C = +25°C$

	RHRU10040	RHRU10050	RHRU10060	UNITS
Peak Repetitive Reverse Voltage . . . . V_{RRM}	400	500	600	V
Working Peak Reverse Voltage . . . . V_{RWM}	400	500	600	V
DC Blocking Voltage . . . . V_R	400	500	600	V
Average Rectified Forward Current . . . . $I_{F(AV)}$ (T_C = +60.8°C)	100	100	100	A
Repetitive Peak Surge Current . . . . I_{FSM} (Square Wave, 20kHz)	200	200	200	A
Nonrepetitive Peak Surge Current . . . . I_{FSM} (Halfwave, 1 Phase, 60Hz)	1000	1000	1000	A
Maximum Power Dissipation . . . . P_D	210	210	210	W
Avalanche Energy . . . . E_{AVL} (L = 40mH)	50	50	50	mj
Operating and Storage Temperature . . . . T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3572.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRU10040 LIMITS			RHRU10050 LIMITS			RHRU10060 LIMITS			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 100A	-	-	2.1	-	-	2.1	-	-	2.1	V
V_F	I_F = 100A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V	-	-	500	-	-	-	-	-	-	μA
	V_R= 500V	-	-	-	-	-	500	-	-	-	μA
	V_R = 600V	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 400V, T_C = +150°C	-	-	2.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	2.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	50	-	-	50	-	-	50	ns
t_{RR}	I_F = 100A, dI_F/dt = 100A/μs	-	-	60	-	-	60	-	-	60	ns
t_A	I_F = 100A, dI_F/dt = 100A/μs	-	28	-	-	28	-	-	28	-	ns
t_B	I_F = 100A, dI_F/dt = 100A/μs	-	18	-	-	18	-	-	18	-	ns
$R_{\theta JC}$		-	-	0.71	-	-	0.71	-	-	0.71	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

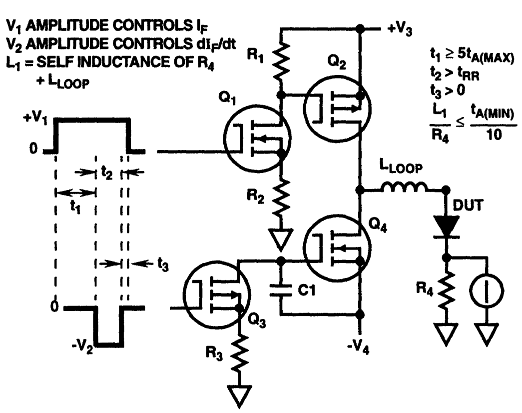


FIGURE 1. t_{RR} TEST CIRCUIT

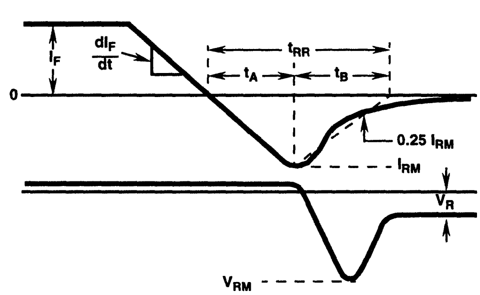


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

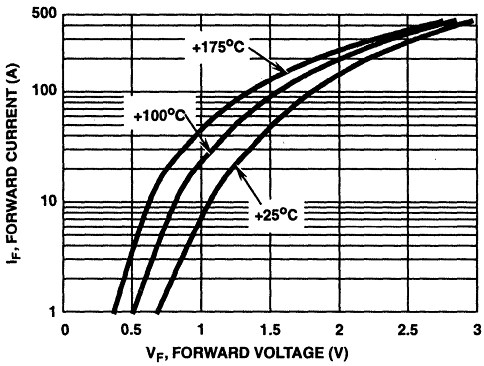


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

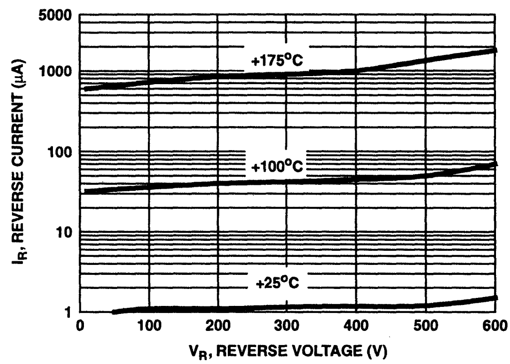


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

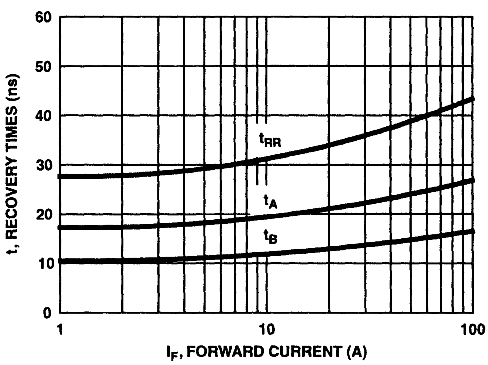


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

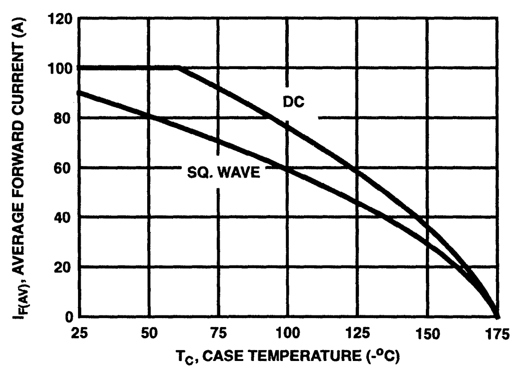


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

I_{MAX} = 1A
L = 40mH
R < 0.1Ω
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 & Q_2 ARE 1000V MOSFETs

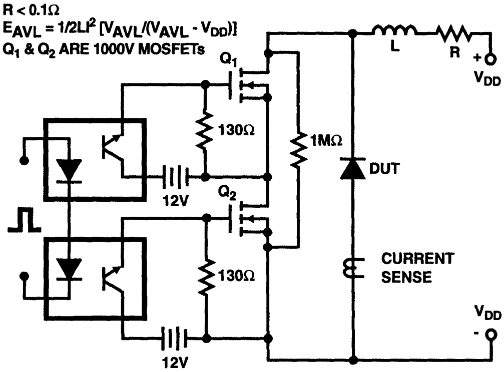


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

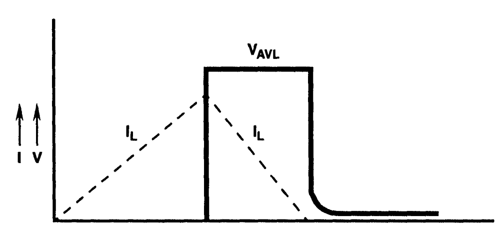


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU100120

April 1995

100A, 1200V Hyperfast Diode

Features

- Hyperfast with Soft Recovery................<90ns
- Operating Temperature....................+175°C
- Reverse Voltage..........................1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRU100120 (TA49070) is a hyperfast diode with soft recovery characteristics (t_{RR} < 90ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

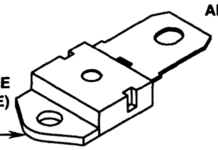
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU100120	TO-218	RHR100120

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU100120	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +62.5°C)	$I_{F(AV)}$	100	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	200	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1000	A
Maximum Power Dissipation	P_D	300	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS			UNITS
			MIN	TYP	MAX	
V_F	$I_F = 100A$	$T_C = +25^oC$	-	-	3.2	V
V_F	$I_F = 100A$	$T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$	$T_C = +25^oC$	-	-	500	µA
I_R	$V_R = 1200V$	$T_C = +150^oC$	-	-	2	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$		-	-	90	ns
	$I_F = 100A$, $dI_F/dt = 100A/\mu s$		-	-	100	ns
t_A	$I_F = 100A$, $dI_F/dt = 100A/\mu s$		-	60	-	ns
t_B	$I_F = 100A$, $dI_F/dt = 100A/\mu s$		-	25	-	ns
$R_{\theta JC}$			-	-	0.5	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

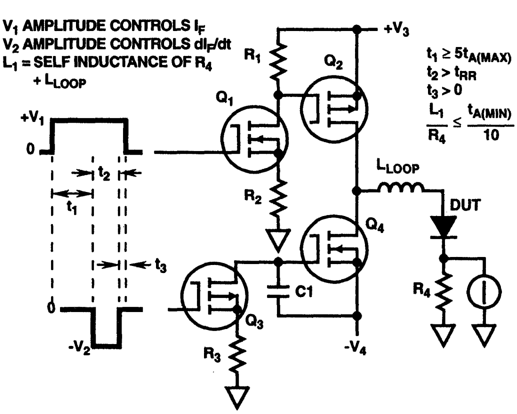


FIGURE 1. t_{RR} TEST CIRCUIT

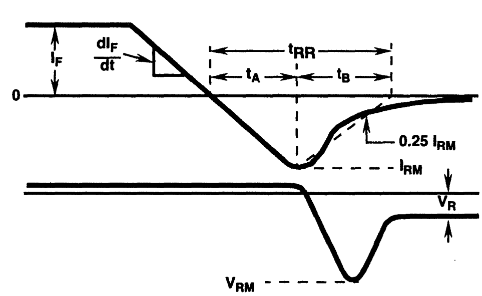


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

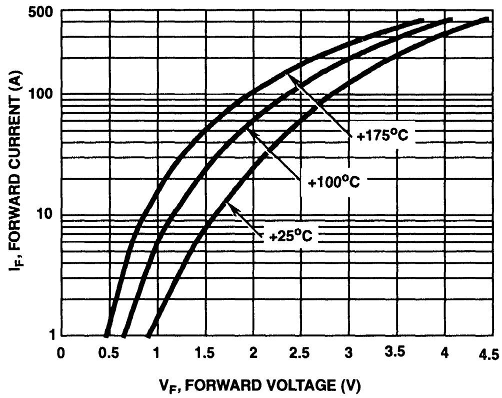


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

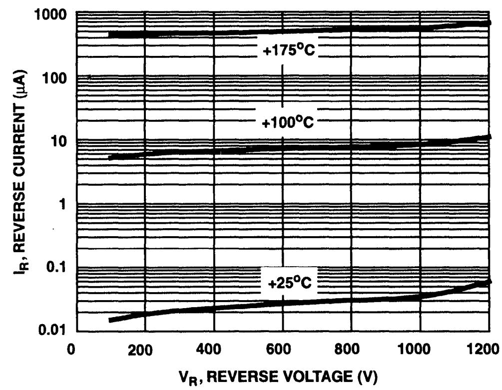


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

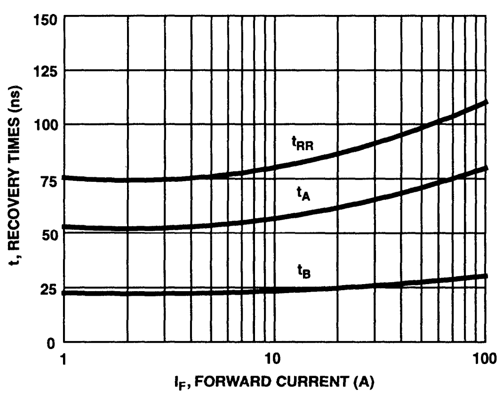


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

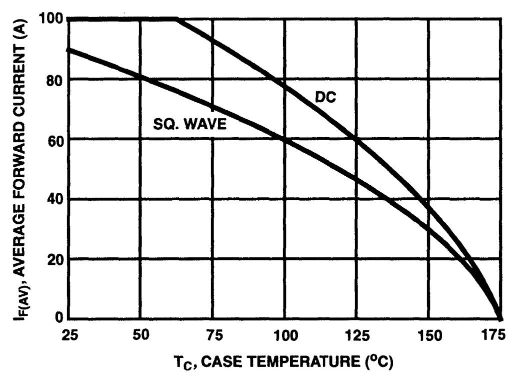


FIGURE 6. CURRENT DERATING CURVE

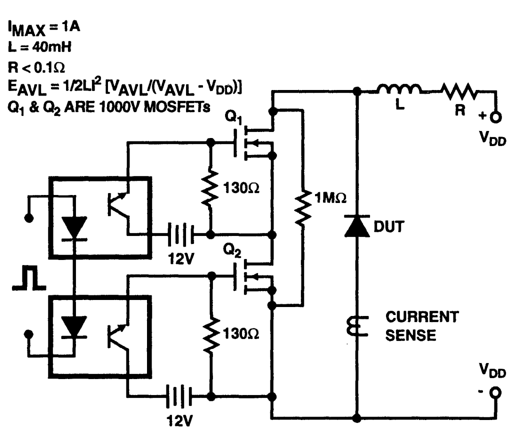


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

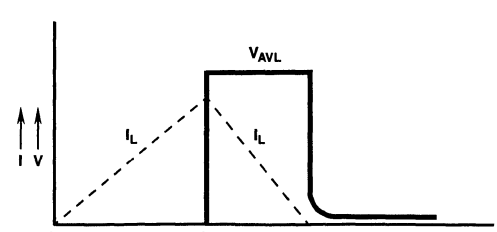


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

7
HYPERFAST SINGLE DIODES

HARRIS SEMICONDUCTOR

RHRU15040, RHRU15050, RHRU15060

April 1995

150A, 400V - 600V Hyperfast Diodes

Features

- Hyperfast with Soft Recovery . . . . <60ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRU15040, RHRU15050 and RHRU15060 (TA49071) are hyperfast diodes with soft recovery characteristics (t_{RR} < 60ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

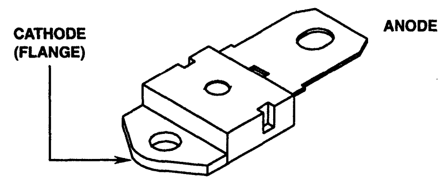
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU15040	TO-218	RHRU15040
RHRU15050	TO-218	RHRU15050
RHRU15060	TO-218	RHRU15060

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

Absolute Maximum Ratings $T_C = +25°C$

		RHRU15040	RHRU15050	RHRU15060
Peak Repetitive Reverse Voltage	V_{RRM}	400V	500V	600V
Working Peak Reverse Voltage	V_{RWM}	400V	500V	600V
DC Blocking Voltage	V_R	400V	500V	600V
Average Rectified Forward Current (T_C = +72°C)	$I_{F(AV)}$	150A	150A	150A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	300A	300A	300A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1500A	1500A	1500A
Maximum Power Dissipation	P_D	375W	375W	375W
Avalanche Energy (L = 40mH)	E_{AVL}	50mj	50mj	50mj
Operating and Storage Temperature	T_{STG}, T_J	-65°C to +175°C	-65°C to +175°C	-65°C to +175°C

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION		RHRU15040 LIMITS			RHRU15050 LIMITS			RHRU15060 LIMITS			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 150A$		-	-	2.1	-	-	2.1	-	-	2.1	V
V_F	$I_F = 150A$	$T_C = +150^oC$	-	-	1.6	-	-	1.6	-	-	1.6	V
I_R	$V_R = 400V$		-	-	500	-	-	-	-	-	-	μA
	$V_R = 500V$		-	-	-	-	-	500	-	-	-	μA
	$V_R = 600V$		-	-	-	-	-	-	-	-	500	μA
I_R	$V_R = 400V$	$T_C = +150^oC$	-	-	2.0	-	-	-	-	-	-	mA
	$V_R = 500V$	$T_C = +150^oC$	-	-	-	-	-	2.0	-	-	-	mA
	$V_R = 600V$	$T_C = +150^oC$	-	-	-	-	-	-	-	-	2.0	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$		-	-	60	-	-	60	-	-	60	ns
t_{RR}	$I_F = 150A$, $dI_F/dt = 100A/\mu s$		-	-	70	-	-	70	-	-	70	ns
t_A	$I_F = 150A$, $dI_F/dt = 100A/\mu s$		-	43	-	-	43	-	-	43	-	ns
t_B	$I_F = 150A$, $dI_F/dt = 100A/\mu s$		-	20	-	-	20	-	-	20	-	ns
$R_{\theta JC}$			-	-	0.4	-	-	0.4	-	-	0.4	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 7 and 8).

pw = pulse width.

D = duty cycle.

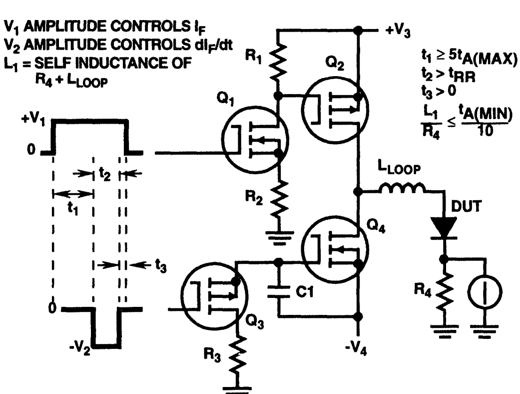


FIGURE 1. t_{RR} **TEST CIRCUIT**

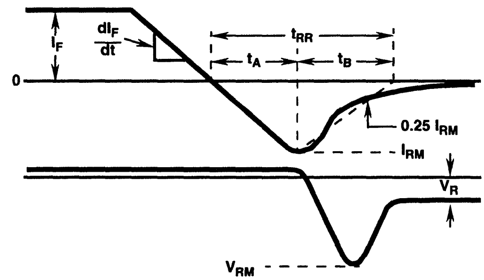


FIGURE 2. t_{RR} **WAVEFORMS AND DEFINITIONS**

Typical Performance Curves

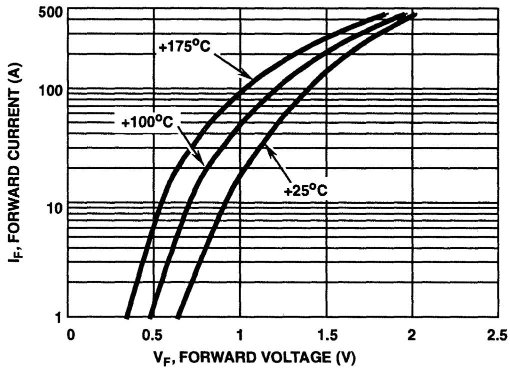


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

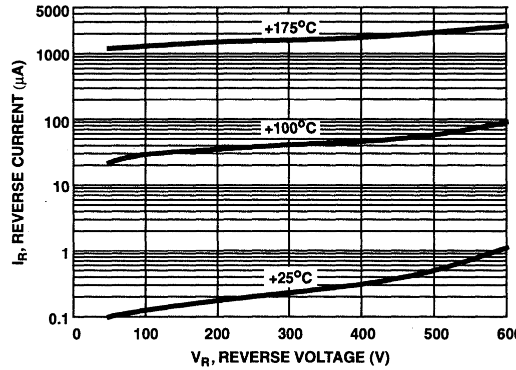


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

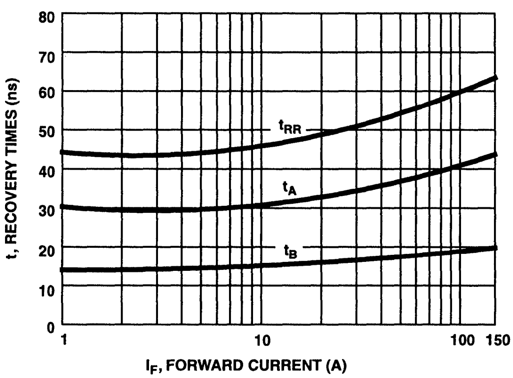


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

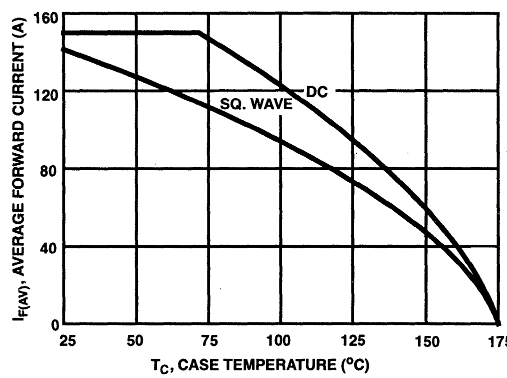


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

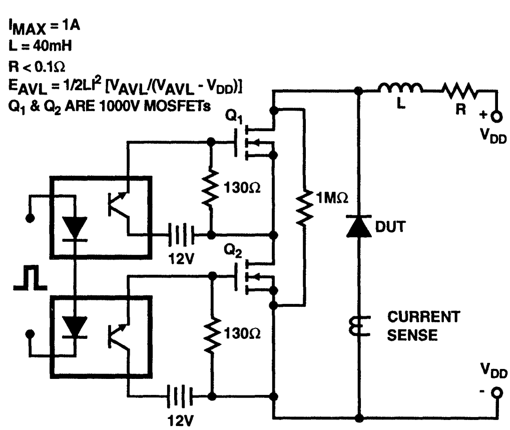


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

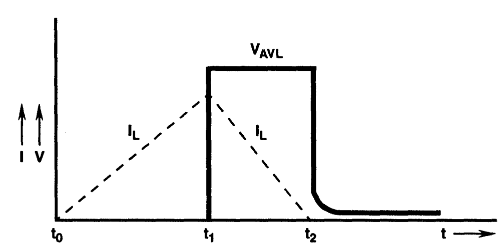


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRU15090, RHRU150100

April 1995

150A, 900V - 1000V Hyperfast Diodes

Features

- **Hyperfast with Soft Recovery .... <90ns**
- **Operating Temperature .... +175°C**
- **Reverse Voltage Up To 1000V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRU15090 and RHRU150100 (TA49072) are hyperfast diodes with soft recovery characteristics (t_{RR} < 90ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

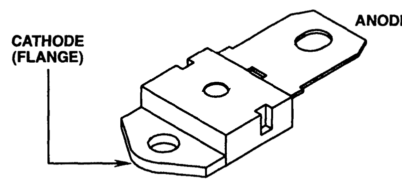
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRU15090	TO-218	RHRU15090
RHRU150100	TO-218	RHR150100

NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-218



Symbol

7

HYPERFAST SINGLE DIODES

Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RHRU15090	RHRU150100	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	900	1000	V
DC Blocking Voltage	V_R	900	1000	V
Average Rectified Forward Current (T_C = +42°C)	$I_{F(AV)}$	150	150	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	300	300	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	1500	1500	A
Maximum Power Dissipation	P_D	375	375	W
Avalanche Energy (L = 40mH)	E_{AVL}	50	50	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	°C

File Number **3589.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS						UNITS
		RHRU15090			RHRU150100			
		MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 150A, T_C = +25°C	-	-	3.0	-	-	3.0	V
V_F	I_F = 150A, T_C = +150°C	-	-	2.5	-	-	2.5	V
I_R	V_R = 900V, T_C = +25°C	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	500	μA
I_R	V_R = 900V, T_C = +150°C	-	-	3.0	-	-	-	mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	3.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	90	-	-	90	ns
	I_F = 150A, dI_F/dt = 100A/μs	-	-	100	-	-	100	ns
t_A	I_F = 150A, dI_F/dt = 100A/μs	-	65	-	-	65	-	ns
t_B	I_F = 150A, dI_F/dt = 100A/μs	-	30	-	-	30	-	ns
$R_{\theta JC}$		-	-	0.4	-	-	0.4	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

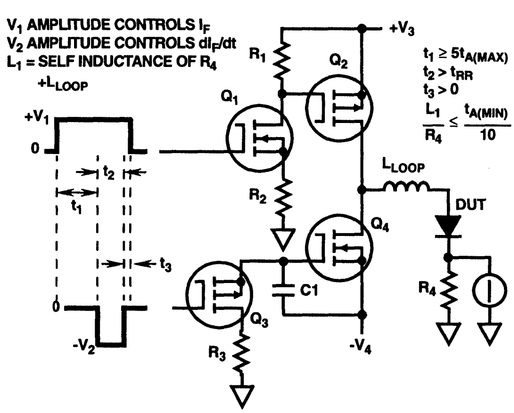


FIGURE 1. t_{RR} TEST CIRCUIT

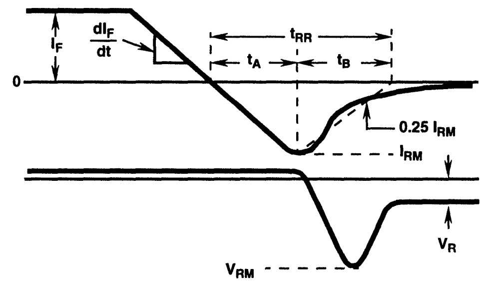


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

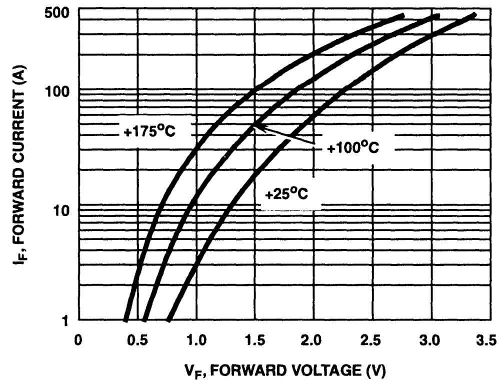


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

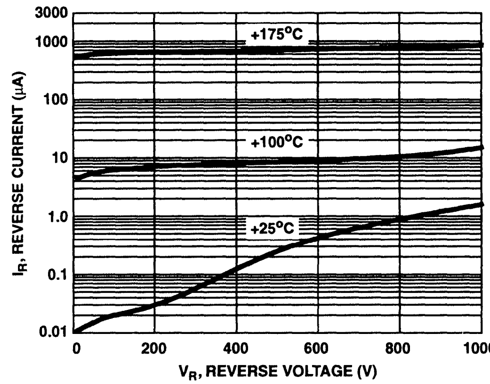


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

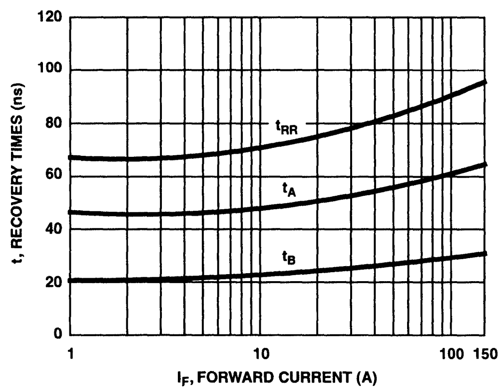


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

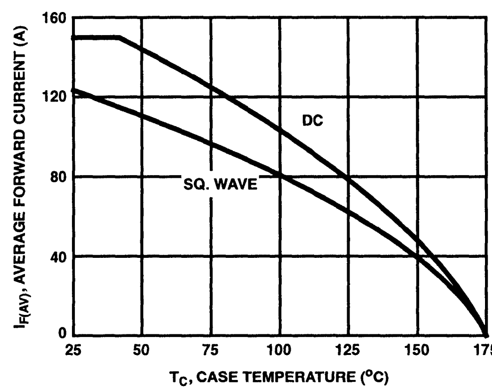


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

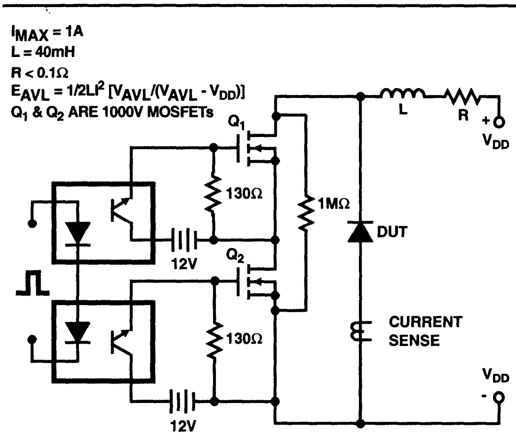


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

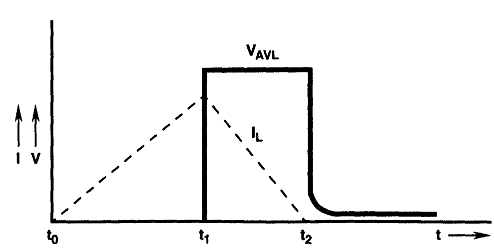
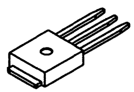
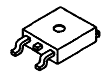
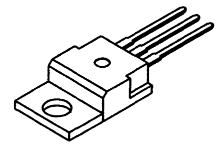
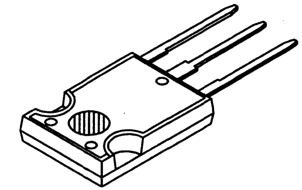


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

MCT/IGBT/DIODES 8

HYPERFAST DUAL DIODES

HARRIS DUAL HYPER-FAST RECOVERY RECTIFIER PRODUCT LINE

	 TO-251AA	 TO-252AA	 TO-220AB			 TO-247	
	$I_{F(AVG)}$	$I_{F(AVG)}$	$I_{F(AVG)}$			$I_{F(AVG)}$	
V_{RRM}	4Ax2	4Ax2	4Ax2	6Ax2	8Ax2	15Ax2	30Ax2
400V	*RHRD440CC* 2.1V 35ns	*RHRD440CCS* 2.1V 35ns		*RHRP640CC* 2.1V 35ns	RHRP840CC 2.1V 35ns	RHRG1540CC 2.1V 40ns	RHRG3040CC 2.1V 45ns
500V	*RHRD450CC* 2.1V 35ns	*RHRD450CCS* 2.1V 35ns		*RHRP650CC* 2.1V 35ns	RHRP850CC 2.1V 35ns	RHRG1550CC 2.1V 40ns	RHRG3050CC 2.1V 45ns
600V	*RHRD460CC* 2.1V 35ns	*RHRD460CCS* 2.1V 35ns		*RHRP660CC* 2.1V 35ns	RHRP860CC 2.1V 35ns	RHRG1560CC 2.1V 40ns	RHRG3060CC 2.1V 45ns
700V					RHRP870CC 3.0V 65ns	RHRG1570CC 3.0V 70ns	RHRG3070CC 3.0V 75ns
800V					RHRP880CC 3.0V 65ns	RHRG1580CC 3.0V 70ns	RHRG3080CC 3.0V 75ns
900V					RHRP890CC 3.0V 65ns	RHRG1590CC 3.0V 70ns	RHRG3090CC 3.0V 75ns
1000V					RHRP8100CC 3.0V 65ns	RHRG15100CC 3.0V 70ns	RHRG30100CC 3.0V 75ns
1200V			*RHRP4120CC* 3.2V 70ns	*RHRP6120CC* 3.2V 65ns	RHRP8120CC 3.2V 65ns	RHRG15120CC 3.2V 75ns	RHRG30120CC 3.2V 75ns

ITALICS = Future Product Offerings; V_F at $I_{F(AVG)}$, $T_J = 25^oC$; T_{RR} at $I_{F(AVG)}$, $dI_F/dt = 100A/\mu sec$ $T_J = 25^oC$; † T_{RR} at $I_F = 1A$.

HARRIS SEMICONDUCTOR

RHRP840CC, RHRP850CC, RHRP860CC

April 1995

8A, 400V - 600V Hyperfast Dual Diodes

Features

- **Hyperfast with Soft Recovery . . . . <30ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage Up To 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRP840CC, RHRP850CC and RHRP860CC (TA49059) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 30ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

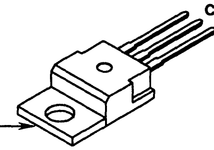
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP840CC	TO-220AB	RHRP840C
RHRP850CC	TO-220AB	RHRP850C
RHRP860CC	TO-220AB	RHRP860C

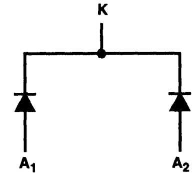
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol



8 HYPERFAST DUAL DIODES

Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RHRP840CC	RHRP850CC	RHRP860CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = 150°C)	$I_{F(AV)}$	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	A
Maximum Power Dissipation	P_D	75	75	75	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3964.1**

Electrical Specifications (per leg) $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS RHRP840CC MIN	TYP	MAX	RHRP850CC MIN	TYP	MAX	RHRP860CC MIN	TYP	MAX	UNITS
V_F	$I_F = 8A$, $T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 8A$, $T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V$, $T_C = +25^oC$	-	-	100	-	-	-	-	-	-	µA
	$V_R = 500V$, $T_C = +25^oC$	-	-	-	-	-	100	-	-	-	µA
	$V_R = 600V$, $T_C = +25^oC$	-	-	-	-	-	-	-	-	100	µA
I_R	$V_R = 400V$, $T_C = +150^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V$, $T_C = +150^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V$, $T_C = +150^oC$	-	-	-	-	-	-	-	-	500	µA
t_{RR}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	-	30	-	-	30	-	-	30	ns
	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	-	35	-	-	35	-	-	35	ns
t_A	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	18	-	-	18	-	-	18	-	ns
t_B	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	10	-	-	10	-	-	10	-	ns
Q_{RR}	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	56	-	-	56	-	-	56	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	25	-	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	2	-	-	2	-	-	2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

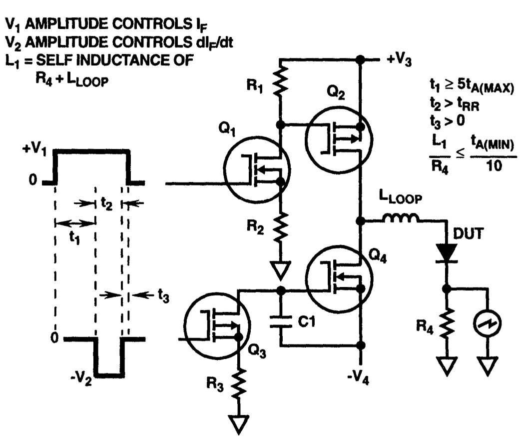


FIGURE 1. t_{RR} TEST CIRCUIT

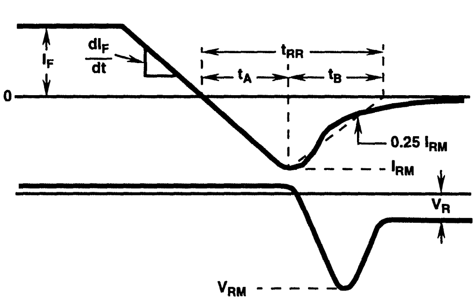


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

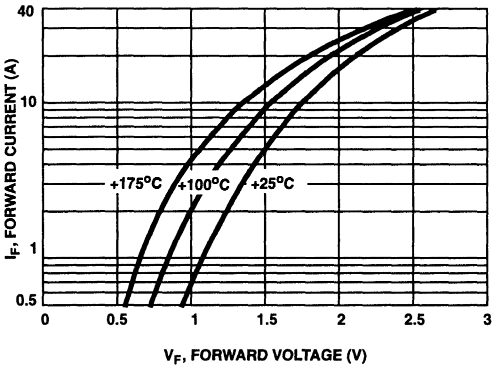


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

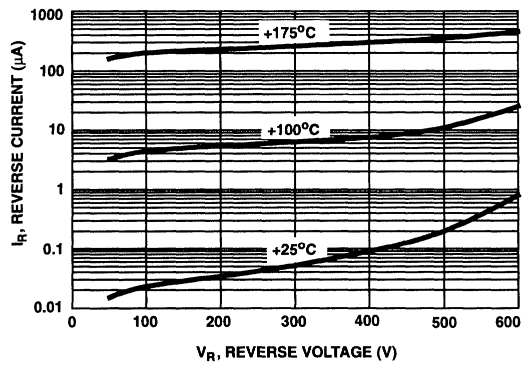


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

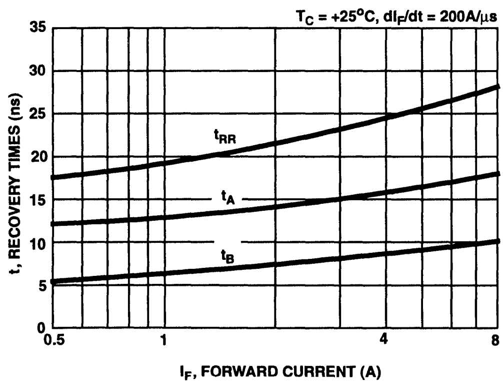


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

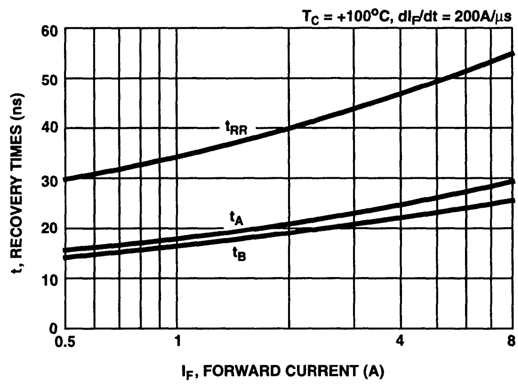


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

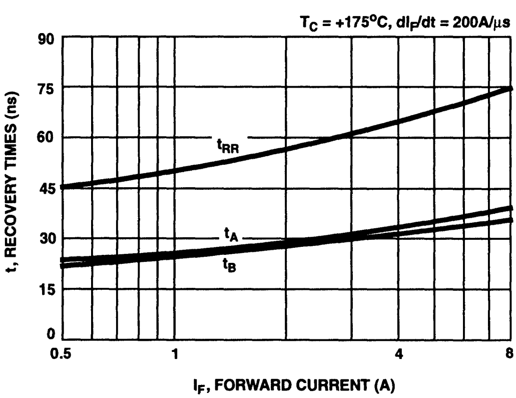


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

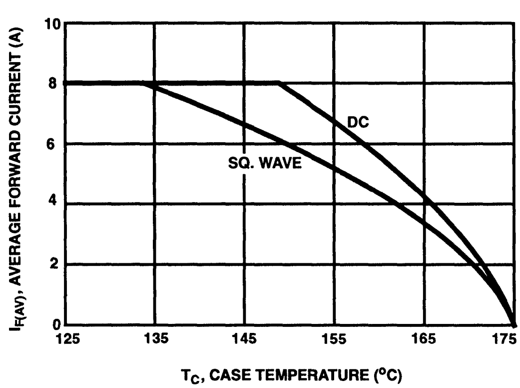


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

8

HYPERFAST DUAL DIODES

Typical Performance Curves (Continued)

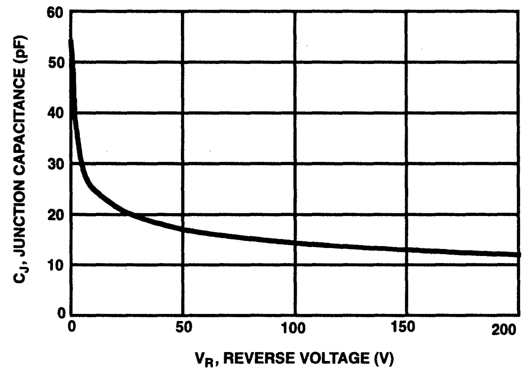


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

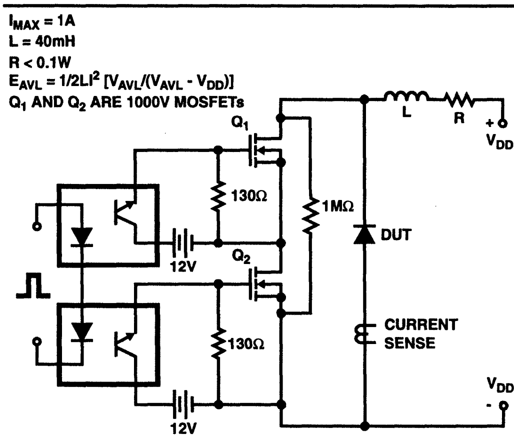


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

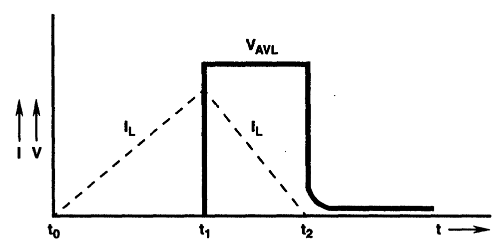


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP870CC, RHRP880CC, RHRP890CC, RHRP8100CC

April 1995

8A, 700V - 1000V Hyperfast Dual Diodes

Features

- Hyperfast with Soft Recovery .... <55ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRP870CC, RHRP880CC, RHRP890CC and RHRP8100CC (TA49060) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 55ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

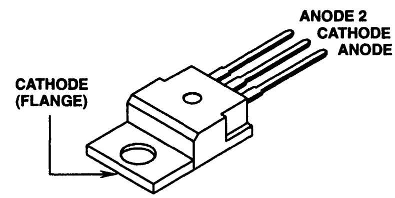
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP870CC	TO-220AB	RHRP870C
RHRP880CC	TO-220AB	RHRP880C
RHRP890CC	TO-220AB	RHRP890C
RHRP8100CC	TO-220AB	RHR8100C

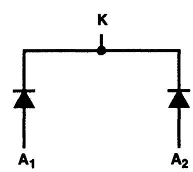
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol



Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RHRP870CC	RHRP880CC	RHRP890CC	RHRP8100CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	8	8	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	16	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	100	100	A
Maximum Power Dissipation	P_D	75	75	75	75	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS												UNITS
		RHRP870CC			RHRP880CC			RHRP890CC			RHRP8100CC			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 8A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 8A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	100	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	100	-	-	-	-	-	-	µA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	100	-	-	-	µA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	100	µA
I_R	V_R = 700V, T_C = +150°C	-	-	500	-	-	-	-	-	-	-	-	-	µA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	500	-	-	-	-	-	-	µA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	--	-	-	500	-	-	-	µA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	500	µA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	55	-	-	55	-	-	55	-	-	60	ns
	I_F = 8A, dI_F/dt = 200A/µs	-	-	65	-	-	65	-	-	65	-	-	65	ns
t_A	I_F = 8A, dI_F/dt = 200A/µs	-	30	-	-	30	-	-	30	-	-	30	-	ns
t_B	I_F = 8A, dI_F/dt = 200A/µs	-	20	-	-	20	-	-	20	-	-	20	-	ns
Q_{RR}	I_F = 8A, dI_F/dt = 200A/µs	-	175	-	-	175	-	-	175	-	-	175	-	nC
C_J	V_R = 10V, I_F = 0A	-	30	-	-	30	-	-	30	-	-	30	-	pF
$R_{\theta JC}$		-	-	2.0	-	-	2.0	-	-	2.0	-	-	2.0	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

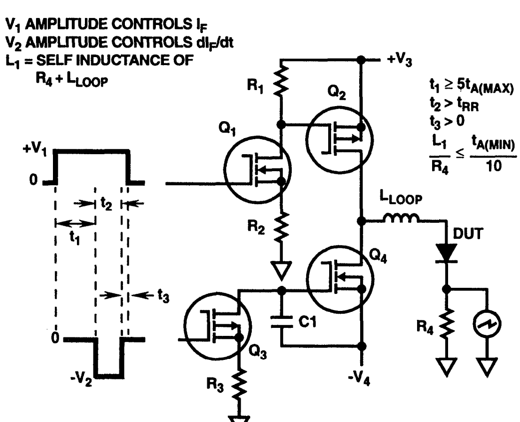


FIGURE 1. t_{RR} TEST CIRCUIT

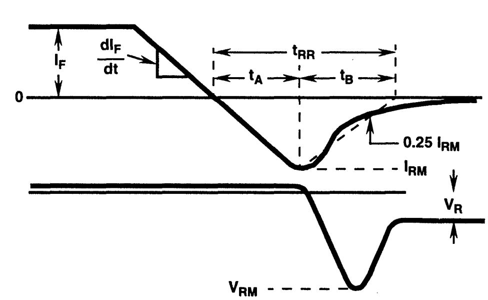


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

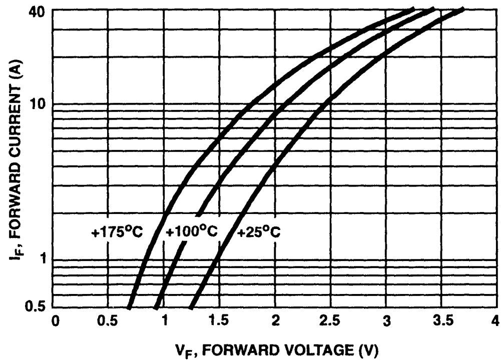


FIGURE 3. TYPICAL FORWARD CURRENT VS FORWARD VOLTAGE DROP

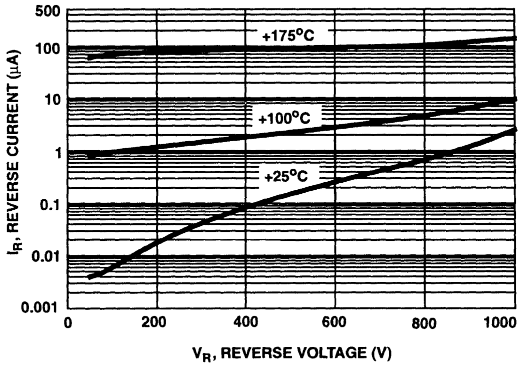


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

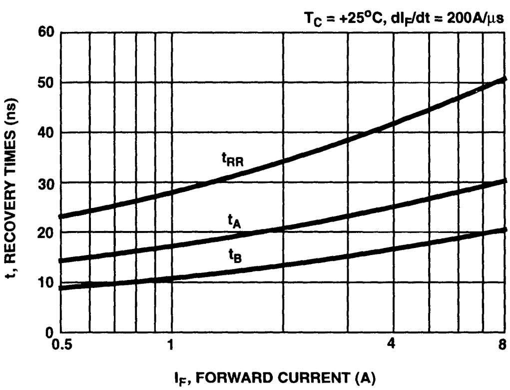


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

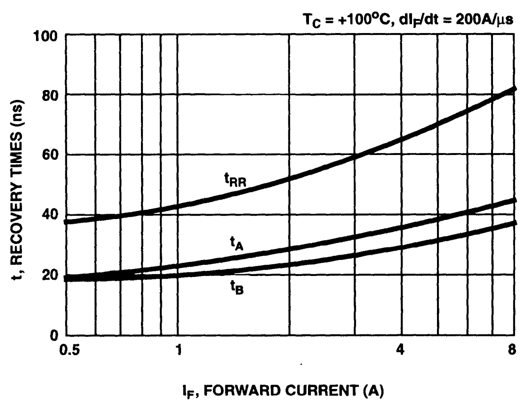


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

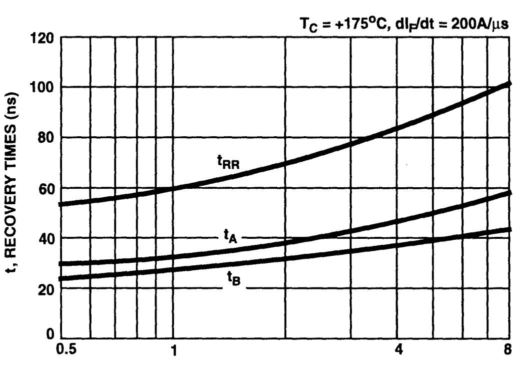


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

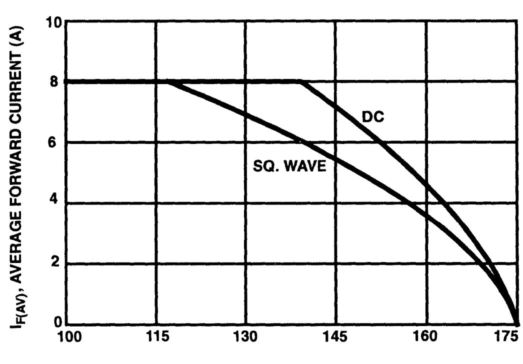


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

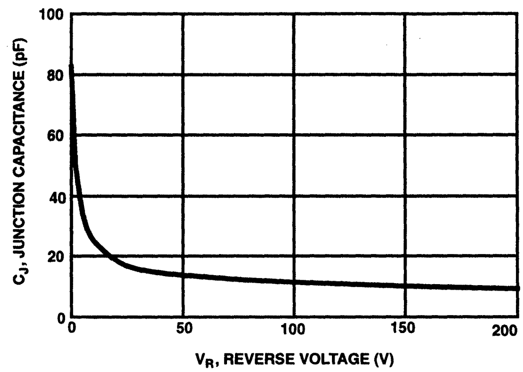


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

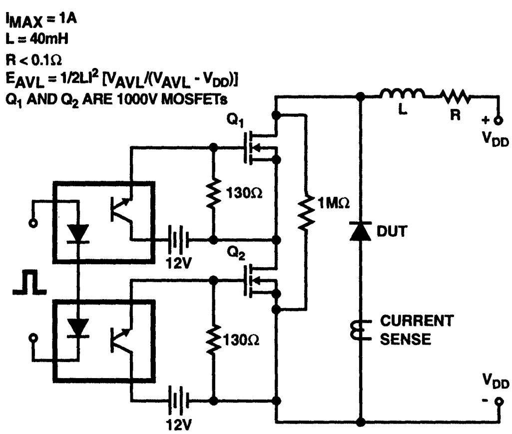


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

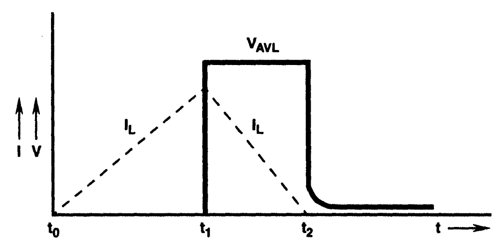


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRP8120CC

April 1995

8A, 1200V Hyperfast Dual Diode

Features

- Hyperfast with Soft Recovery .... <55ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRP8120CC (TA49096) is a hyperfast dual diode with soft recovery characteristics (t_{RR} < 55ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

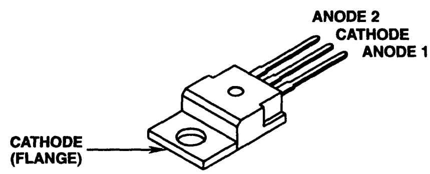
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRP8120CC	TO-220AB	RHR8120C

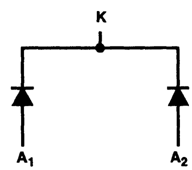
NOTE: When ordering, use the entire part number.

Package

JEDEC TO-220AB



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RHRP8120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	A
Maximum Power Dissipation	P_D	75	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3966.1**

Electrical Specifications (per leg) $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	LIMITS MIN	TYP	MAX	UNITS
V_F	$I_F = 8A$, $T_C = +25^oC$	-	-	3.2	V
	$I_F = 8A$, $T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$, $T_C = +25^oC$	-	-	100	μA
	$V_R = 1200V$, $T_C = +150^oC$	-	-	500	μA
t_{RR}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	-	55	ns
	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	-	65	ns
t_A	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	30	-	ns
t_B	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	20	-	ns
Q_{RR}	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	165	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	25	-	pF
$R_{\theta JC}$		-	-	2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

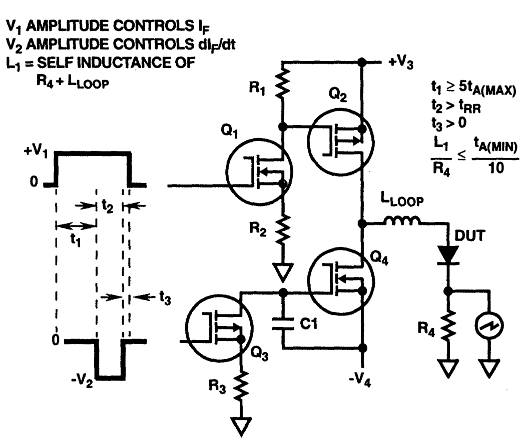


FIGURE 1. t_{RR} TEST CIRCUIT

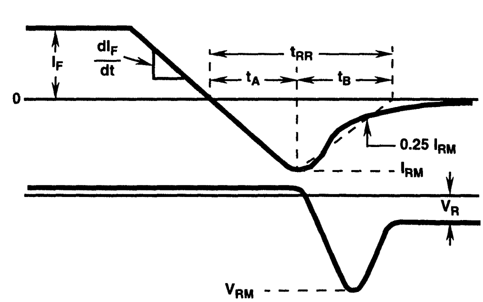


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

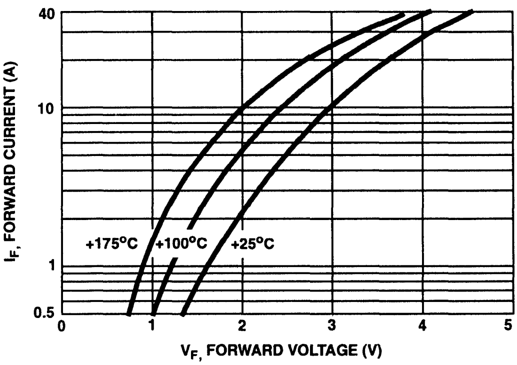


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

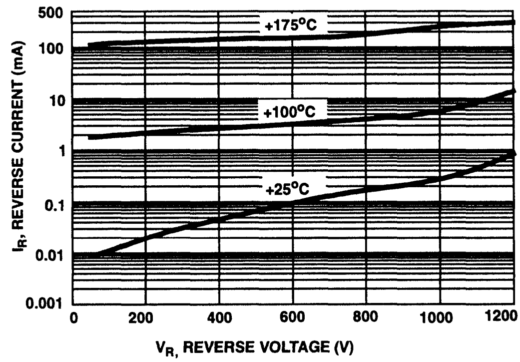


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

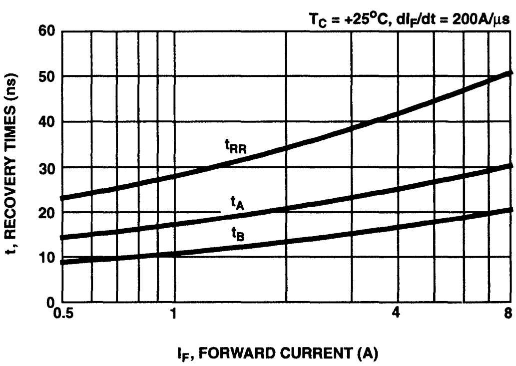


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

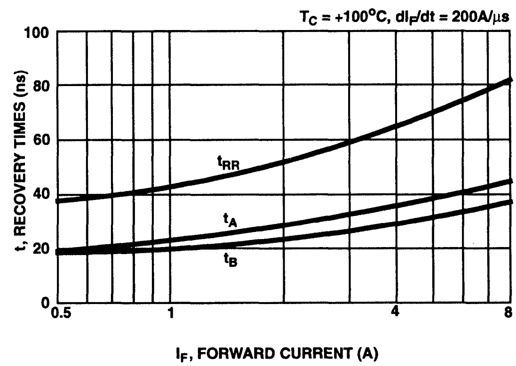


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

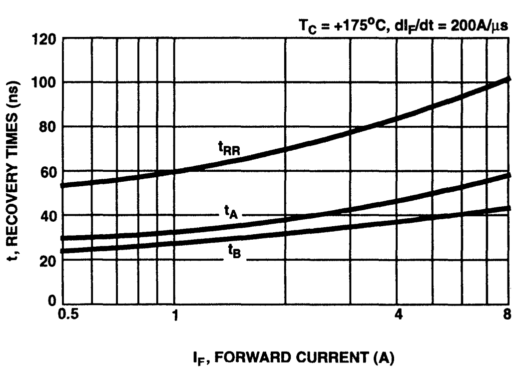


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

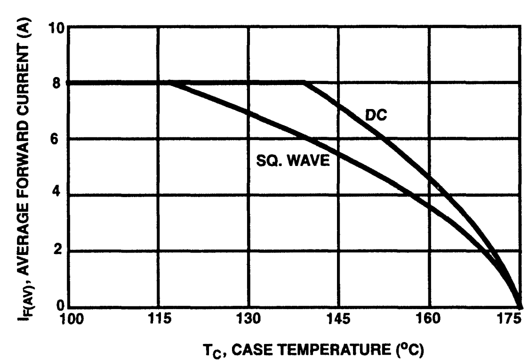


FIGURE 8. CURRENT DERATING CURVE

8
HYPERFAST DUAL DIODES

Typical Performance Curves (Continued)

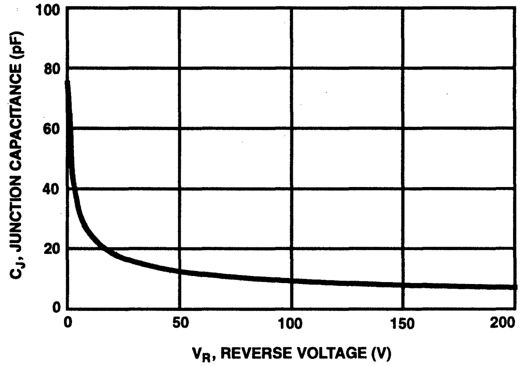


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

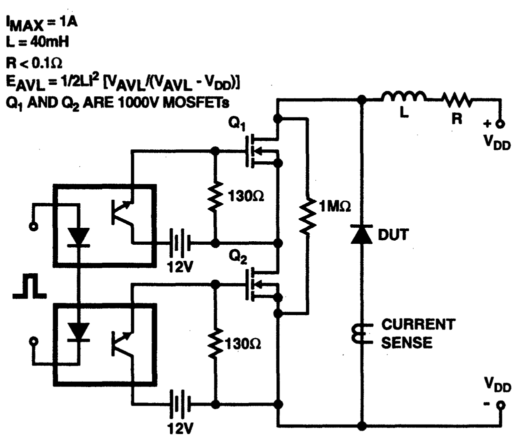


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

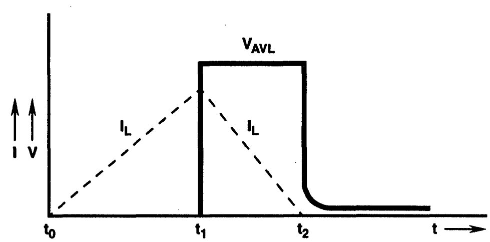


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG1540CC, RHRG1550CC, RHRG1560CC

April 1995

15A, 400V - 600V Hyperfast Dual Diodes

Features

- Hyperfast with Soft Recovery .... < 35ns
- Operating Temperature .... +175°C
- Reverse Voltage Up To 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG1540CC, RHRG1550CC and RHRG1560CC (TA49061) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 35ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

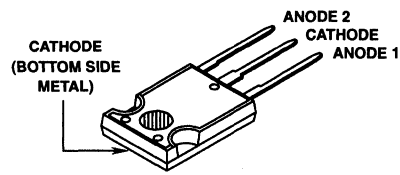
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG1540CC	TO-247	RHRG1540C
RHRG1550CC	TO-247	RHRG1550C
RHRG1560CC	TO-247	RHRG1560C

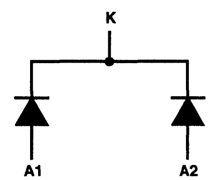
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings (Per Leg) T_C = +25°C, Unless Otherwise Specified

		RHRG1540CC	RHRG1550CC	RHRG1560CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +140°C)	$I_{F(AV)}$	15	15	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	30	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	200	200	A
Maximum Power Dissipation	P_D	100	100	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3684.1**

Electrical Specifications (Per Leg) $T_C = +25^oC$, Unless Otherwise Specified

		LIMITS									
		RHRG1540CC			RHRG1550CC			RHRG1560CC			
SYMBOL	TEST CONDITION	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
V_F	$I_F = 15A, T_C = +25^oC$	-	-	2.1	-	-	2.1	-	-	2.1	V
	$I_F = 15A, T_C = +150^oC$	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	$V_R = 400V, T_C = +25^oC$	-	-	100	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +25^oC$	-	-	-	-	-	100	-	-	-	µA
	$V_R = 600V, T_C = +25^oC$	-	-	-	-	-	-	-	-	100	µA
I_R	$V_R = 400V, T_C = +150^oC$	-	-	500	-	-	-	-	-	-	µA
	$V_R = 500V, T_C = +150^oC$	-	-	-	-	-	500	-	-	-	µA
	$V_R = 600V, T_C = +150^oC$	-	-	-	-	-	-	-	-	500	µA
t_{RR}	$I_F = 1A, dI_F/dt = 100A/\mu s$	-	-	35	-	-	35	-	-	35	ns
	$I_F = 15A, dI_F/dt = 100A/\mu s$	-	-	40	-	-	40	-	-	40	ns
t_A	$I_F = 15A, dI_F/dt = 100A/\mu s$	-	20	-	-	20	-	-	20	-	ns
t_B	$I_F = 15A, dI_F/dt = 100A/\mu s$	-	15	-	-	15	-	-	15	-	ns
Q_{RR}	$I_F = 15A, dI_F/dt = 100A/\mu s$	-	40	-	-	40	-	-	40	-	nC
C_J	$V_R = 10V, I_F = 0A$	-	60	-	-	60	-	-	60	-	pF
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

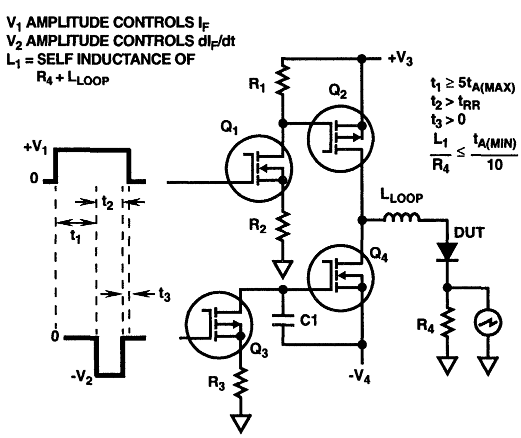


FIGURE 1. t_{RR} TEST CIRCUIT

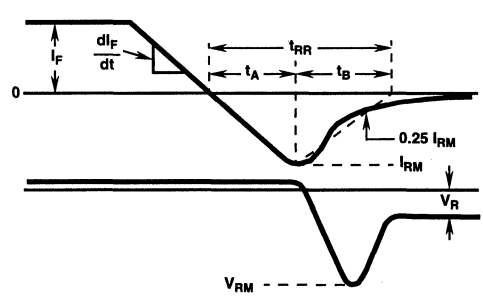


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

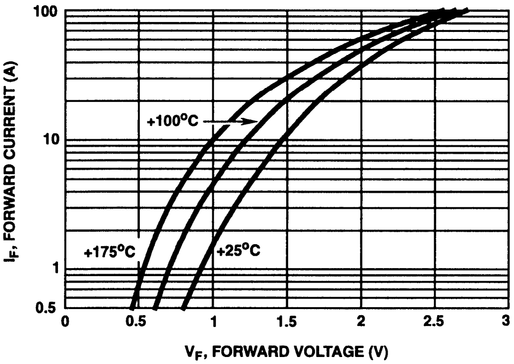


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

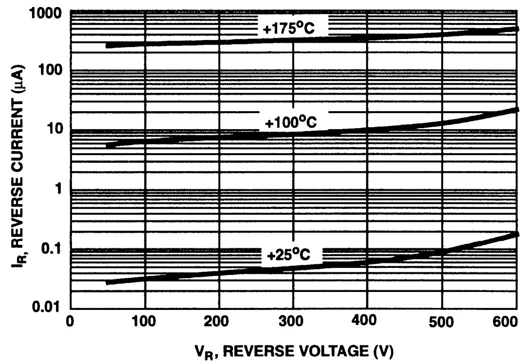


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

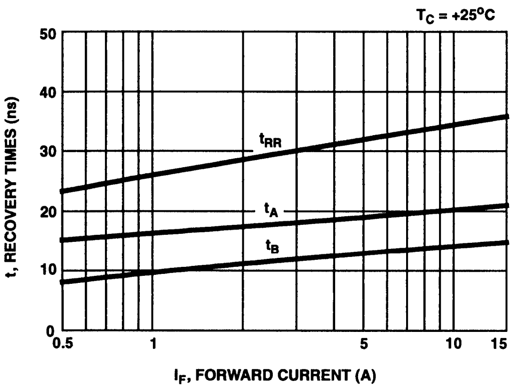


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

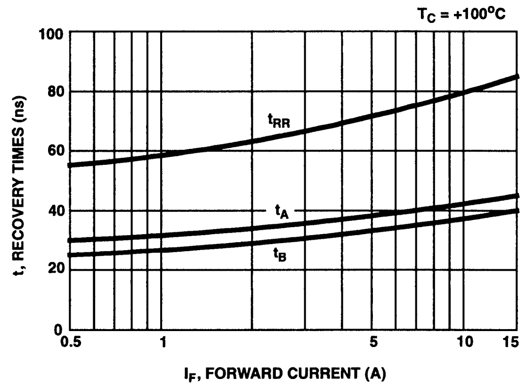


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

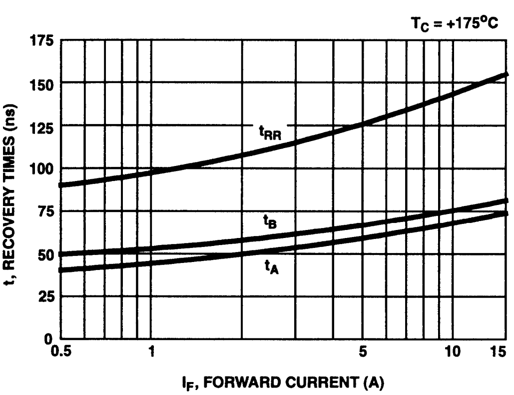


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

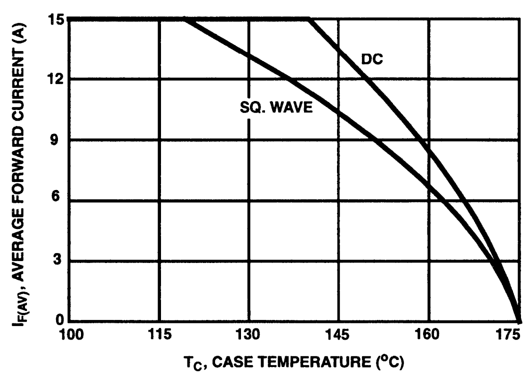


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

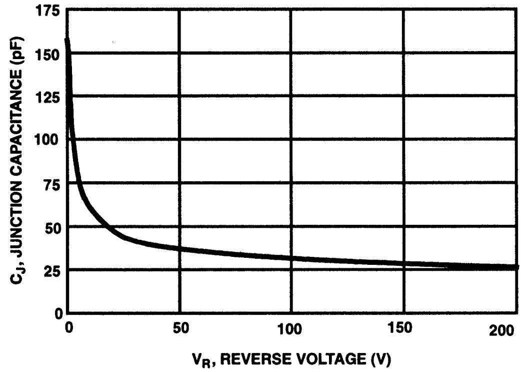


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

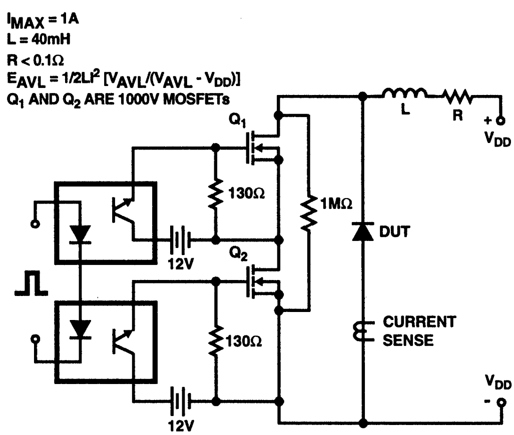


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

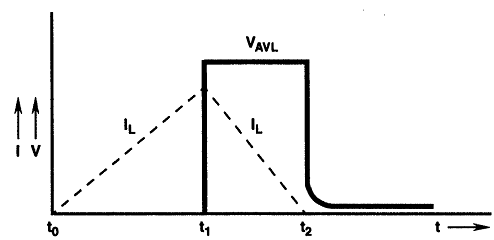


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG1570CC, RHRG1580CC, RHRG1590CC, RHRG15100CC

April 1995

15A, 700V - 1000V Hyperfast Dual Diodes

Features

- Hyperfast with Soft Recovery . . . . < 60ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG1570CC, RHRG1580CC, RHRG1590CC and RHRG15100CC (TA49062) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 60ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

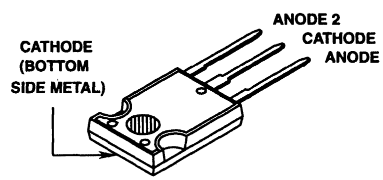
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG1570CC	TO-247	RHRG1570C
RHRG1580CC	TO-247	RHRG1580C
RHRG1590CC	TO-247	RHRG1590C
RHRG15100CC	TO-247	RHR15100C

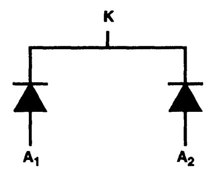
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings (Per Leg) T_C = +25°C, Unless Otherwise Specified

		RHRG1570CC	RHRG1580CC	RHRG1590CC	RHRG15100CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +130°C)	$I_{F(AV)}$	15	15	15	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	30	30	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 phase, 60Hz)	I_{FSM}	200	200	200	200	A
Maximum Power Dissipation	P_D	100	100	100	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3693.1**

Electrical Specifications (Per Leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG1570CC			RHRG1580CC			RHRG1590CC			RHRG15100CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 15A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 15A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	100	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	100	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C	-	-	-	-	-	-	-	-	100	-	-	-	μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	100	μA
I_R	V_R = 700V, T_C = +150°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +150°C	-	-	-	-	-	-	-	-	500	-	-	-	μA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	60	-	-	60	-	-	60	-	-	60	ns
	I_F = 15A, dI_F/dt = 100A/μs	-	-	70	-	-	70	-	-	70	-	-	70	ns
t_A	I_F = 15A, dI_F/dt = 100A/μs	-	40	-	-	40	-	-	40	-	-	40	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/μs	-	25	-	-	25	-	-	25	-	-	25	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/μs	-	160	-	-	160	-	-	160	-	-	160	-	nC
C_J	V_R = 10V, I_F = 0A	-	66	-	-	66	-	-	66	-	-	66	-	pF
$R_{\theta JC}$		-	-	1.5	-	-	1.5	-	-	1.5	-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

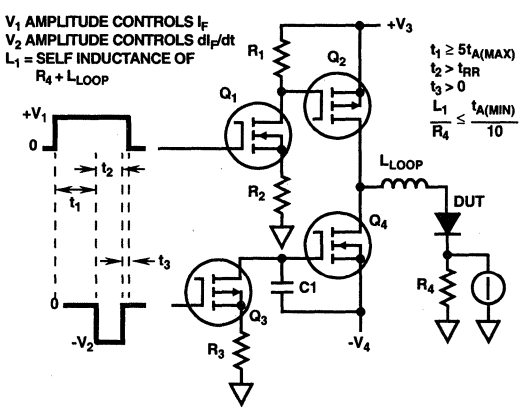


FIGURE 1. t_{RR} TEST CIRCUIT

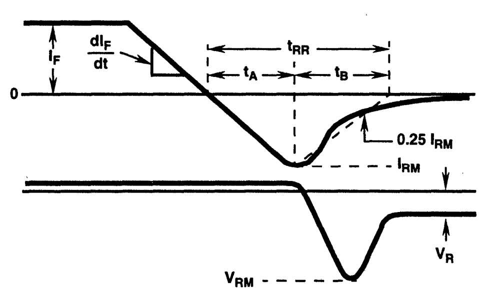


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

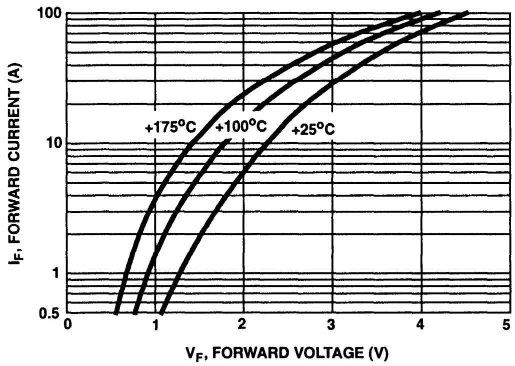


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

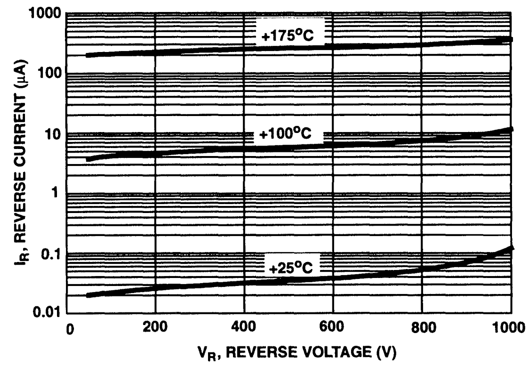


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

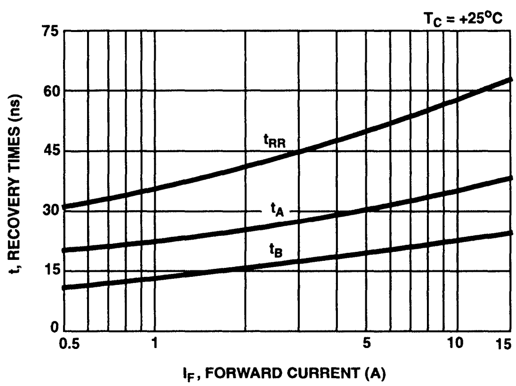


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 25°C

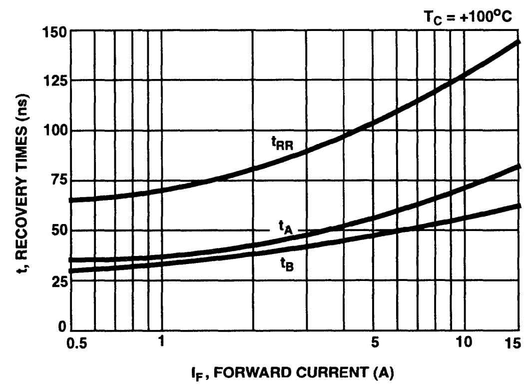


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 100°C

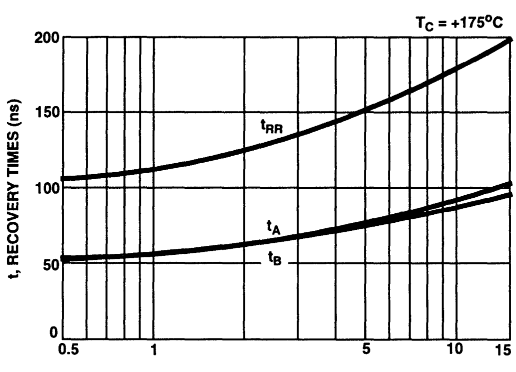


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT 175°C

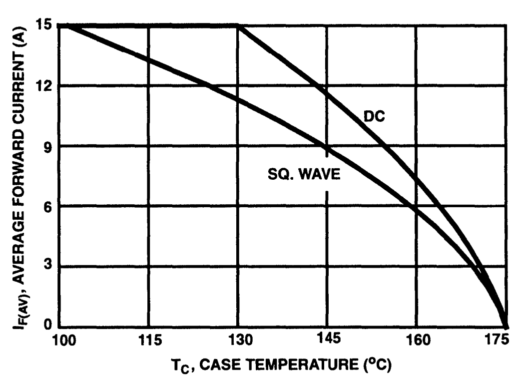


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

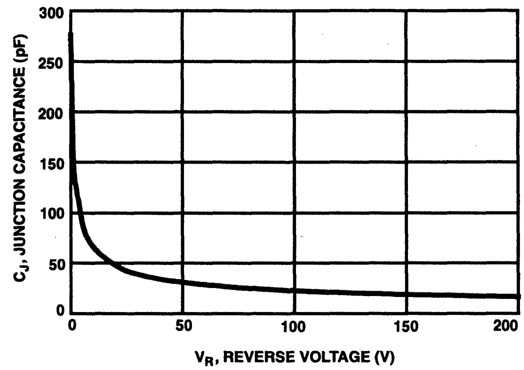


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

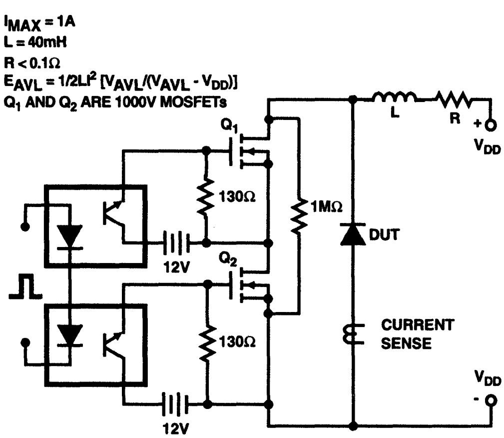


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

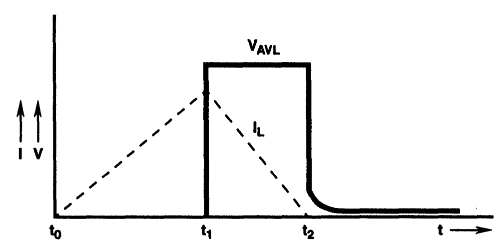


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG15120CC

April 1995

15A, 1200V Hyperfast Dual Diode

Features

- Hyperfast with Soft Recovery . . . . < 65ns
- Operating Temperature . . . . +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRG15120CC (TA49098) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 65ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

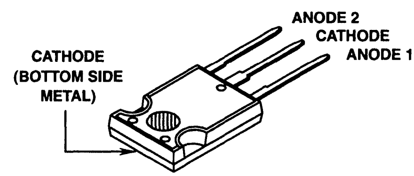
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG15120CC	TO-247	RHR15120C

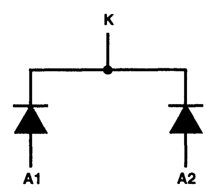
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings (Per Leg) T_C = +25°C, Unless Otherwise Specified

		RHRG15120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (T_C = 130°C)	$I_{F(AV)}$	15	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	30	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	200	A
Maximum Power Dissipation	P_D	100	W
Avalanche Energy (L = 40mH)	E_{AVL}	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	°C

File Number **3686.1**

Electrical Specifications (Per Leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG15120CC LIMITS MIN	TYP	MAX	UNITS
V_F	I_F = 15A, T_C = +25°C	-	-	3.2	V
	I_F = 15A, T_C = +150°C	-	-	2.6	V
I_R	V_R = 1200V, T_C = +25°C	-	-	100	μA
	V_R = 1200V, T_C = +150°C	-	-	500	μA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	65	ns
	I_F = 15A, dI_F/dt = 100A/μs	-	-	75	ns
t_A	I_F = 15A, dI_F/dt = 100A/μs	-	36	-	ns
t_B	I_F = 15A, dI_F/dt = 100A/μs	-	28	-	ns
Q_{RR}	I_F = 15A, dI_F/dt = 100A/μs	-	150	-	nC
C_J	V_R = 10V, I_F = 0A	-	55	-	pF
$R_{\theta JC}$		-	-	1.5	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

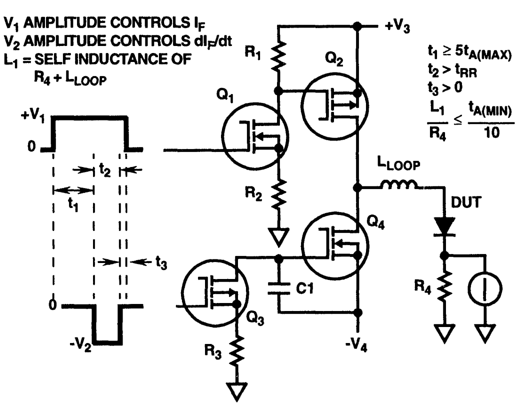


FIGURE 1. t_{RR} TEST CIRCUIT

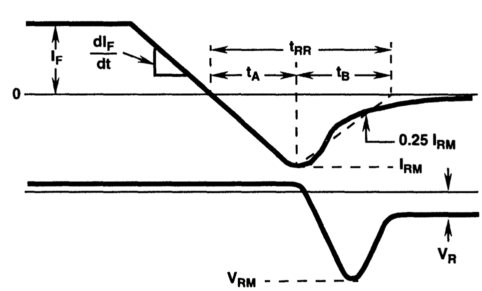


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

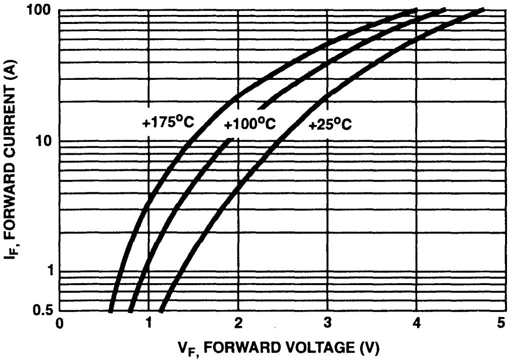


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

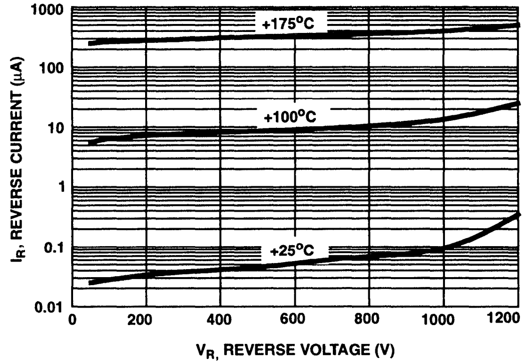


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

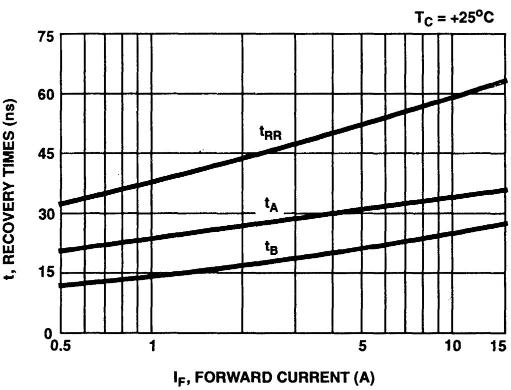


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

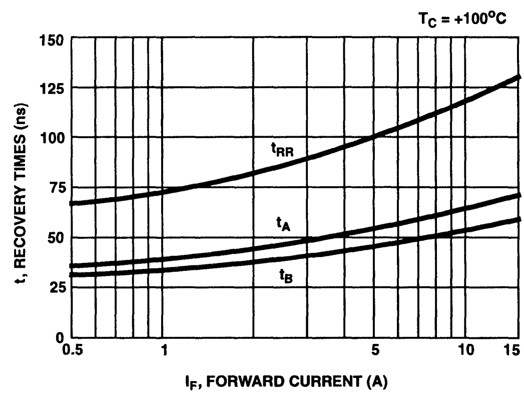


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

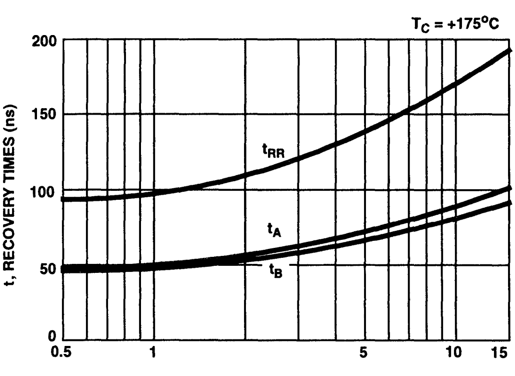


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

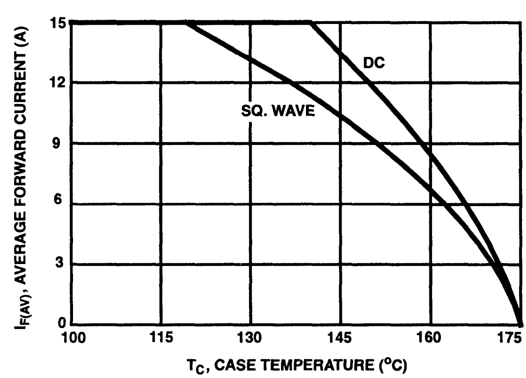


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

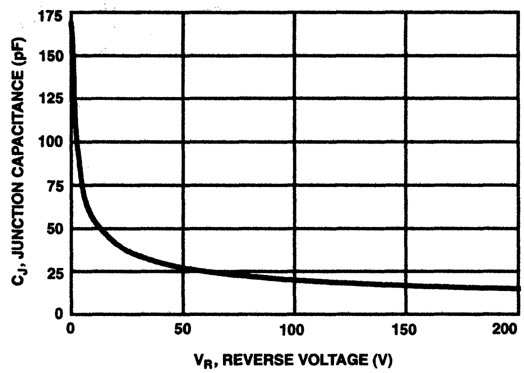


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuit and Waveforms

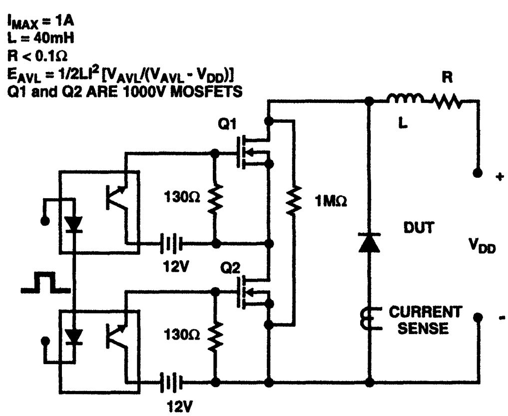


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

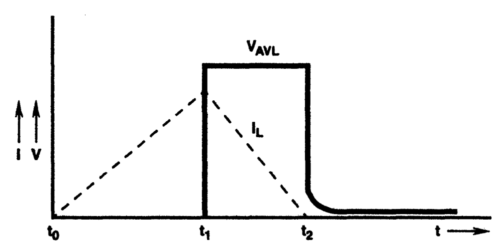


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG3040CC, RHRG3050CC, RHRG3060CC

April 1995

30A, 400V - 600V Hyperfast Dual Diodes

Features

- **Hyperfast with Soft Recovery . . . . <40ns**
- **Operating Temperature . . . . +175°C**
- **Reverse Voltage Up To 600V**
- **Avalanche Energy Rated**
- **Planar Construction**

Applications

- **Switching Power Supplies**
- **Power Switching Circuits**
- **General Purpose**

Description

RHRG3040CC, RHRG3050CC and RHRG3060CC are hyperfast diodes with soft recovery characteristics (t_{RR} < 40ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

PACKAGING AVAILABILITY

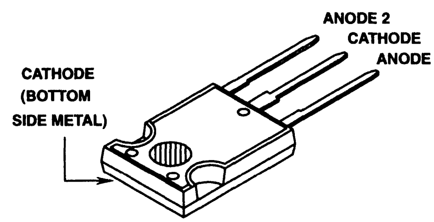
PART NUMBER	PACKAGE	BRAND
RHRG3040CC	TO-247	RHRG3040C
RHRG3050CC	TO-247	RHRG3050C
RHRG3060CC	TO-247	RHRG3060C

NOTE: When ordering, use the entire part number.

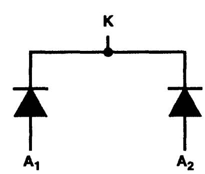
Formerly developmental type TA49063.

Package

JEDEC STYLE TO-247



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RHRG3040CC	RHRG3050CC	RHRG3060CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	400	500	600	V
Working Peak Reverse Voltage	V_{RWM}	400	500	600	V
DC Blocking Voltage	V_R	400	500	600	V
Average Rectified Forward Current (T_C = +120°C)	$I_{F(AV)}$	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3939.2**

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG3040CC			RHRG3050CC			RHRG3060CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	2.1	-	-	2.1	-	-	2.1	V
	I_F = 30A, T_C = +150°C	-	-	1.7	-	-	1.7	-	-	1.7	V
I_R	V_R = 400V, T_C = +25°C	-	-	500	-	-	-	-	-	-	µA
	V_R = 500V, T_C = +25°C	-	-	-	-	-	500	-	-	-	µA
	V_R = 600V, T_C = +25°C	-	-	-	-	-	-	-	-	500	µA
I_R	V_R = 400V, T_C = +150°C	-	-	1.0	-	-	-	-	-	-	mA
	V_R = 500V, T_C = +150°C	-	-	-	-	-	1.0	-	-	-	mA
	V_R = 600V, T_C = +150°C	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 200A/µs	-	-	40	-	-	40	-	-	40	ns
	I_F = 30A, dI_F/dt = 200A/µs	-	-	45	-	-	45	-	-	45	ns
t_A	I_F = 30A, dI_F/dt = 200A/µs	-	22	-	-	22	-	-	22	-	ns
t_B	I_F = 30A, dI_F/dt = 200A/µs	-	18	-	-	18	-	-	18	-	ns
Q_{RR}	I_F = 30A, dI_F/dt = 200A/µs	-	100	-	-	100	-	-	100	-	nC
C_J	V_R = 10V, I_F = 0A	-	85	-	-	85	-	-	85	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
Q_{RR} = Reverse recovery charge.
C_J = Junction Capacitance.
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).
pw = pulse width.
D = duty cycle.

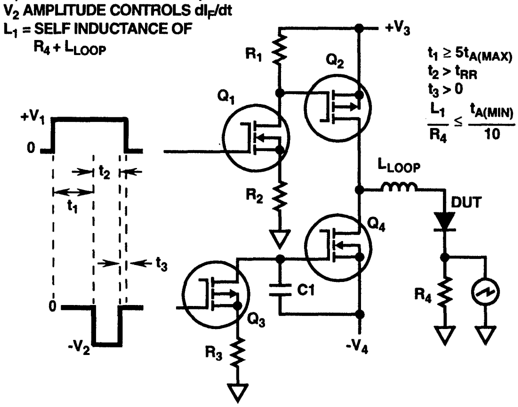


FIGURE 1. t_{RR} TEST CIRCUIT

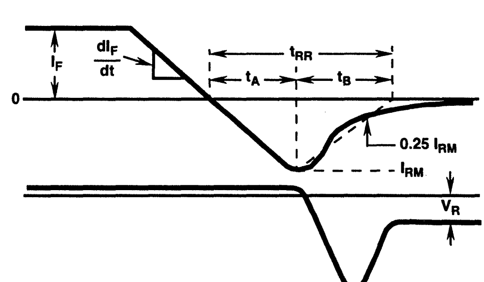


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

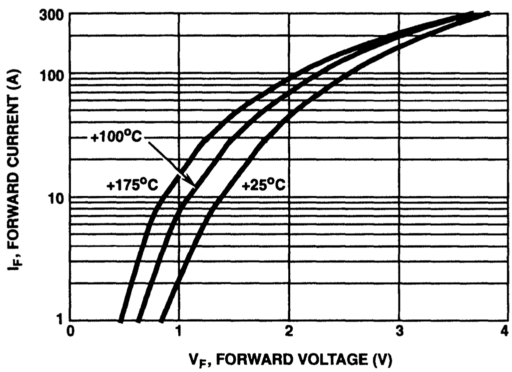


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

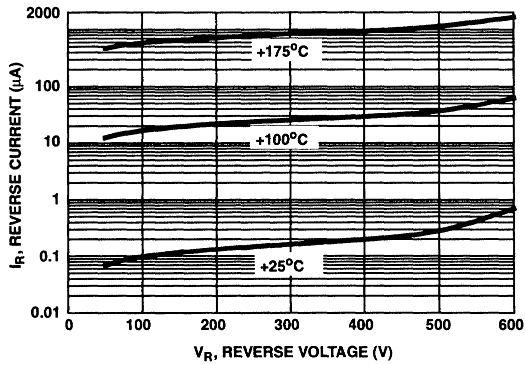


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

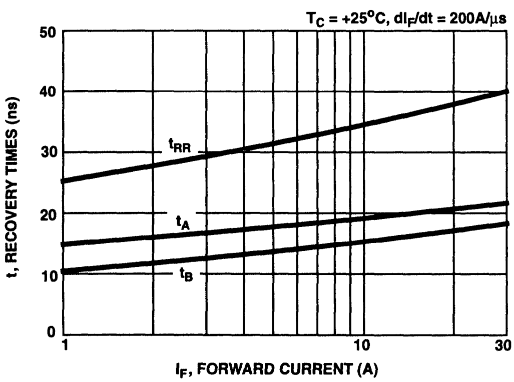


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

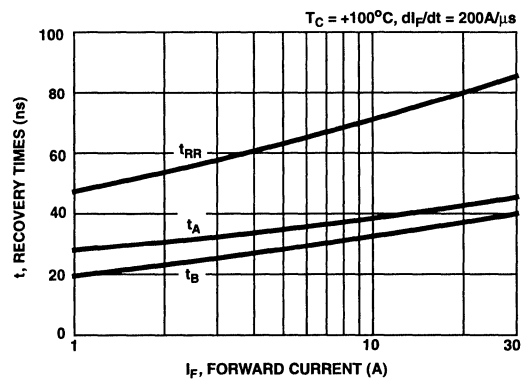


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

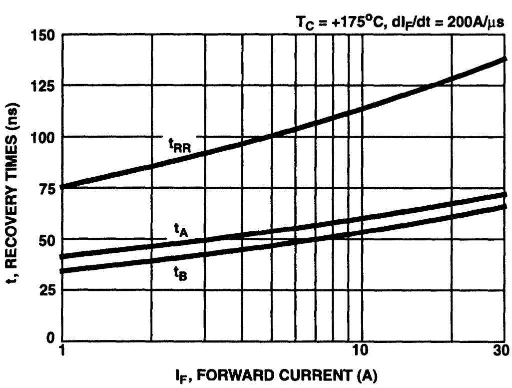


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

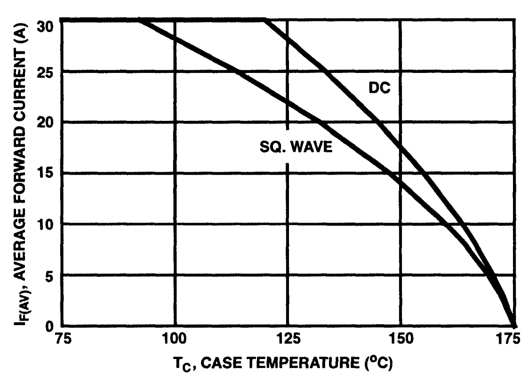


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

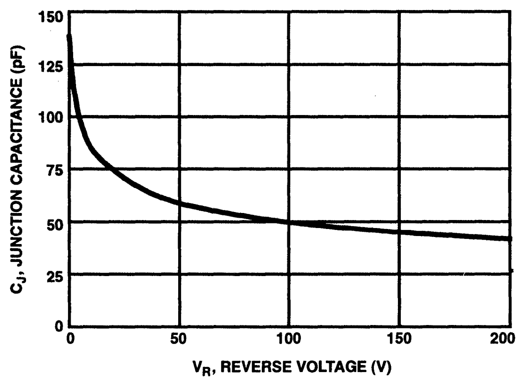


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

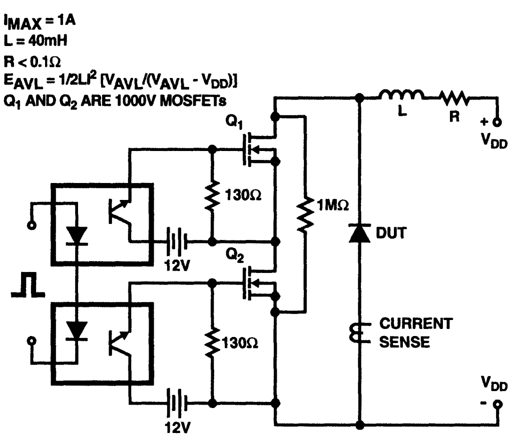


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

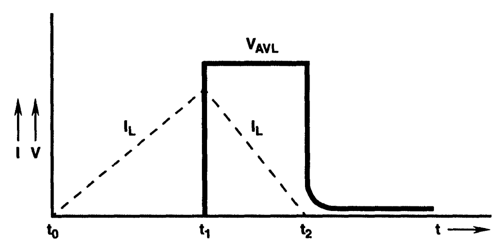


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG3070CC, RHRG3080CC, RHRG3090CC, RHRG30100CC

April 1995

30A, 700V - 1000V Hyperfast Dual Diodes

Features

- Hyperfast with Soft Recovery . . . . <65ns
- Operating Temperature . . . . +175°C
- Reverse Voltage Up To 1000V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

RHRG3070CC, RHRG3080CC, RHRG3090CC, and RHRG30100CC (TA49064) are hyperfast dual diodes with soft recovery characteristics (t_{RR} < 65ns). They have half the recovery time of ultrafast diodes and are silicon nitride passivated ion-implanted epitaxial planar construction.

These devices are intended for use as freewheeling/clamping diodes and rectifiers in a variety of switching power supplies and other power switching applications. Their low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits reducing power loss in the switching transistors.

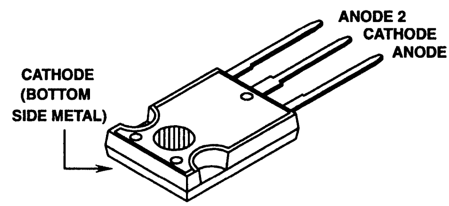
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG3070CC	TO-247	RHRG3070C
RHRG3080CC	TO-247	RHRG3080C
RHRG3090CC	TO-247	RHRG3090C
RHRG30100CC	TO-247	RHR30100C

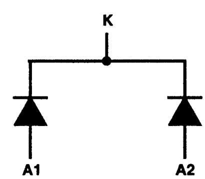
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings (per leg) T_C = +25°C, Unless Otherwise Specified

		RHRG3070CC	RHRG3080CC	RHRG3090CC	RHRG30100CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	700	800	900	1000	V
Working Peak Reverse Voltage	V_{RWM}	700	800	900	1000	V
DC Blocking Voltage	V_R	700	800	900	1000	V
Average Rectified Forward Current (T_C = +95°C)	$I_{F(AV)}$	30	30	30	30	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FSM}	70	70	70	70	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	325	325	325	325	A
Maximum Power Dissipation	P_D	125	125	125	125	W
Avalanche Energy (see Figures 10 and 11)	E_{AVL}	20	20	20	20	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	-65 to +175	-65 to +175	-65 to +175	°C

File Number **3942.1**

Electrical Specifications (per leg) T_C = +25°C, Unless Otherwise Specified

SYMBOL	TEST CONDITION	RHRG3070CC			RHRG3080CC			RHRG3090CC			RHRG30100CC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_F	I_F = 30A, T_C = +25°C	-	-	3.0	-	-	3.0	-	-	3.0	-	-	3.0	V
	I_F = 30A, T_C = +150°C	-	-	2.5	-	-	2.5	-	-	2.5	-	-	2.5	V
I_R	V_R = 700V, T_C = +25°C	-	-	500	-	-	-	-	-	-	-	-	-	μA
	V_R = 800V, T_C = +25°C	-	-	-	-	-	500	-	-	-	-	-	-	μA
	V_R = 900V, T_C = +25°C							-	-	500				μA
	V_R = 1000V, T_C = +25°C	-	-	-	-	-	-	-	-	-	-	-	500	μA
I_R	V_R = 700V, T_C = +150°C	-	-	1.0	-	-	-	-	-	-	-	-	-	mA
	V_R = 800V, T_C = +150°C	-	-	-	-	-	1.0	-	-	-	-	-	-	mA
	V_R = 900V, T_C = +150°C							-	-	1.0				mA
	V_R = 1000V, T_C = +150°C	-	-	-	-	-	-	-	-	-	-	-	1.0	mA
t_{RR}	I_F = 1A, dI_F/dt = 100A/μs	-	-	65	-	-	65	-	-	65	-	-	65	ns
	I_F = 30A, dI_F/dt = 100A/μs	-	-	75	-	-	75	-	-	75	-	-	75	ns
t_A	I_F = 30A, dI_F/dt = 100A/μs	-	35	-	-	35	-	-	35	-	-	35	-	ns
t_B	I_F = 30A, dI_F/dt = 100A/μs	-	33	-	-	33	-	-	33	-	-	33	-	ns
Q_{RR}	I_F = 30A, dI_F/dt = 100A/μs	-	200	-	-	200	-	-	200	-	-	200	-	nC
C_J	V_R = 10V, I_F = 0A	-	100	-	-	100	-	-	100	-	-	100	-	pF
$R_{\theta JC}$		-	-	1.2	-	-	1.2			1.2	-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{RR} = Reverse recovery time (Figure 2), summation of $t_A + t_B$.

t_A = Time to reach peak reverse current (See Figure 2).

t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (see Figure 2).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

E_{AVL} = Controlled avalanche energy. (See Figures 10 and 11).

pw = pulse width.

D = duty cycle.

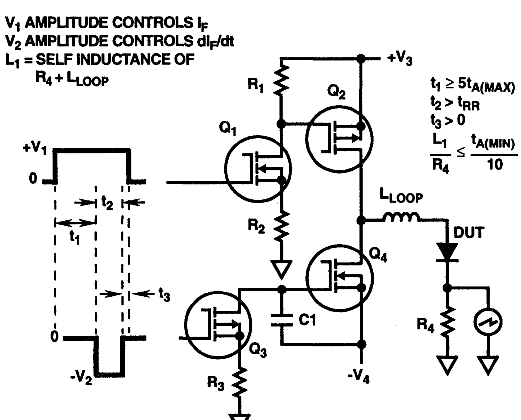


FIGURE 1. t_{RR} TEST CIRCUIT

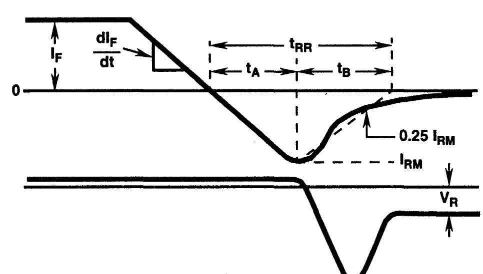


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

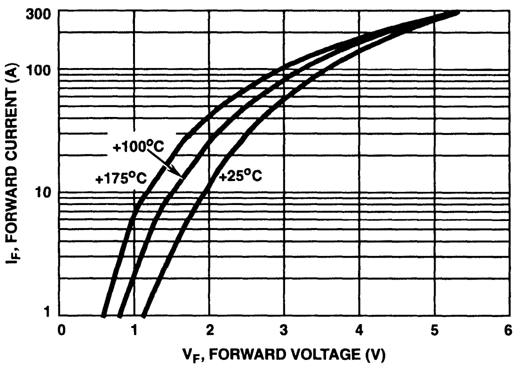


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

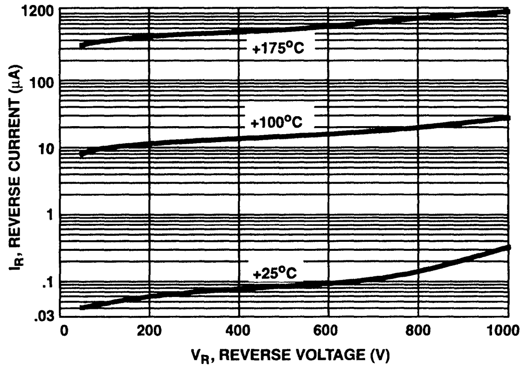


FIGURE 4. TYPICAL REVERSE CURRENT vs REVERSE VOLTAGE

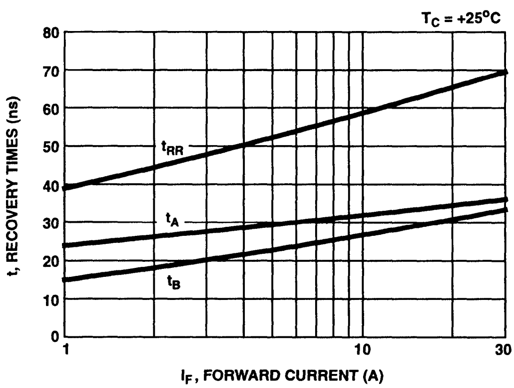


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +25°C

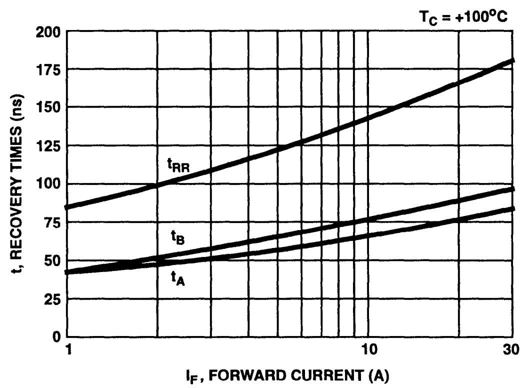


FIGURE 6. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +100°C

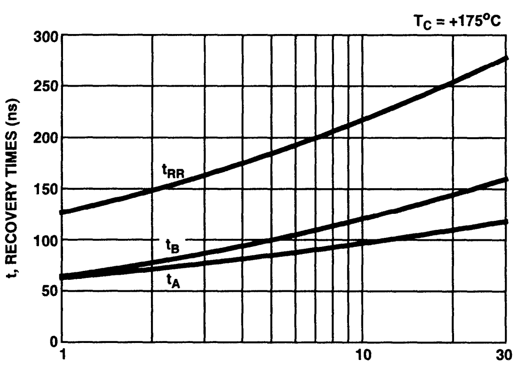


FIGURE 7. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT AT +175°C

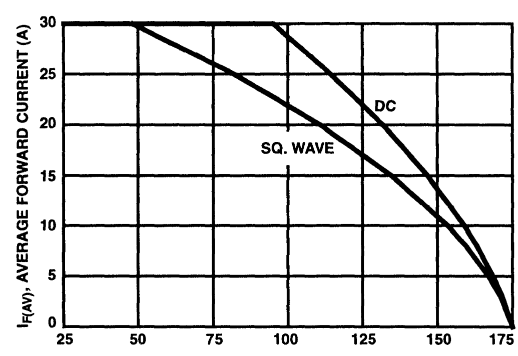


FIGURE 8. CURRENT DERATING CURVE FOR ALL TYPES

Typical Performance Curves (Continued)

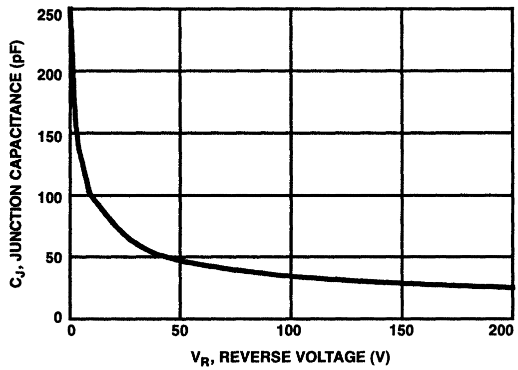


FIGURE 9. TYPICAL JUNCTION CAPACITANCE vs REVERSE VOLTAGE

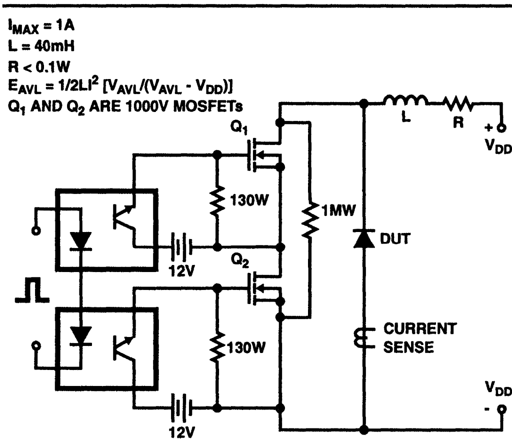


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

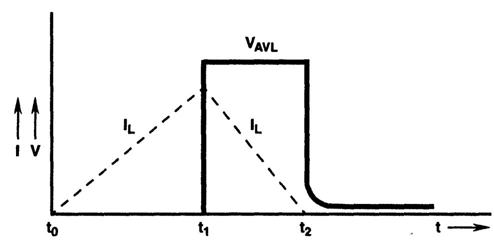


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

RHRG30120CC

April 1995

30A, 1200V Hyperfast Dual Diode

Features

- Hyperfast with Soft Recovery .... <65ns
- Operating Temperature .... +175°C
- Reverse Voltage 1200V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Description

The RHRG30120CC (TA49041) is a hyperfast dual diode with soft recovery characteristics (t_{RR} < 65ns). It has half the recovery time of ultrafast diodes and is silicon nitride passivated ion-implanted epitaxial planar construction.

This device is intended for use as a freewheeling/clamping diode and rectifier in a variety of high frequency switching power supplies and other power switching applications. Its low stored charge and hyperfast soft recovery minimize ringing and electrical noise in many power switching circuits, reducing power loss in the switching transistors.

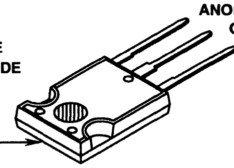
PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RHRG30120CC	TO-247	RHR30120C

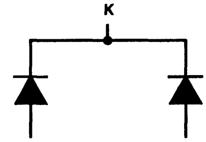
NOTE: When ordering, use the entire part number.

Package

JEDEC STYLE TO-247



Symbol



8

HYPERFAST DUAL DIODES

Absolute Maximum Ratings $T_C = +25^oC$

		RHRG30120CC	UNITS
Peak Repetitive Reverse Voltage	V_{RRM}	1200	V
Working Peak Reverse Voltage	V_{RWM}	1200	V
DC Blocking Voltage	V_R	1200	V
Average Rectified Forward Current (Per Leg) ($T_C = +78^oC$)	$I_{F(AV)}$	30	V
Repetitive Peak Surge Current (Per Leg) (Square Wave, 20kHz)	I_{FSM}	60	V
Nonrepetitive Peak Surge Current (Per Leg) (Halfwave, 1 Phase, 60Hz)	I_{FSM}	300	V
Maximum Power Dissipation	P_D	125	W
Avalanche Energy (L = 40mH)	E_{AVL}	30	mj
Operating and Storage Temperature	T_{STG}, T_J	-65 to +175	^oC

File Number **3411.2**

Electrical Specifications (Per Leg) $T_C = +25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION		LIMITS MIN	TYP	MAX	UNITS
V_F	$I_F = 30A$		-	-	3.2	V
V_F	$I_F = 30A$	$T_C = +150^oC$	-	-	2.6	V
I_R	$V_R = 1200V$		-	-	500	µA
I_R	$V_R = 1200V$	$T_C = +150^oC$	-	-	1	mA
t_{RR}	$I_F = 1A$, $dI_F/dt = 100A/\mu s$		-	-	65	ns
t_{RR}	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	-	75	ns
t_A	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	48	-	ns
t_B	$I_F = 30A$, $dI_F/dt = 100A/\mu s$		-	22	-	ns
$R_{\theta JC}$			-	-	1.2	°C/W

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300µs, D = 2%).
I_R = Instantaneous reverse current.
t_{RR} = Reverse recovery time (See Figure 2), summation of $t_A + t_B$.
t_A = Time to reach peak reverse current (See Figure 2).
t_B = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 2).
$R_{\theta JC}$ = Thermal resistance junction to case.
E_{AVL} = Controlled avalanche energy (See Figures 7 and 8).
pw = pulse width.
D = duty cycle.

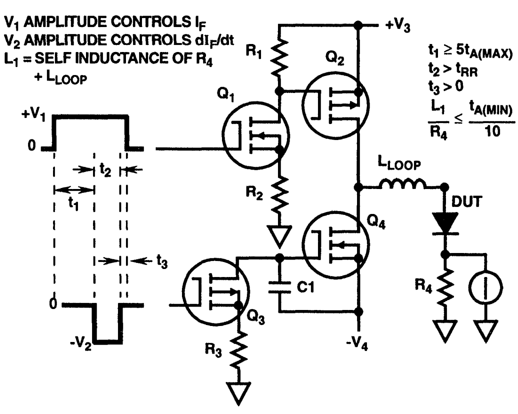


FIGURE 1. t_{RR} TEST CIRCUIT

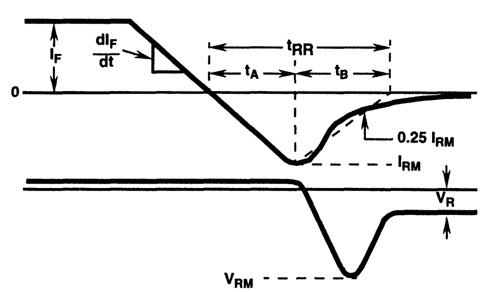


FIGURE 2. t_{RR} WAVEFORMS AND DEFINITIONS

Typical Performance Curves

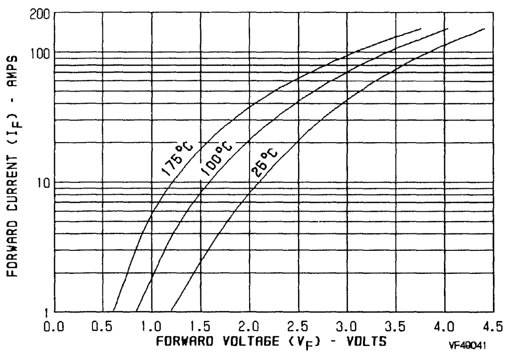


FIGURE 3. TYPICAL FORWARD CURRENT vs FORWARD VOLTAGE DROP

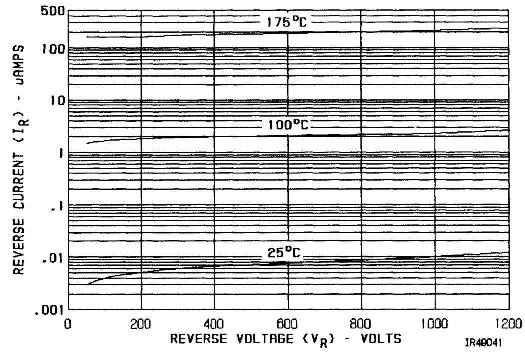


FIGURE 4. TYPICAL REVERSE CURRENT vs VOLTAGE

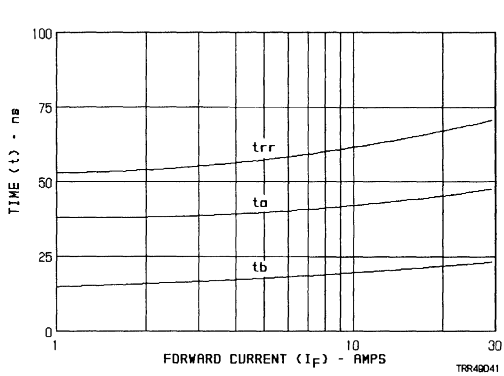


FIGURE 5. TYPICAL t_{RR}, t_A AND t_B CURVES vs FORWARD CURRENT

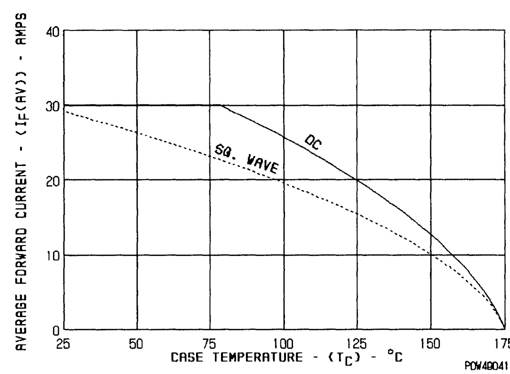


FIGURE 6. CURRENT DERATING CURVE FOR ALL TYPES

$I_{MAX} = 1A$
$L = 40mH$
$R < 0.1\Omega$
$E_{AVL} = 1/2LI^2 [V_{AVL}/(V_{AVL} - V_{DD})]$
Q_1 & Q_2 ARE 1000V MOSFETs

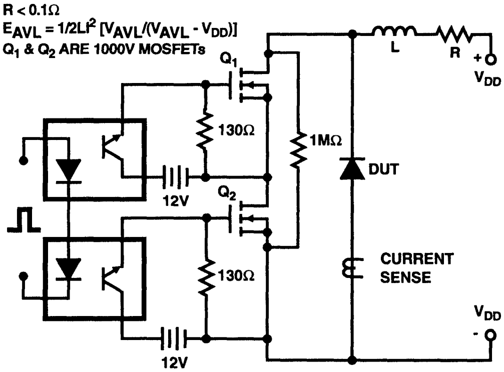


FIGURE 7. AVALANCHE ENERGY TEST CIRCUIT

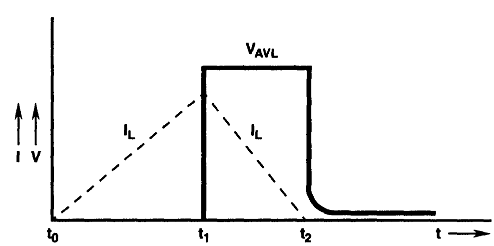


FIGURE 8. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

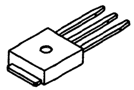
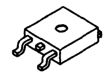
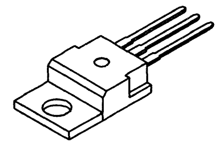
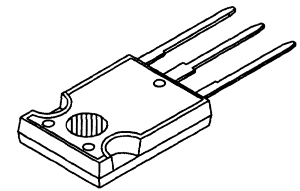
8

HYPERFAST DUAL DIODES

MCT/IGBT/DIODES 9

PREVIEW PRODUCTS

HARRIS GENERATION III ULTRA-FAST SWITCHING "UFS" IGBT FUTURE PRODUCTS

	 TO-251AA	 TO-252AA	 TO-220AB	 TO-247
600V	HGTD5N60B3 HGTD7N60B3	HGTD5N60B3S HGTD7N60B3S	HGTP12N60B3	HGTG30N60B3 HGTG40N60B3
1200V	HGTD4N120B3 HGTD6N120B3	HGTD4N120B3S HGTD6N120B3S	HGTP10N120B3 HGTP15N120B3	HGTG20N120B3 HGTG30N120B3
PRODUCTS WITH HYPERFAST ANTI-PARALLEL DIODES				
600V	HGTD5N60B3D	HGTD5N60B3DS	HGTP7N60B3D HGTP12N60B3D	HGTG30N60B3D
1200V	HGTD4N120B3D	HGTD4N120B3DS	HGTP6N120B3D HGP10N120B3D	HGTG15N120B3D HGTG20N120B3D HGTG30N120B3D

NOTES::

1. Collector current rating at $T_C = 110^oC$.
2. Values for collector current may vary when final characterization is completed.
3. Collector current rating at 25^oC can assumed to be 2 x $T_C = 110^oC$ rating.

HARRIS SEMICONDUCTOR

HGTG40N60B3

PRELIMINARY

May 1995

70A, 600V, UFS Series N-Channel IGBT

Features

- 70A, 600V at $T_C = +25^oC$
- Square Switching SOA Capability
- Typical Fall Time - 160ns at +150°C
- Short Circuit Rating
- Low Conduction Loss

Description

The HGTG40N60B3 is a MOS gated high voltage switching device combining the best features of MOSFETs and bipolar transistors. The device has the high input impedance of a MOSFET and the low on-state conduction loss of a bipolar transistor. The much lower on-state voltage drop varies only moderately between +25°C and +150°C.

The IGBT is ideal for many high voltage switching applications operating at moderate frequencies where low conduction losses are essential, such as: AC and DC motor controls, power supplies and drivers for solenoids, relays and contactors.

PACKAGING AVAILABILITY

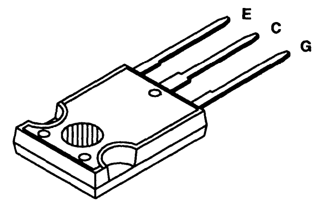
PART NUMBER	PACKAGE	BRAND
HGTG40N60B3	TO-247	G40N60B3

NOTE: When ordering, use the entire part number.

Formerly Developmental Type TA49052

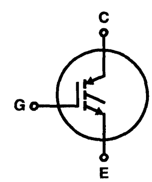
Package

JEDEC STYLE TO-247



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		HGTG40N60B3	UNITS
Collector-Emitter Voltage	BV_{CES}	600	V
Collector-Gate Voltage, $R_{GE} = 1M\Omega$	BV_{CGR}	600	V
Collector Current Continuous			
At $T_C = +25^oC$ (Package Limited)	I_{C25}	70	A
At $T_C = +110^oC$	I_{C110}	40	A
Collector Current Pulsed (Note 1)	I_{CM}	330	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching Safe Operating Area at $T_C = +150^oC$	SSOA	160A at 0.8 BV_{CES}	
Power Dissipation Total at $T_C = +25^oC$	P_D	290	W
Power Dissipation Derating $T_C > +25^oC$		2.33	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-40 to +150	°C
Maximum Lead Temperature for Soldering	T_L	260	°C
Short Circuit Withstand Time (Note 2) at $V_{GE} = 15V$	t_{SC}	2	µs
Short Circuit Withstand Time (Note 2) at $V_{GE} = 10V$	t_{SC}	10	µs

NOTE:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $V_{CE(PK)} = 360V$, $T_C = +125^oC$, $R_{GE} = 25\Omega$.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3943**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
				MIN	TYP	MAX	
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_{CE} = 250\mu A$, $V_{GE} = 0V$		600	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_J = +25^oC$	-	-	250	A
		$V_{CE} = BV_{CES}$	$T_J = +150^oC$	-	-	7.5	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{CE} = 40A$ $V_{GE} = 15V$	$T_J = +25^oC$	-	1.4	2.0	V
			$T_J = +150^oC$	-	1.5	2.3	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	$I_{CE} = 250A$, $V_{CE} = V_{GE}$	$T_J = +25^oC$	3.0	5	6.0	V
Gate-Emitter Leakage Current	I_{GES}	$V_{GE} = \pm 20V$		-	-	±300	nA
Latching Current	I_L	$T_J = +150^oC$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 3\Omega$ $L = 45\mu H$		160	-	-	A
Gate-Emitter Plateau Voltage	V_{GEP}	$I_{CE} = 40A$, $V_{CE} = 0.5\ BV_{CES}$		-	8.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	$I_{CE} = 40A$, $V_{CE} = 0.5\ BV_{CES}$	$V_{GE} = 15V$	-	240	320	nC
			$V_{GE} = 20V$	-	350	450	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	$T_J = +150^oC$ $I_{CE} = 40A$ $V_{CE(PK)} = 0.8\ BV_{CES}$ $V_{GE} = 15V$ $R_G = 3\Omega$ $L = 100\mu H$		-	50	-	ns
Current Rise Time	t_{RI}			-	40	-	ns
Current Turn-Off Delay Time	$t_{D(OFF)I}$			-	350	435	ns
Current Fall Time	t_{FI}			-	160	200	ns
Turn-On Energy	E_{ON}			-	1400	-	J
Turn-Off Energy (Note 1)	E_{OFF}			-	3300	-	J
Thermal Resistance	$R_{\theta JC}$			-	-	0.43	$^oC/W$

NOTE:

1. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero ($I_{CE} = 0A$). The HGTG40N60B3 was tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

HARRIS SEMICONDUCTOR IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS:

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,567,641
4,587,713	4,598,461	4,605,948	4,618,872	4,620,211	4,631,564	4,639,754	4,639,762
4,641,162	4,644,637	4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690
4,794,432	4,801,986	4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606
4,860,080	4,883,767	4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951
4,969,027							

Typical Performance Curves

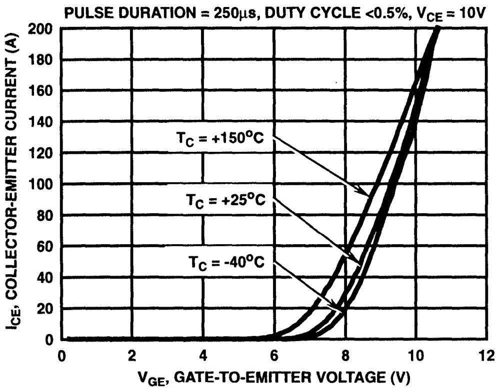


FIGURE 1. TRANSFER CHARACTERISTICS

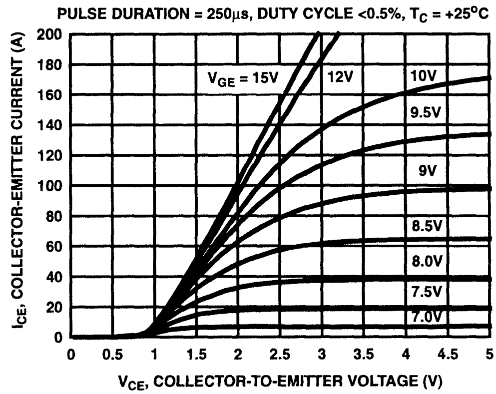


FIGURE 2. SATURATION CHARACTERISTICS

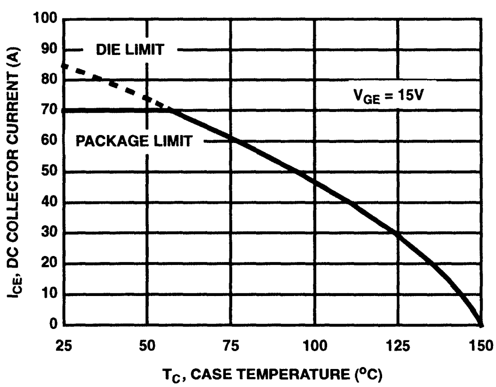


FIGURE 3. DC COLLECTOR CURRENT vs CASE TEMPERATURE

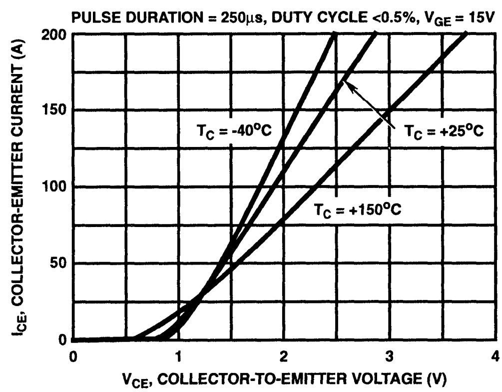


FIGURE 4. COLLECTOR-EMITTER ON-STATE VOLTAGE

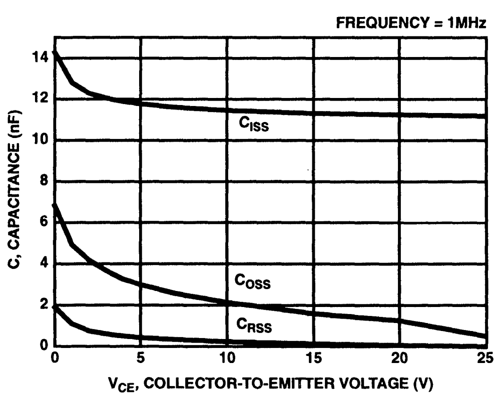


FIGURE 5. CAPACITANCE vs COLLECTOR-EMITTER VOLTAGE

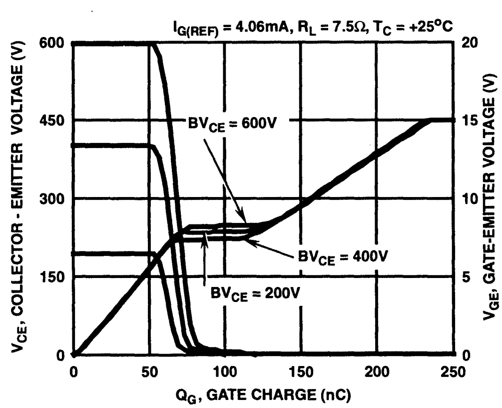


FIGURE 6. GATE CHARGE WAVEFORMS

9

PREVIEW PRODUCTS

Typical Performance Curves (Continued)

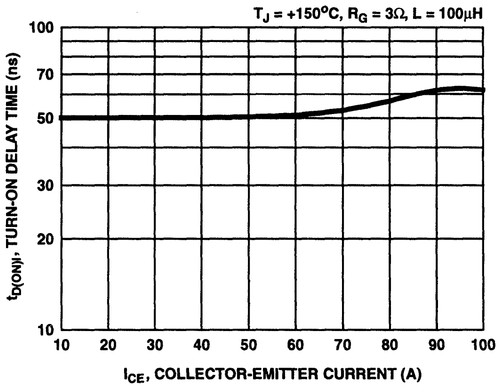


FIGURE 7. TURN-ON DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

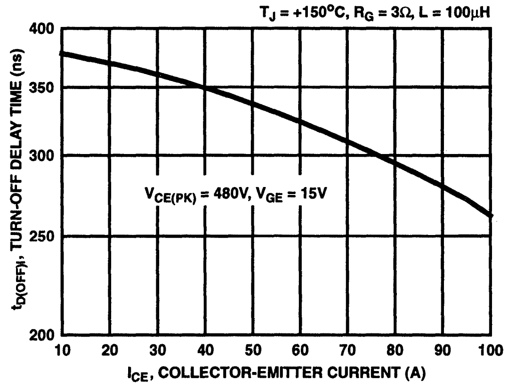


FIGURE 8. TURN-OFF DELAY TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

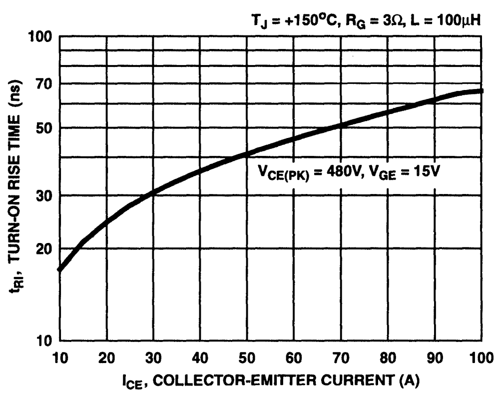


FIGURE 9. TURN-ON RISE TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

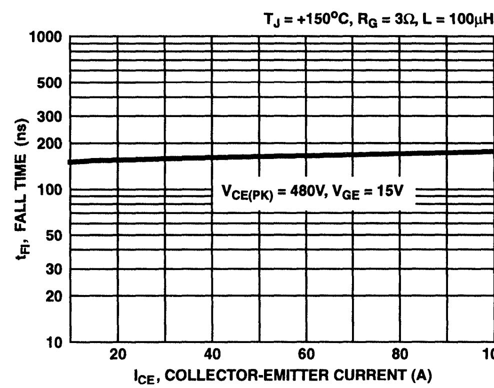


FIGURE 10. TURN-OFF FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

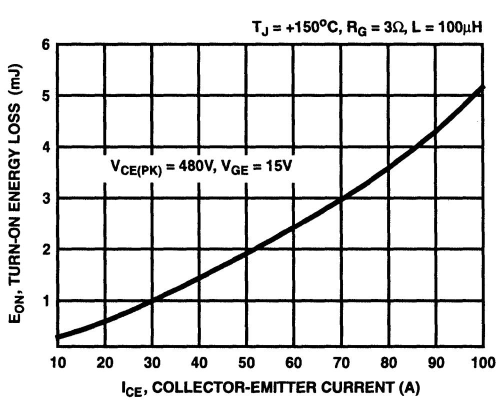


FIGURE 11. TURN-ON ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

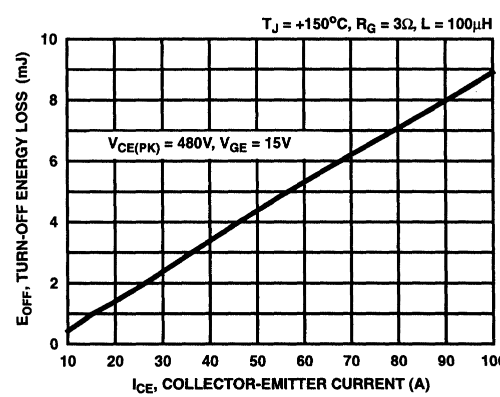


FIGURE 12. TURN-OFF ENERGY LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

Typical Performance Curves (Continued)

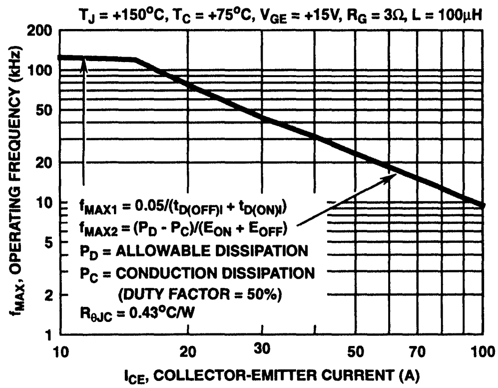


FIGURE 13. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

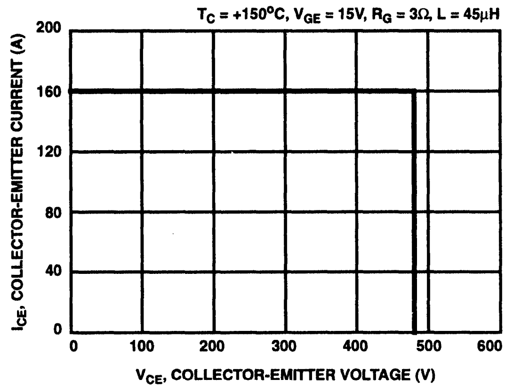


FIGURE 14. SWITCHING SAFE OPERATING AREA

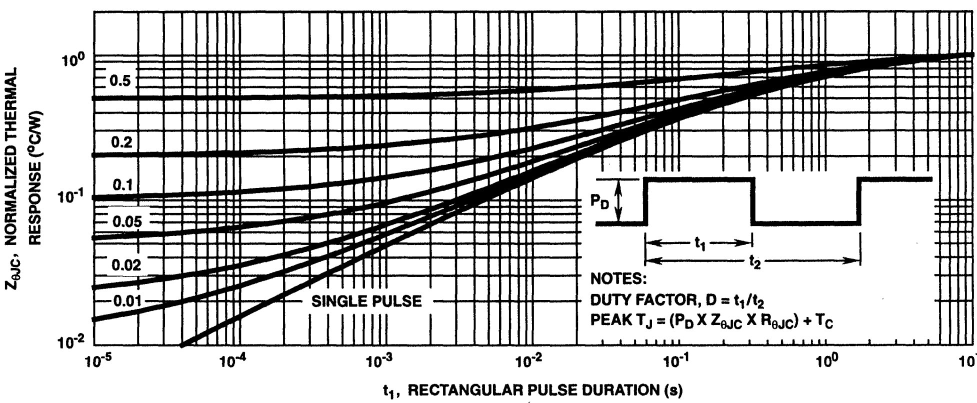


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

Test Circuit and Waveforms

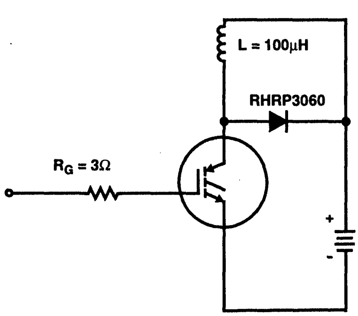


FIGURE 16. INDUCTIVE SWITCHING TEST CIRCUIT

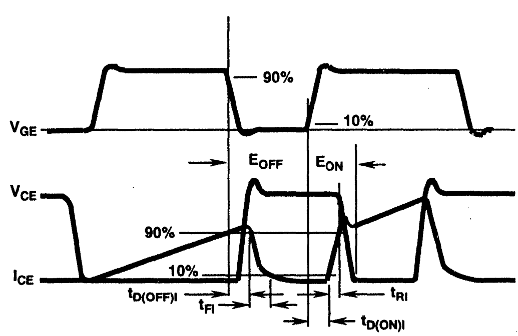


FIGURE 17. SWITCHING TEST WAVEFORMS

Operating Frequency Information

Operating frequency information for a typical device (Figure 13) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 4, 7, 8, 11 and 12. The operating frequency plot (Figure 13) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{D(OFF)I} + t_{D(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ and $t_{D(ON)I}$ are defined in Figure 17.

Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$.

The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 13) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON} and E_{OFF} are defined in the switching waveforms shown in Figure 17. E_{ON} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation of E_{OFF}; i.e.the collector current equals zero ($I_{CE} = 0$).

Handling Precautions for IGBT's

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBT's are currently being extensively used in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBT's can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as †"ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

MCT/IGBT/DIODES 10

APPLICATION NOTES

Introduction to the MCT User's Guide

Opportunities for continued progress in Power Delivery and Control Systems were never more evident than today. The efficient and elegant use of energy commands the attention of conservationists, political leaders, technologists, indeed, all those concerned with continued improvement in the human condition concurrent with respect for their world's environment. Power Electronics is an enabling technology that offers newly attractive solutions to many diverse applications of electric power. And progress in Power Electronics is paced by progress in the Semiconductor Components available as Power Switches.

A new Power Semiconductor Device, the MOS Controlled Thyristor, the MCT, is now available for commercial use. This is a significant benchmark in the progress of Power Electronics.

The MCT is a truly different product. It has its own set of characteristics. Some of these characteristics bear resemblance to the older thyristors, SCRs and GTOs. Yet the merger of modern MOS design and processing features with the older double injection bipolar structures results in a new device, with new characteristics and capabilities.

This manual is offered in the desire to facilitate the introduction of this new product. It will introduce the user to the new MCT technology. Our desire is to make available to the reader the experience of others; as it exists, and as it develops. It is our hope that the MCT will be properly applied and will be a rewarding experience for its users.

This introduction is an opportunity to recognize the contributions of Dr. Vic Temple and his associates at the Schenectady R&D Center, who are the developers of this new technology.

Research and Development support, first from the Electric Power Research Institute (EPRI) and NASA, followed by US Government Agency support through Wright Patterson AFB, DARPA, U.S. Navy (DTRC) and the U.S. Army Labcom, Electronics Technology and Devices Laboratory at Ft. Monmouth has been instrumental in MCT development. Some of these programs were co-funded by SDIO. The foresight and fortitude of the individuals who guide these agencies are to be acknowledged.

In closing, we at Harris Semiconductor wish you every success in your use of MCT's. We are committed to serve you, our customer.

HARRIS
SEMICONDUCTOR

MCT Description

2.0 *MCT's, a New Class of Power Devices*

2.0.1 Background

MOS Controlled Thyristors are a new class of power semiconductor devices that combine thyristor current and voltage capability with MOS gated turn-on and turn-off. Various subclasses of MCTs can be made: P-type or N-type, symmetric or asymmetric blocking, one or two-sided Off-FET gate control, and various turn-on alternatives including direct turn-on with light. All of these sub-classes have one thing in common; turn-off is accomplished by turning on a highly interdigitated Off-FET to short out one or both of the thyristor's emitter-base junctions. This users guide focuses on the first product introduced by Harris, a P-type asymmetric blocking, MOS gated MCT.

2.0.2 Description

Figure 2.0.1 shows the basic elements of the MCT that Harris is now producing. On the left is a representative cross section of one cell of the device that is repeated 10's of thousands of times to make a device that can turn off 120A at +150°C junction temperature. On the right is an equivalent circuit based on the well-known two transistor model of the thyristor. In the P-MCT a P-channel On-FET is turned on with a negative voltage which charges up the base of the lower transistor to latch on the MCT. The MCT turns on simultaneously over the entire device area giving the MCT excellent di/dt capability. Figure 2.0.2 compares different 600V power switching devices for 2.0.3 conduction drop.

Figure 2.0.3 shows measured device comparisons which are typical of the conduction drop advantage of the MCT. Here, a 1000V P-MCT is shown with an IGBT die similarly packaged and of the same voltage rating. Note that the MCT typically has 10 to 15 times the current at the same forward drop.

2.0.4 Turn Off

The MCT will remain in the on-state until current is reversed (like a normal thyristor) or until the Off-FET is activated by a positive gate voltage. Obviously, the higher the Off-FET gate voltage and the denser the Off-FET channels, the more current can be shorted across the emitter-base junction to effect turn-off. It is clear that successful turn-off requires all cells to turn off at the same time to prevent current from crowding. This imposes gate risetime constraints that are discussed later.

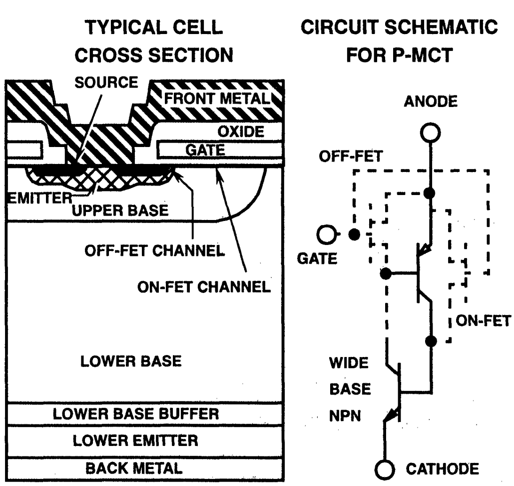


FIGURE 2.0.1 CROSSSECTION OF MCT CELL SHOWING TURN-ON AND TURN-OFF FETs

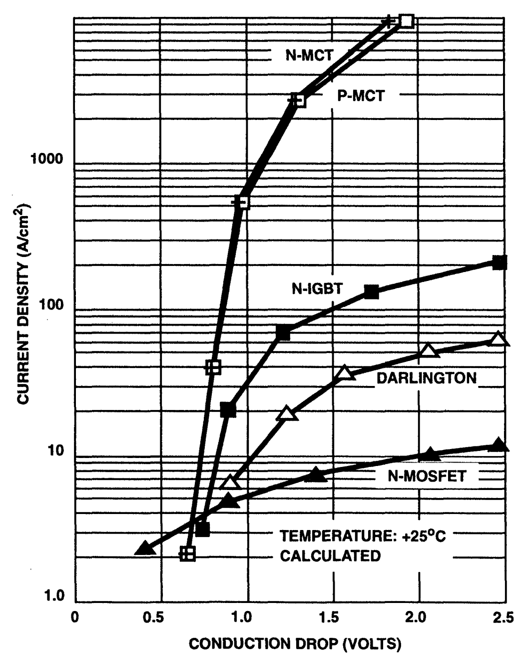


FIGURE 2.0.2 COMPARISON OF 600V DEVICES, WITH <1μs TURN-OFF TIME CAPABILITY, NEGLECTING PACKAGE RESISTANCE.

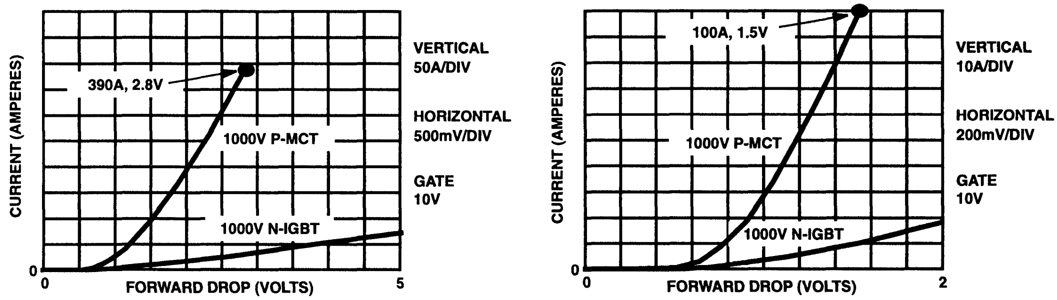


FIGURE 2.0.3 CURVE TRACER FORWARD DROP COMPARISON OF 1000V P-MCT AND N-IGBT AT +150°C

2.1 The MCT Advantages

2.1.1 Turn-On and On-State:

MCTs, are superior devices in terms of conduction drop, surge current and di/dt capability. MCTs of similar blocking voltages, thyristors or GTOs can have lower forward drop, owing to the MCTs reduced cell size (compared to the GTO) and lack of emitter shorts (compared to the thyristor).

2.1.2 Off-State:

MCTs can be made over a broad range of voltages from 100V to 8KV to 10KV. MCTs can be made symmetric or asymmetric blocking.

High dv/dt capability is provided in the MCT when the junction charging current is diverted around the Base-Emitter junction of the PNP transistor through the low impedance of the Off-FET.

Leakage current is also diverted through the Off-FET, providing excellent high temperature voltage blocking capability. For instance, under laboratory conditions, MCTs have been operated turning off 80A at +300°C, withstanding dv/dt's of 10KV/μs at +250°C and surviving 100 hours of blocking life testing at +235°C junction temperatures. For these reasons it is recommended that the gate on bias be maintained continuously.

2.1.3 Turn Off:

The MCT provides a turn off capability, through gate control. Conventional SCRs can not be turned off by the gate. The insulated gate structure of the MCT allows turn off of the principle current with much less drive energy than GTO - SCRs.

2.1.4 Temperature Capability:

The thyristor structure and the thyristor alleviating the usual voltage and current stress of the typical MOSFET elements of the power FET or IGBT. The FET element helps the thyristor withstand self-turn-on. The Off-FET elements see little stress, since in the MCT structure, they are not active durning blocking and conduction. The Off-FET conducts only during turn-off transitions. The FET elements neither conduct the principal current, nor are they exposed to the mode without blocking voltage.

What is the MCTs temperature limit? Obviously, in the case of Harris' first commercial offering, it is now the package and the temperature to which we have taken sufficient reliability data. Ultimately, however, it is thermal runaway associated with leakage current, perhaps as high as +250°C in the 600 to 1000V range and +275°C in the 100V to 300V range.

2.2 Why a P-MCT With Its P-Power Device Limitations?

From the above discussion it would seem that there would be few circuit niches above 100 volts or 200 volts which would not be best served with an MCT. That indeed should be the case once Harris is able to market a full line of MCTs - especially N-MCTs. However, our first MCT products are P-type, i.e., they have a blocking voltage region that is P-type with inherently higher gain and with inherently lower SOA than in an N-type device.

The reason for this choice lies in the fact that the current density that can be turned off is 2 to 3 times higher if the Off-FETs are n-channel. To have a peak turn-off capability consistent with the MCTs high RMS current rating we decided that having n-channel Off-FET's was more important than the 30% higher SOA and 2 times lower switching loss that we would get (and have measured) in an N-MCT.

We still retain the low forward drop, good di/dt and dv/dt and good voltage and temperature capability but have sacrificed some usefulness, particularly in high frequency, hard switched circuits where SOA and switching losses are critical. Even in those circuits a snubber will allow one to use the P-MCT but at increased cost.

2.2.1 Where Should I Consider Using a P-MCT?

In any circuit dominated by conduction loss our first generation P-MCT can result in half the losses and use half the active silicon area - i.e., a smaller device and higher efficiency. In replacing a GTO or BJT it also offers the considerable advantage of MOS gate control. Even in hard switched circuits, at frequencies of several KHz and below, the P-MCT may be a good choice despite the possible need of a snubber circuit of some sort to keep the P-MCT within its turn-off SOA. In most instances, the MCTs high di/dt and good hard turn-on capability allows one to use a snubber consisting of a capacitor alone, somewhat reducing snubber cost and simplifying the circuit.

In Sections 5 and Section 6 P-MCTs are discussed in 1) hard switched, 2) soft switched, 3) SCR-like, 4) symmetric blocking and 5) complementary device circuits.

2.2.2 Where Should I Not Use a P-MCT?

As can be seen from the device ratings section, the P-MCTs SOA is rated at half the device's breakdown voltage rather than at the 80% typical of an n-type power device. If your circuit requires hard switched inductive turn-off above the SOA level and a snubber is not cost effective then you cannot use a P-MCT. Further, if your switching losses now are equivalent to your conduction losses you may gain very little. For example, consider replacing an IGBT of 50W conduction loss and 30W switching loss with a generation 1 P-MCT. One could rightly expect to find that the P-MCT would have <25W conduction loss but nearly 60W of switching loss. Adding the appropriate snubber would put the switching loss elsewhere which would have the cost advantage of allowing the use of an MCT of half the size of the IGBT. That still might not be the right answer to your circuit.

2.3 Future MCT Developments

Although this material is covered later in more depth, it is appropriate to describe the kind of MCT devices that can be expected to be developed and produced by Harris and other semiconductor manufacturers.

This would first include more voltage ratings - first asymmetric MCTs down to perhaps as low as 200V and as high as 1600V. Later, high voltage MCTs will be available for what are now typically thyristor and GTO circuits. (See Reference 2.)

P-MCTs will also improve in switching capability in both SOA and turn-off time, bettering N-IGBTs in speed and turn-off loss and being at less of a disadvantage in hard switched SOA.

N-MCTs will begin to become available but with about half the peak turn-off current capability of P-MCTs. However, both P-MCTs and N-MCTs will be improving in that characteristic as improved process capability allows denser Off-FET channel structure.

As with other FET-containing devices higher current switches will be produced in the form of modules, usually including diodes, and sometimes including some degree of intelligence. Our experience is that MCTs (up to 12 have been paralleled at Harris Power R&D) can be successfully paralleled if done carefully. As with IGBTs this is best done by the manufacturer.

The timetable for these developments depends on resources.

2.4 References

[1] V. Temple, "Power Device Evolution and the MOS-Controlled Thyristor", PCIM, November, 1987, pp 23-29.

[2] V.A.K. Temple, S.D. Arthur et al., "Megawatt MOS Controlled Thyristor for High Voltage Power Circuits" PESC 92 Proceedings, pp 1018-1025 (Toledo, Spain, June 29 - July 3, 1992)

MCT Equivalent Circuit Models

3.0 Introduction

The new Harris P-MCT is a high power and high speed switching device that is useful in many applications. In our user's guide we have included several models that can be used to investigate whether the generation 1 600V P-MCT that is Harris' first commercial MCT is appropriate for your application. As other products are announced it is hoped that the data sheets will include, for example, SPICE model parameters. In addition to SPICE model parameters we have included other physically based models that may be useful and in some cases more accurate.

3.1 SPICE Modelling of MCTs

3.1.0 Introduction

SPICE parameter extraction of the MCT device is not an easy job, because the MCT integrates the four layers of a PNPN thyristor with NMOSFET and PMOSFET elements in a single device. The SPICE program has no model for a PNPN device, so either a three-diode model or a two-transistor bipolar model must be used for the vertical PNPN structures. In general, the three-diode model is a device physics oriented approach but requires longer computation time, while the two-bipolar model is an applications oriented model and runs faster. Implementation of either of the two models requires a separation of the PNPN device somewhere in a semiconductor layer, so that minority carrier currents on both sides are not always equal. Another aspect to both models is transient analysis that is caused by current amplification of the PNPN. The bipolar model has current amplification, while the diode model lacks it. The two-transistor bipolar model has been chosen in this modeling.

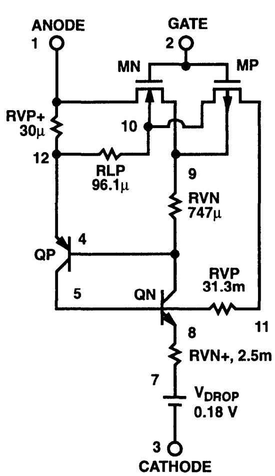
3.1.1 Equivalent Circuit

As realized in Harris' first 600V P-MCT, the P-MCT can be thought of as consisting of about 11,000 parallel groups of 9 20mm x 20mm unit cells in a 0.4cm^2 active area. In each group of 9 cells there is one on-cell surrounded by 8 off-cells. Figure 2.0.1 showed half of a cross section, i.e., half an on-cell and a complete off-cell along with the 2-transistor electrical equivalent circuit that is the basis of our SPICE model. The equivalent subcircuit model contains back-to-back connected NPN and PNP bipolar transistors, serial connected PMOSFET and NMOSFET, and parasitic passive components. The three-dimensional 600V P-MCT device has been converted to one-dimensional components with values as given in Figure 3.1.1.

3.1.2 Parameter Calculation

Dimensions and physical parameters of each layer were determined assuming doping in each layer is to be uniform, and a reasonable mobility is given to each layer. Finally, resistivity and diffusion lengths are calculated.

Parameter calculation for the two bipolars requires some caution. First, the collectors of PNP and NPN bipolars share the same P-/N-junction, so the collector area of each bipolar is taken to be a half of the junction area as shown in Figure 3.1.2. Second, reverse parameters are always unnecessary



	QP	QN
BF	9.1	2.75
VAF	2000	2000
IKF	600	600
IS	1.14E-10	1.14E-10
TF	42.9ns	207ns
CJE	9.47nF	1.25nF
VJE	1.0	0.66
CJC	362pF	362pF
MJC	0.5	0.5
VJC	0.64	0.64

	MN	MP
L	0.5	5.0
W	5.63	0.715
NSUB	1E18	8E13
U	500	200

FIGURE 3.1.1 P-MCT SUBCIRCUIT AND +150°C DEVICE CONSTANTS

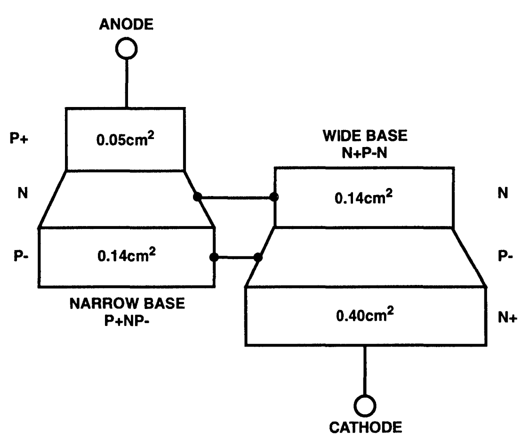


FIGURE 3.1.2 SHARED P- / N-JUNCTIONS IN NPN AND PNP BIPOLAR TRANSISTORS

TABLE 3.1.1 CALCULATED AND MODIFIED SPICE PARAMETERS AT T_J = +150°C

TABLE A WIDE BASE N+P-N BIPOLAR		UNIT	DEVICE PHYSICS	MODIFIED SPICE
Transport Saturation Current	IS	A	1.14E-10	1.14E-10
Ideal Maximum Forward Beta	BF	-	0.536	2.75
Fwd Current Emission Coeff	NF	-	1.0	1.18
Corner for Fwd Beta Roll-Off	IKF	A	3.45E-2	6.00E2
Forward Early Voltage	VAF	V	2.05E1	2.00E3
B-E Built-In Potential	VJE	V	0.66	0.66
B-C Built-In Potential	VJC	V	0.64	0.64
Base Forward Transit Time	TF	sec	4.72E-7	2.07E-7
B-E Zero Bias Capacitance	CJE	F	1.25E-9	1.25E-9
B-E Junction Exponent	MJE		0.5	0.5
B-C Zero Bias Capacitance	CJC	F	3.62E-10	3.62E-10
B-C Junction Exponent	MJC	-	0.5	0.5

TABLE B NARROW BASE P+NP BIPOLAR		UNIT	DEVICE PHYSICS	MODIFIED SPICE
Transport Saturation Current	IS	A	6.67E-10	1.14E-10
Ideal Maximum Forward Beta	BF	-	9.10	9.10
Fwd Current Emission Coeff	NF	-	1.0	1.18
Corner for Fwd Beta Roll-Off	IKF	A	4.42E1	6.00E2
Forward Early Voltage	VAF	V	2.00E2	2.00E3
B-E Built-In Potential	VJE	V	1.00	1.00
B-C Built-In Potential	VJC	V	0.64	0.64
Base Forward Transit Time	TF	sec	4.29E-8	4.29E-8
B-E Zero Bias Capacitance	CJE	F	9.47E-9	9.47E-9
B-E Junction Exponent	MJE		0.5	0.5
B-C Zero Bias Capacitance	CJC	F	3.62E-10	3.62E-10
B-C Junction Exponent	MJC		0.5	0.5

TABLE C OFF MOSFET		UNIT	DEVICE PHYSICS	MODIFIED SPICE
Zero Bias Threshold Voltage	VTO	V	2.0	2.0
Substrate Doping	NSUB	$1/cm^3$	1E18	1E18
Oxide Thickness	TOX	meter	7E-8	7E-8
Mobility	UO	$cm^2/V.sec$	500	500
Channel Length	L	meter	0.5E-6	0.5E-6
Channel Width	W	meter	5.63	5.63

TABLE D ON MOSFET		UNIT	DEVICE PHYSICS	MODIFIED SPICE
Zero Bias Threshold Voltage	VTO	V	-2.0	-2.0
Substrate Doping	NSUB	$1/cm^3$	8.0E13	8.0E13
Oxide Thickness	TOX	meter	7E-8	7E-8
Mobility	UO	$cm^2/V.sec$	200	200
Channel Length	L	meter	5.0E-6	5.0E-6
Channel Width	W	meter	0.715	0.715

TABLE E PARASITICS		UNIT	DEVICE PHYSICS	MODIFIED SPICE
PNP Emitter Resistor	RVP+	ohm	3.00E-5	3.00E-5
PMOS Series Resistor	RLP	ohm	9.61E-5	9.61E-5
NMOS Series Resistor	RVN	ohm	7.47E-4	7.47E-4
P- Layer Resistor	RVP	ohm	3.17E-2	3.17E-2
NPN Emitter Resistor	RVN+	ohm	1.22E-3	2.5E-3
NPN Base Voltage Drop	VDROP	V	0.18	0.18

because the MCT reverse operation is inhibited. Third, the SPICE BJT model allows only choice of one of two DC models - transport saturation current (IS) only or emitter and collector saturation current (ISE and ISC). The IS only model (Gummel-Poon model) has been chosen because of its simplicity. Twelve calculated parameters for each of narrow base PNP and wide base NPN bipolars are summarized respectively in Subtables A - E of Table 3.1.1.

The PMOSFET and NMOSFET of elements of the MCT are very high speed devices compared with bipolar speed. They work as voltage controlled switches, except for several approximately 10nsec gate delays. The MOSFET uses the Shichman-Hodges model, and the gate capacitance model is a 12-section Meyer model. These choices result in 6 parameters for each MOSFET. Physical parameters are given in Subtables C and D of Table 3.1.1. Notice SPICE uses the meter as a unit of length.

Parasitics consist of one voltage source and 6 resistors. The voltage source describes an electric field in the very wide base NPN bipolar transistor. NPN and PNP emitter resistances (RVN+ and RVP+) were determined from measured data in the forward ON state. The other three parasitic resistors were calculated from Figure 2.0.1, bringing the total number of SPICE parameters to 42 as seen from Table 3.1.1.

3.1.3 Parameter Calibration

The calculated SPICE parameters had to be calibrated to fit measured 600V generation 1 P-MCT data over a wide range of current, voltage, time, temperature and load.

The first step of calibration was to modify SPICE parameters to match measured forward OFF characteristics up to 700V at +25°C/+100°C/+150°C. The OFF condition biases the center P-/N junction in reverse, and leakage current through the junction determines the MCT OFF current. Critical SPICE parameters for the forward OFF state are:

1. NPN bipolar: IS, BF and VAF
2. PNP bipolar: IS and VAF

The IS of NPN was set to be equal to the IS of PNP because the collector-base junction of both bipolars are the same P-/N junction. Fit is fairly good at high voltage and high temperature, the more critical region because of the relatively higher losses, but poor at low voltage and room temperature. Once NPN BF was set to the calculated 0.536 value, fitting was between 50% and 200% at all voltage and temperature ranges. Later BF was modified to 2.75 to accommodate transient fitting. The OFF state loss is approximately 0.23W at 700V and +150°C, and becomes negligibly small at +100°C. It is noteworthy that the most important parameter, IS for the PNP, remains unchanged at 11.4nA.

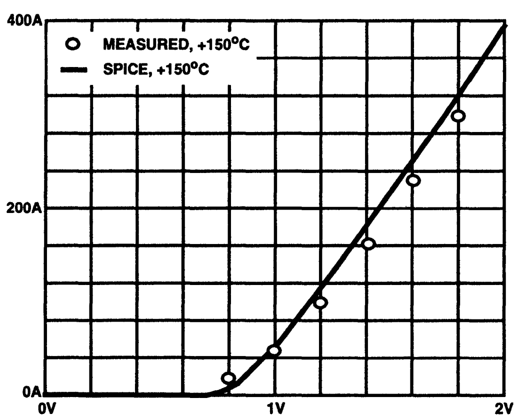


FIGURE 3.1.3. SPICE FORWARD VOLTAGE SIMULATION

The second step of calibration is ON-state characteristics. In this condition all the emitter junctions of MCT are forward biased and the central P- and N layers are strongly modulated by two types of injected carriers from P+ and N+ emitters, so that the forward drop is very much similar to a PIN diode. Measured and simulated forward ON characteristics from 10A to 300A at +150°C are plotted in Figure 3.1.3. Fitting is approximately within 50mV except at low current. Sensitive SPICE parameters for the forward characteristics are:

1. NPN bipolar: IS, BF and NF
2. PNP bipolar: IS and NF
3. Parasitics: RVN+, VDROP and RVP+

As IS's and BF's were already set in the first step the NF's of two bipolars and NPN emitter series resistance (RVN+) and PNP series emitter resistance (RVP+) are available to fit the measured data. Once BF of the NPN was set to the calculated 0.536, fitting was plus/minus 100mV at all the ranges. The 2.75 NPN beta calibration comes from the transient fitting. Power loss at 100A is approximately 120W at all temperatures.

The third step is the most difficult calibration - transient turn-on and turn-off which are influenced by different phenomena. An important process for the ON transient is plasma spreading carried by holes and electrons. Capacitances in the circuit delay the transient. The turn ON is fairly constant over various current, voltage and temperature. Sensitive SPICE parameters for the turn-on transient are:

1. NPN bipolar: BF
2. Parasitic: CPOLY

The minority carrier lifetimes in P- and N regions play major roles for the OFF transient. In SPICE they appear in the base transit times (TF).

Figure 3.1.4 compares simulated and measured turn-off time and energy for +150°C, 100A unsnubbered turn-off clamped at 300 volts. Fit to experiment is better than 10%. No doubt users will be able to refine the model for even better fits of key MCT behavior for their individual circuits. However, a perfect fit with the two-transistor model will always be difficult as it is not a true representation of the thyristor part of the MCT.

A model has been presented with fitting shown only for the +150°C case as this is normally the limiting case. Operation at other temperature requires 2 coefficients for each of IS (for conduction drop) and NF, TF (for turn off). Later datasheets and user's guide will include these coefficients.

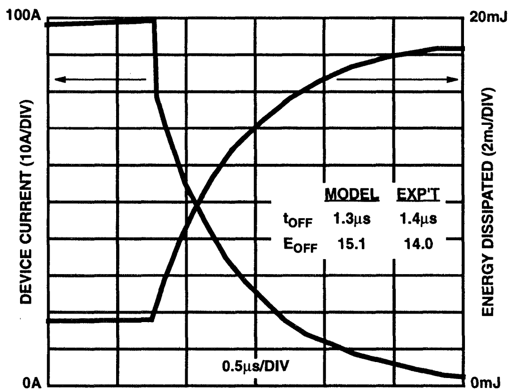


FIGURE 3.1.4. SPICE MODELLING OF 600V P-MCT TURN-OFF
(300V, +150°C Inductive Turn-Off)

3.1.5 Modelling Series/Parallel MCTs

One of the more important reasons SPICE modelling of MCTs was undertaken several years ago at Harris Power R&D was to design modules with parallel MCTs for a number of R&D programs focussed chiefly in aerospace systems. It was useful to introduce "weak" and "strong" MCTs in which turn-off times and forward drops were varied.

3.1.6 SPICE Modelling Summary

The newly developed MCT model can simulate not only MCT devices but also MCT power circuits and systems. The MCT subcircuit is a strong tools for design and verification of MCT power circuits. However, this is a first version of the model. In the future an upgrade of the model to a more accurate version with a MOS capacitor type CPOLY. Also, more transient measurements to cover wider ranges of applications. Finally, in using SPICE models there is often a lot of "numerical noise" caused by the fact that when the MCT switches, very small time steps are needed compared to the rest of the simulation. SPICE handles those transitions poorly, sometimes leading to wild oscillations. Holding down the maximum time step can work in many cases. In others, small snubbers need to be added between nodes where voltages change too quickly. For example, while the curves in Figure 3.1.4 had no snubber, small maximum time step was used which reduced numerical noise to acceptable levels. In using the same model as part of a half bridge circuit, a 0.5 ohm, 0.033μF snubber across the MCT to get the SPICE simulation to work.

3.2 Special MCT Models

3.2.0 Introduction

The big weakness of the MCT models built out of simpler devices is that they are non-physical in one important way. They do not account for the fact that the MCT is swamped with holes and electrons in the P- and N base regions. This has led to investigation of a 4-layer device model that can be implemented in SPICE or some other model useful to applications engineers. This has not yet been totally successful. However, some portions of that developing model have proved very useful, especially in calculating MCT turn-off.

Figure 3.2.1A shows a very simple MCT model for looking at turn-off. The MCT is assumed to be a current source in parallel with a capacitor. It is a very device physics oriented model which needs the current gain of the lower transistor, the recombination tail time constant and the device self-capacitance to accurately give the device turn-off trajectory (I and V vs t) along with device losses. In fitting low and high voltage turn-off to experiment, it was found that the above parameters are a function of voltage and current. For example, depletion width depends on current density in a known fashion. Also, undepleted base width controls current gain and is thus voltage and current dependent, also in a known way. Finally, recombining excess carriers are pushed toward and into the more heavily doped buffer region where recombination lifetimes are shorter. Here, a less precise parameter variation is possible.

The lower part of Figure 3.2.1 shows turn-off energies calculated for inductive turn-off of different currents with various snubber capacitors for temperatures of +75°C and +150°C. No energies are plotted for turn-offs that would at any time exceed the device SOA. In this case the SOA used is for a typical device and not all 600V generation 1 MCTs (75P60's). Later, in section 6, measured turn-off energies are plotted for the same currents and snubbers. Fits are excellent.

The model described was implemented in "c" programming language but could also be implemented, with less accuracy, in SPICE.

3.3 Summary

A passable SPICE model whose parameters have been fit to the first Harris 600V MCT (75P60). This model works well in modelling more complex circuits. It does not, however, check to see if the SOA has been exceeded.

We have also shown a different type of model useful for turn-off transients which is more physical than the 2-transistor SPICE model.

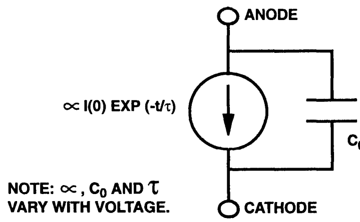


FIGURE 3.2.1A SIMPLE MODEL FOR MCT TURN-OFF
(∝ C_0 AND τ FIT TO GENERATION 1, 600V P-MCT)

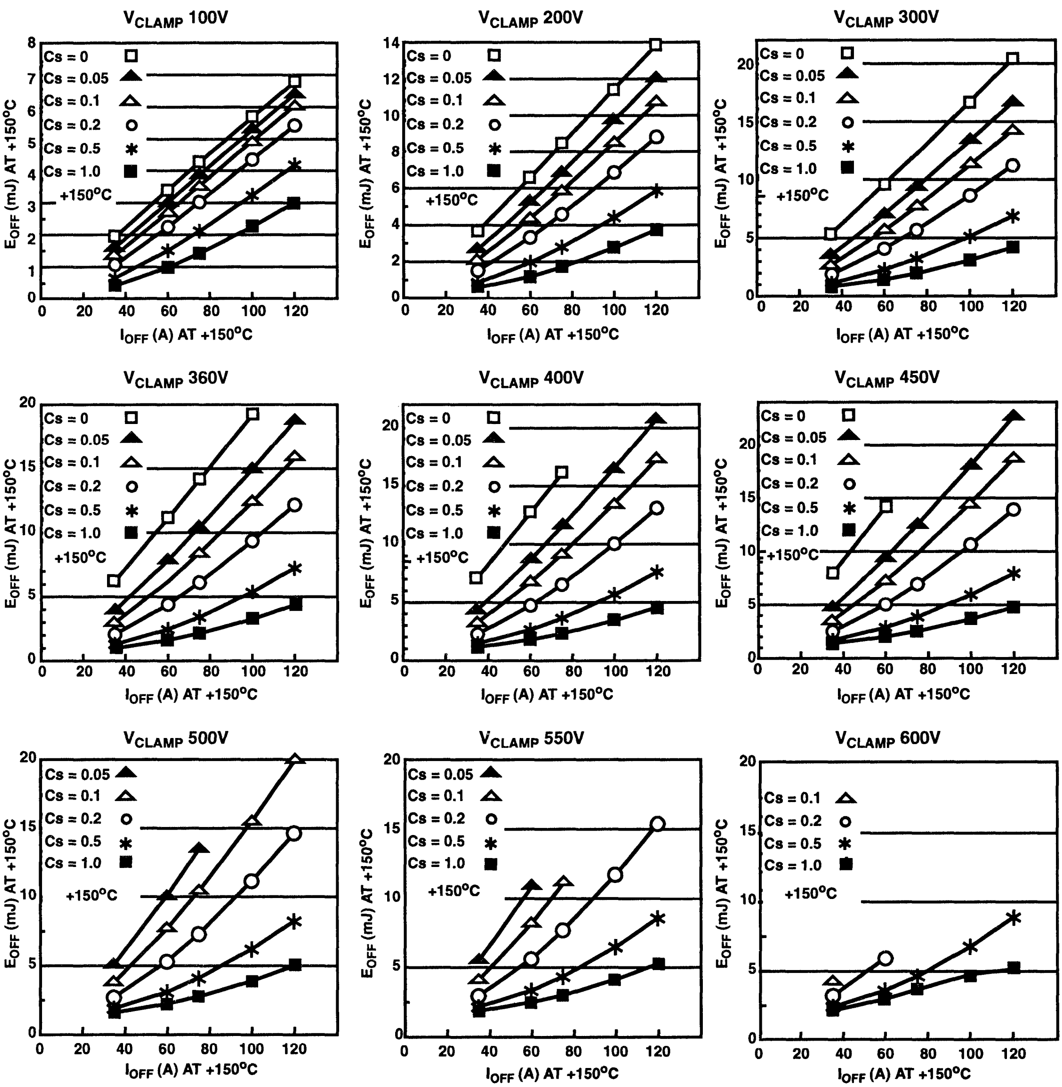


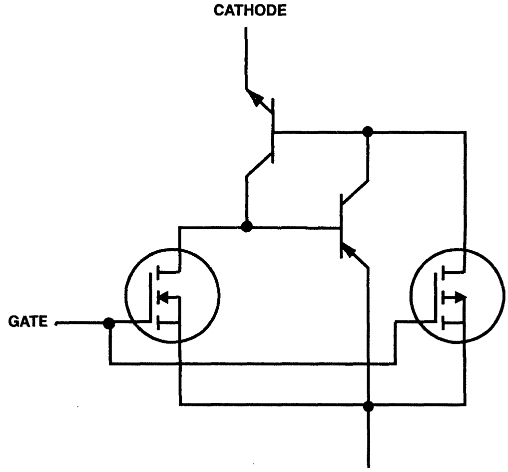
FIGURE 3.2.1B TURN-OFF ENERGY vs CURRENT AND SNUBBER

Characteristics

With the commercial introduction of the first MCT will come many questions concerning use and content of the data sheet. While the majority of the ratings, characteristics and curves will be familiar to most users, there are some subtle differences. This section is intended as a guide to the interpretation and significance of each of the ratings and characteristics that appear on a data sheet. The curves and figures used to illustrate these descriptions are intended to be generic and could be different than the curves included in an MCT data sheet.

Operation Explained by Means of the Equivalent Circuit

Most of the characteristics of an MCT can be understood easily by reference to the equivalent circuit shown here. An MCT closely approximates a bipolar thyristor (The two transistor model is shown) with two opposite polarity MOSFET transistors connected between its anode and the proper layers to turn it on and off. Since an MCT is an NPNP device rather than a PNPN device the output terminal or cathode must be negatively biased. Driving the gate terminal negative with respect to the common terminal or anode turns the P channel FET on, firing the bipolar SCR. Driving the gate terminal positive with respect to the anode turns on the N channel FET on shunting the base drive to PNP bipolar transistor making up part of the SCR, causing the SCR to turn off. It is obvious from the equivalent circuit that when no gate to anode voltage is applied to the gate terminal of the device, the input terminals of the bipolar SCR are unterminated. Operation without gate bias is not recommended.



Ratings

Most of the ratings seen on an MCT data sheet are identical to those found on PowerFET data sheets or are explained elsewhere in this document and do not need further explanation. The ratings which are differ from standard convention will be explained below.

- Peak Off-State Blocking Voltage: (V_{DRM})
  - Maximum allowable cathode to anode voltage. Explained in characteristic curve section.
- Peak Reverse Voltage: (V_{RRM})
  - The MCT is not by design a reverse blocking device, but like IGBTs it does have sufficient blocking capability to allow the use of an antiparallel diode.
- Continuous Cathode Current: (I_C)
  - Explained in characteristic curve section.
- Non-repetitive Peak Cathode Current: (I_{TSM})
  - This is the maximum allowable current through the device in the on-state at the pulse width. Junction temperature limits the acceptable peak current and pulse width.
- Peak Controllable Current: (I_{TC})
  - This is the maximum amount of cathode current the device is rated to turn off when commanded by the MCT gate signal. Turn off of the device is guaranteed in the circuit listed in the particular data sheet. This capability is for both inductive and resistive circuits. The volt amp load line in Figure 4.12 must be adhered to during turn-off. Attempting to turn the device off at currents higher than the rated peak controllable current may result in destroying the device. The device may be used at currents greater than the peak controllable current if it is commutated off at a current at or below the peak controllable rating.
- Gate-Anode Voltage (Continuous): (V_{GA})
  - Similar to other MOS gated devices.
- Gate-Anode Voltage (Peak): (V_{GA})
  - Allows for voltage overshoot during on and off gate voltage transitions, is explained elsewhere in the users guide.
- Rate of Change of Voltage: (dv/dt)
  - Explained in characteristic curve section.
- Rate of Change of Current: (di/dt)
  - Explained in characteristic curve section.
- Maximum Power Dissipation: (P_T)
  - A function of the maximum junction to case thermal resistance (0.6°C/W) and a maximum delta temperature (junction to case) of +125°C.

- Linear Derating Factor:
  - Self explanatory.
- Operating and Storage Temperature: (T_J, T_{STG})
  - Self explanatory.
- Maximum Lead Temperature for Soldering: (T_L)
  - Self explanatory.

Parameters

As with the ratings most of the parameters are similar to those found on PowerFETs or thyristor class devices, parameters which need further explanation will be clarified below.

- Peak Off-state Blocking Current: (I_{DRM})
  - Self explanatory.
- Peak Reverse Blocking Current: (I_{RRM})
  - Self explanatory.
- On-state Voltage: (V_{TM})
  - Explained in characteristic curve section.
- Gate-anode Leakage Current: (I_{GAS})
  - Self explanatory.
- Input Capacitance: (C_{ISS})
  - The MCT does not have Miller capacitance therefore it does not have gate plateau characteristics. The gate can be viewed strictly as a capacitance.
- Switching Characteristics:
  - Explained in characteristic curve section.
- Thermal Resistance: ($R_{\theta JC}$)
  - Self explanatory.

Static Characteristics

Low conduction drop of the MCT is what sets it apart from MOSFETs, BIPOLARs and IGBTs. As the characteristic curves show conduction drop voltage is diode like which accounts for the high DC current rating of the device. Important aspects of the conduction drop voltage characteristic are the current at which the temperature coefficient is zero and the negative temperature coefficient of the conduction drop voltage below that current.

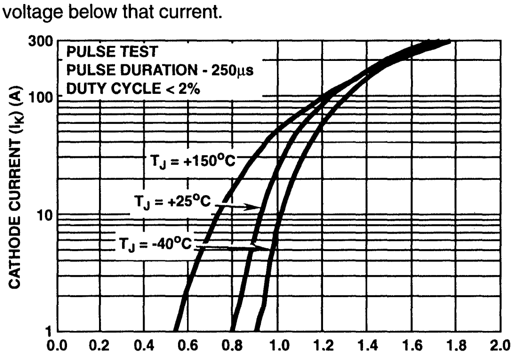


FIGURE 4.1 TYPICAL CONDUCTION DROP CHARACTERISTICS

Below the zero temperature coefficient current, conduction voltage decreases with increasing temperature; a practical ramification of this is that if mismatched devices are paralleled one device could go into thermal runaway. From a paralleling standpoint, it is advantageous to operate in an area of positive temperature coefficient which, depending on the circuit configuration, could mean operating above the peak switching capability of a single device. To operate above the zero temperature coefficient current the circuit must resonate or the current must be commutated to a safe switching level before it is switched off.

Figure 4.2 is a calculated curve which defines the DC current carrying capability of the device vs temperature, the limiting factor to the current is the rated junction temperature of +150°C. This curve was plotted using a junction to case thermal resistance of 0.6°C/W and a device with a I_K vs V_{TM} curve passing through $V_{TM(MAX)}$ at I_{C90} and T_J = +150°C. Using the above data and the following formula we can calculate the curve.

$$T_C = 150 - 0.6 * I_{DC} * V_{TM} \qquad I_{DC} = \frac{150 - T_C}{0.6 * V_{TM}}$$

The package limit shown on the curve is a wirebond limit and is not a function of the MCT die.

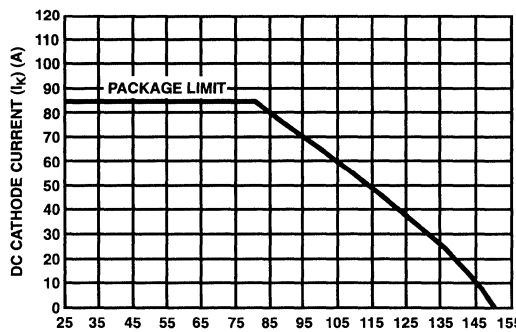


FIGURE 4.2. TYPICAL DC CURRENT CAPABILITY

Switching Characteristics

Hard switched characteristics are described in Figures 4.5 through 4.10, and Figures 4.3 and 4.4 show the switching circuit and switching waveforms respectively. To obtain turn on characteristics a double pulse test must be used. The first pulse charges the load inductor to I_{C90}. When cathode current reaches I_{C90} the MCT is gated off, current then transfers from the MCT to the freewheeling diode. The diode also functions as a voltage clamp which limits voltage overshoot at turn-off. After the MCT has been given time (3-5µs) to fully turn off, it is gated back on and current transfers back from the freewheeling diode to the MCT. Note that if the delay time between pulses is too long the resistance in the inductor diode loop and diode losses will cause the current to decay below I_{C90}. Also, if the second pulse is too long the maximum switching capability of the MCT could be exceeded.

An important point must be understood for this test and any other tests which include hard switching. The peak voltage

V_{KA} is not the supply voltage but must include any voltage excursion above supply voltage while the clamp diode is turning on.

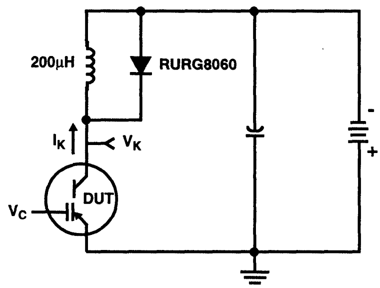


FIGURE 4.3 INDUCTIVE SWITCHING CIRCUIT

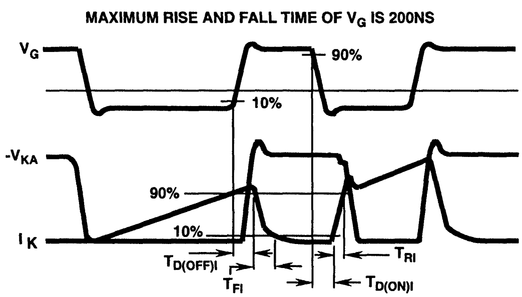


FIGURE 4.4 INDUCTIVE SWITCHING WAVEFORMS

Turn-off characteristics are measured at the trailing edge of the first current pulse and turn-on characteristics are measured at the beginning of the second pulse. Switching time measurements are defined as follows:

Turn-On Delay ($T_{D(ON)I}$) - Measured from the 90% point of V_G to the 10% point of I_K.

Turn-Off Delay ($T_{D(OFF)I}$) - Measured from the 10% point of V_G to the 90% point of I_K.

Turn-On Rise Time (T_{RI}) - Measured from the 10% point of I_K to the 90% point of I_K.

Turn-Off Fall Time (T_{FI}) - Measured from the 90% point of I_K to the 10% point of I_K.

Switching loss measurements are defined as the integral of the instantaneous power loss within the following time intervals:

Turn-On Switching Loss (E_{ON}) - Measured from the 90% point of V_G to the $V_{KA} = V_{TM}$ point.

Turn-off switching loss (E_{OFF}) - Measured from the 10% point of V_G to the $I_K = 0$ point.

Maximum operating frequency curves for a typical device (Figure 4.11) are presented as a guide for estimating device performance for a specific application. Other typical frequency vs cathode current (I_{AK}) plots are possible using the information shown for a typical unit in Figures 4.5-4.10. The operating frequency plot of a typical device shows f_{max1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

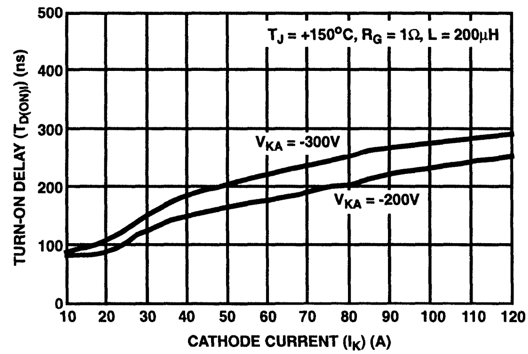


FIGURE 4.5 TURN-ON DELAY vs CATHODE CURRENT (TYPICAL)

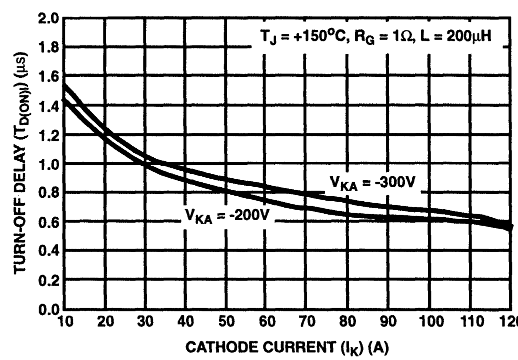


FIGURE 4.6 TURN-OFF DELAY vs CATHODE CURRENT (TYPICAL)

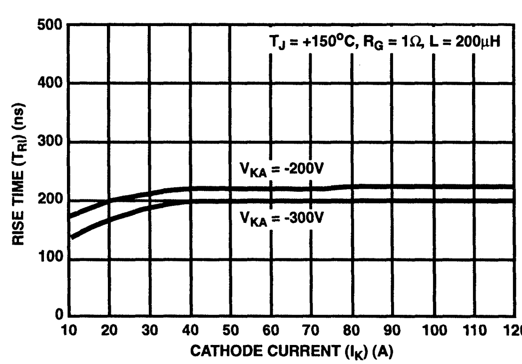


FIGURE 4.7 TURN-ON RISE TIME vs CATHODE CURRENT (TYPICAL)

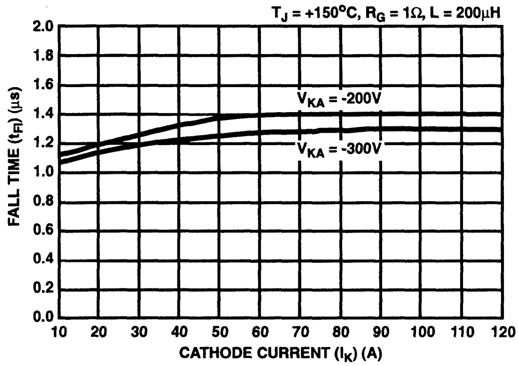


FIGURE 4.8 TURN-OFF FALL TIME vs CATHODE CURRENT (TYPICAL)

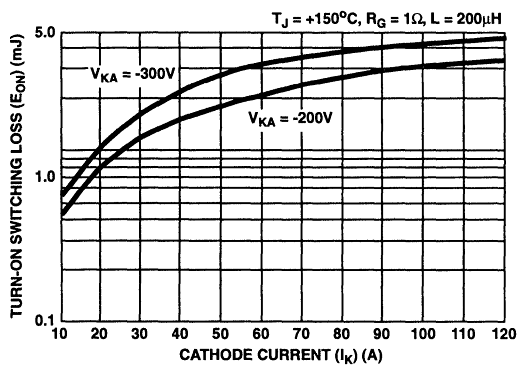


FIGURE 4.9 TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

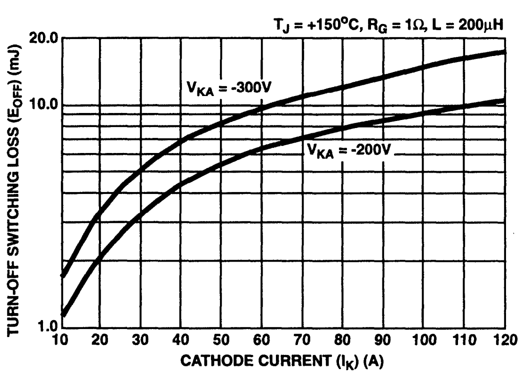


FIGURE 4.10 TURN-OFF ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

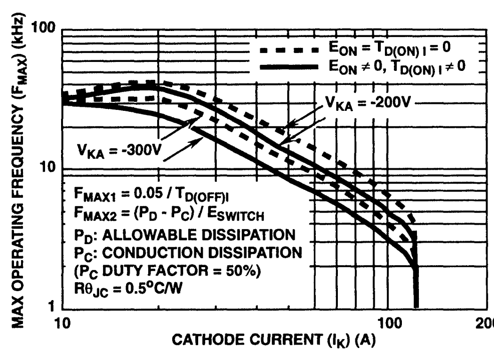


FIGURE 4.11 TYPICAL F_{MAX} CURVES

F_{MAX1} is defined by $F_{MAX1} = 0.05 / (T_{D(ON)I}+T_{D(OFF)I})$. $T_{D(ON)I} + T_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. Device delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $T_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

F_{MAX2} is defined by $F_{MAX2} = (Pd - Pc) / (E_{ON}+E_{OFF})$. The allowable dissipation (Pd) is defined by $Pd = (T_{JMAX} - T_C) / R_{\theta JC}$. The sum of device switching and conduction losses must not exceed Pd. A 50% duty factor was used and the conduction losses (Pc) are approximated by $Pc = (V_{AK} \cdot I_{AK})$. E_{ON} is defined as the power loss starting at the leading edge of the input pulse and ending at the point where the anode-cathode voltage equals the conduction voltage drop, ($V_{AK} = V_{TM}$). E_{OFF} is defined as the power loss starting at the trailing edge of the input pulse and ending at the point where the cathode current equals zero ($I_K = 0$).

Because Turn-on switching losses can be greatly influenced by external circuit conditions and components, F_{MAX} curves are plotted both including and neglecting turn-on losses.

P-type MCTs have switching SOA limitations as other P-type semiconductor switches as shown in Figure 4.12. Switching capability is primarily impacted by three things:

1. Gate voltage rise time - Gate voltage rise times longer than the times recommended in the data sheet will lower switching SOA capability below that shown in the Figure.

2. Gate voltage during turn-off - The gate voltage must reach and maintain the recommended level until the MCT is fully turned off. Gate voltages lower than the recommended level will cause the horizontal upper switching limit to move down. Dependence of switching capability on V_g is described elsewhere in the users guide.

3. V_{KA} peak - In the high voltage region of the switching curve, switching capability is also impacted by the peak level of V_{KA} during the switching transition. As mentioned previously, the voltage must include any overshoot above supply voltage. The overshoot will be of very short duration so an oscilloscope capabile of measuring very short pulses should be used.

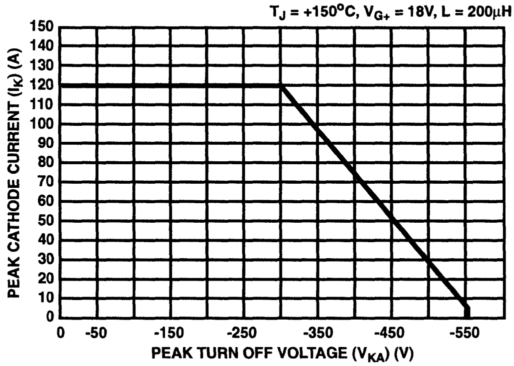


FIGURE 4.12 TYPICAL TURN-OFF CAPABILITY CURVE

Spike voltage data is intended to aid the user in evaluating MCT performance in zero voltage resonant switching circuits. Spike voltage is defined as the peak amplitude V_{KA} will reach before the device latches on. As shown in Figure 4.13, V_{SPIKE} increases with temperature and can be reduced by adding or increasing the size of the anode-cathode capacitive snubber.

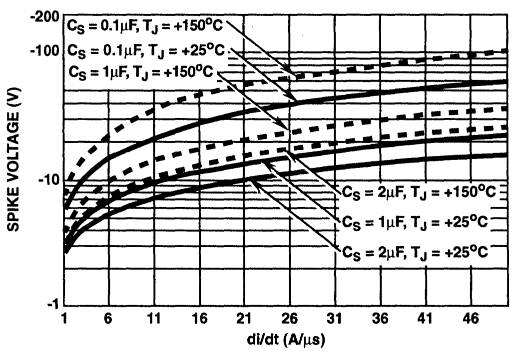


FIGURE 4.13 TYPICAL SPIKE VOLTAGE CURVES

In the spike voltage test circuit (Figure 4.14) the purpose of the 20V supply, diode and 500Ω resistor loop is to reverse bias the MCT. The reverse bias is intended to simulate the MCT bias in a resonant switching circuit as current begins flowing in the MCT. Figure 4.15 shows the timing of waveforms during the test. Load inductance and supply voltage are adjusted to provide the desired di/dt. Because V_{SPIKE} subtracts from the inductor voltage it will cause the current ramp to be nonlinear. As V_{SPIKE} is increased, supply voltage will also need to be increased to reduce the nonlinearity of I_K.

Two factors that may reduce the blocking voltage capability of the MCT are temperature and dv/dt. Figure 4.16 shows the relationship of the blocking voltage of a typical MCT to dv/dt. Temperatures above the rating (+150°C) will also reduce blocking voltage to less than rated voltage.

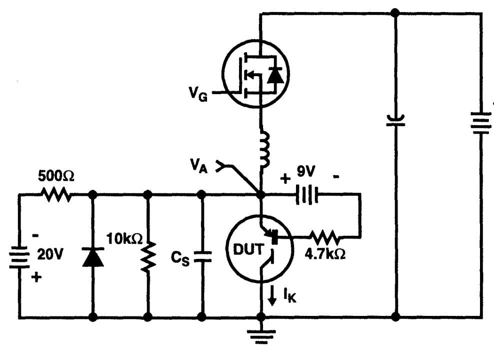


FIGURE 4.14 V_{SPIKE} TEST CIRCUIT

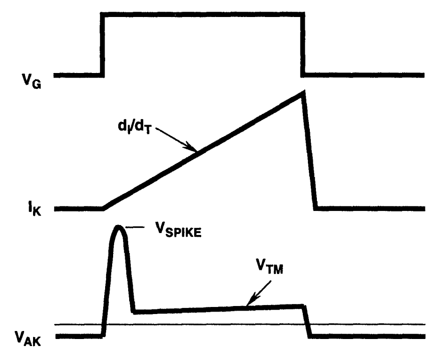


FIGURE 4.15 SPIKE VOLTAGE WAVEFORMS

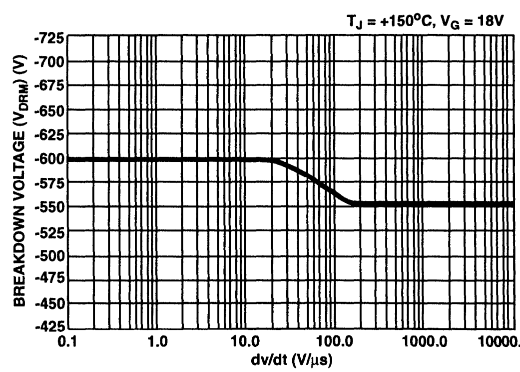


FIGURE 4.16 TYPICAL BLOCKING VOLTAGE vs dv/dt

Gate Circuits

5.0 MCT Gate Drive Requirements and Gating Circuits

The MCT has a MOS gate, similar to FETs and IGBTs, making it relatively easy to drive. The MCT gate capacitance is typically 10nF. Unlike other MOS gate devices the MCT gate experiences essentially no Miller current during switching, simplifying gate drive requirements. However there are several differences compared with other MOS gate devices that must be considered for successful operation. These differences will be discussed in more detail in the following sections. A brief discussion of several gate drive circuits can be found in section 5.3.0.

5.1 Gate Waveform

5.1.1 Boundary Limits

Rated performance of the MCT requires that the gate waveform meet criteria in amplitude and risetime. Figure 5.1.1 shows a graph of boundary limits for an acceptable gate waveform. The gate waveform should fall within the steady state limits during MCT ON or OFF time of the gate pulse. The gate waveform should fall within the shaded areas during the waveform transitions. These boundry limits are discussed in more detail in the following sections.

5.1.2 Negative Amplitude

The MCT is gated ON with a voltage that is negative with respect to the MCT anode. Since the MCT is a thyristor, internal regeneration will insure that the device switches fully to the ON state once cathode current exceeds the device holding current (mA's). The -7V steady state ON voltage boundary insures the MCT will switch ON and switch with reasonable delay time. The -20V steady state boundary insures that the gate will not be damaged from excessive voltage.

5.1.3 Negative Going Transition

One distinct difference between the MCT and other MOS gated devices is that the gate cannot be used to control the switching time of the MCT although the slope of the negative

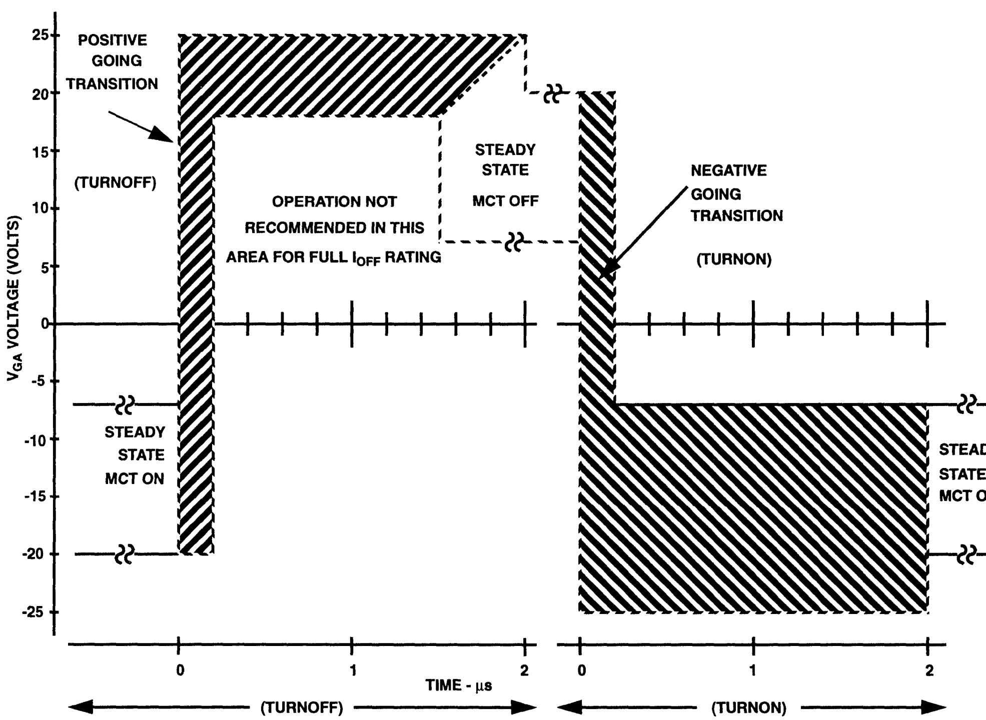


FIGURE 5.1.1. BOUNDRY LIMITS FOR MCT GATE WAVEFORM

going gate voltage transition does influence switching delay time. As the transition time is reduced gate displacement current will cause the MCT to initiate turn-on while the gate voltage is still positive. The boundary limits permit overshoot in negative going gate voltage.

5.1.4 Positive Amplitude

The MCT is gated OFF and held OFF with a voltage that is positive with respect to the MCT anode. The 18V ≥1.5μs duration OFF voltage boundary insures the MCT will switch off rated current at +150°C. The 20V steady state boundary insures the gate will not be damaged from excessive voltage. We do, however, allow the voltage to overshoot 20 volts to 25 volts but on a transient bases only

5.1.5 Positive Going Transition

The MCT turns-off by internal FET transistors shorting the base-emitter junction of the internal PNP transistor. To maximize turn-off capability the shorting FETs must be turned ON uniformly and rapidly to ensure that all MCT cells turn off essentially the same current. If the gate voltage rises slowly current will redistribute among the cells reaching a value in some cells that cannot be turned off. This requirement establishes the 200ns boundary time of the positive going transition. To ease problems with inductive gate overshoot the gate voltage is allowed to transiently go as high as ±25 volts.

5.2.1 Derating

If the minimum positive steady state gate voltage is reduced or if the positive going gate voltage transition time is increased the turn-off capability of the MCT is reduced as shown by the curves in Figure 5.2.1 and Figure 5.2.2. These curves are not to be interpreted as device ratings. They show measured performance on a small sample of devices that are believed to be representative of the broad population of devices. The solid line curves are suggested limits that could be used to estimate reduced I_{OFF} capability resulting from non-ideal gate voltage waveforms. The gate voltage referred to in Figure 5.2.2 occurs during the 1.5μs immediately following the positive gate transition. If increased rise time and reduced gate voltage occur simultaneously the % rating factors must be multiplied together. For example a gate pulse rise time of 0.5μs to 16V can be expected to reduce I_{OFF} capability to (0.6 x 0.83) 50% of rated.

5.3. Gating Circuits

5.3.1 Circuits Using Commercial Parts

Circuits for gating an MCT should meet the following requirements.

- Gate Drive Voltage - up to ±20V
- Rise/Fall Time - <200ns
- Peak Current - up to 2A
- Thermal - Handle Gate Current vs Frequency Plus DC Losses
- Signal Interface - Typically Magnetic or Optical Isolation
- Power Isolation - Gate Drive Circuit Ohmically Connects To MCT Anode. Isolation Required For Bus Voltage And Switching dv/dt.

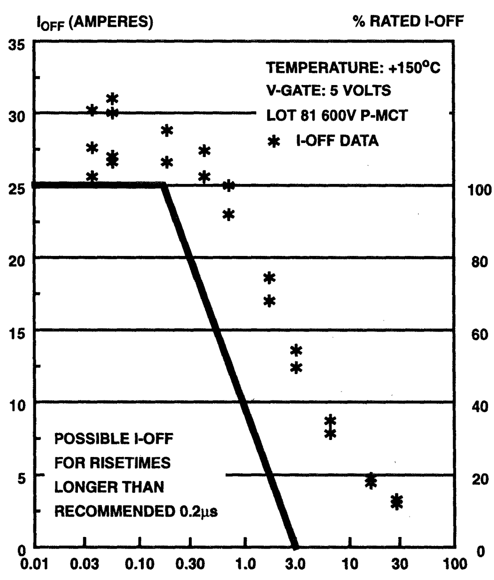


FIGURE 5.2.1 I_{OFF} μs GATE RISETIME (μs) I

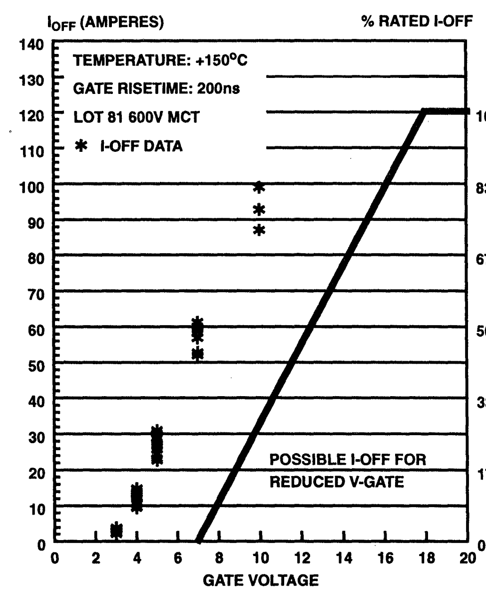


FIGURE 5.2.2 I-OFF vs GATE VOLTAGE (TYPICAL)

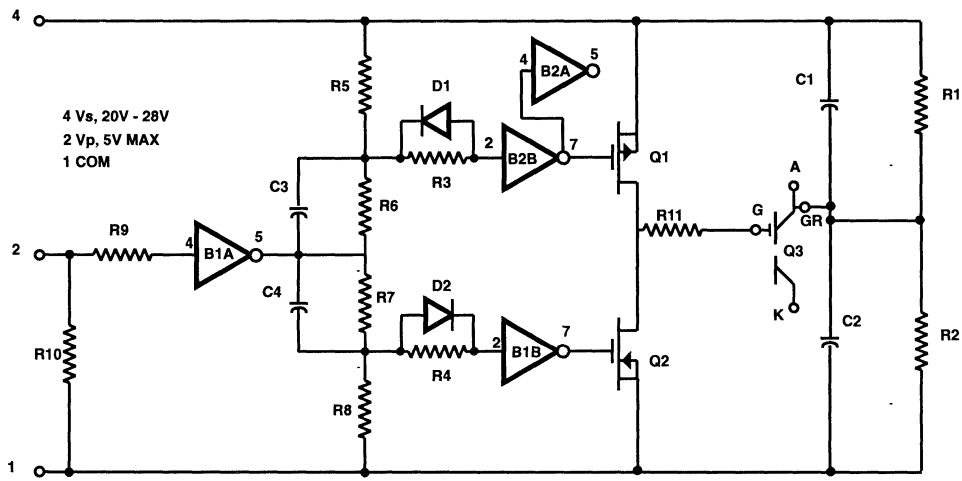
The circuits that follow illustrate several different approaches for gating the MCT. The fact that the required peak to peak MCT gate voltage exceeds FET drive requirements narrows the choices of commercially available ICs that can directly gate the MCT. Each of the driver circuits will typically be energized from a transformer secondary (usually high frequency) and rectifier to provide isolated DC power. The switching signal will typically be coupled through a fiber optic light pipe or optocoupler. Either of these would be energized from the isolated DC voltage through appropriate voltage divider or zener diode.

5.3.2 Circuit 1 - Using Dual FET Drivers

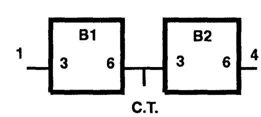
Figure 5.3.1 shows a gate drive circuit topology which utilizes two dual 15V-18V rated FET driver ICs and discrete FETs to generate the required 20V+ MCT gate turn off signal. The secondary of power supply transformer produces ±13V which energizes the two dual power inverters connected between the transformer neutral and each rail. The input signal at terminal 2 is level shifted to drive upper and lower power inverters which in turn drive FET transistors Q1 and Q2. The voltage capability of these transistors must exceed the 26V range required for the MCT. Components D1-R3 and D2-R4 provide differential delay to avoid overlap short circuit current through Q1 and Q2. Resistor R11 provides damping for gate voltage waveform. Resistors R1 and R2 establish the division of bus voltage between positive and negative voltage applied to the MCT gate. Capacitors C1 and C2 provide bus filtering and the peak current required to switch the MCT gate capacitance.

Assessment:

+ Circuit Operation is Tolerant of Bus Voltage Variation.
+ Circuit Can Drive MCTs in Parallel by decreasing $r_{DS(ON)}$ of Q1 And Q2.
+ Multiple Sources for all Parts.
- Circuit is Relatively Complex for Driving a Single MCT.



NOTE: V2+ = MCT GATED ON
V2 PULSE = 5V MAX



R1 = 6.7K	C1 = 10μF, 25V	
R2 = 3.3K	C2 = 10μF, 25V	
R3 = 3K	C3 = 100pF	
R4 = 3K	C4 = 100pF	
R5 = 15K		
R6 = 15K	Q1 = IRFD9113R	
R7 = 15K	Q2 = IRFD113R	
R8 = 15k	Q3 = MCT	
R9 = 100		
R10 = 1000	B1 = ICL7667	
R11 = 0.15	B2 = ICL7667	

FIGURE 5.3.1 MCT GATE DRIVE CIRCUIT USING TWO DUAL FET DRIVER ICs

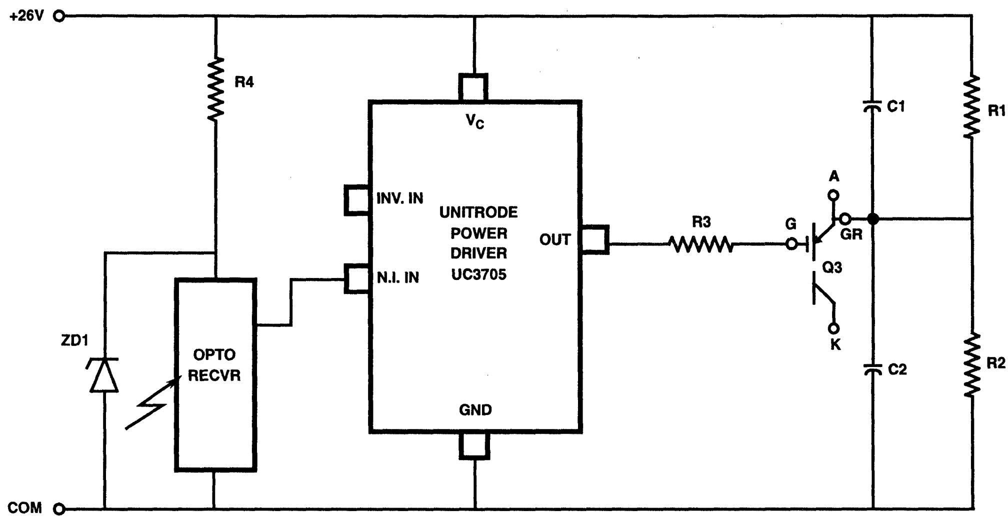


FIGURE 5.3.2 MCT GATE DRIVE CIRCUIT USING UNITRODE POWER DRIVER IC

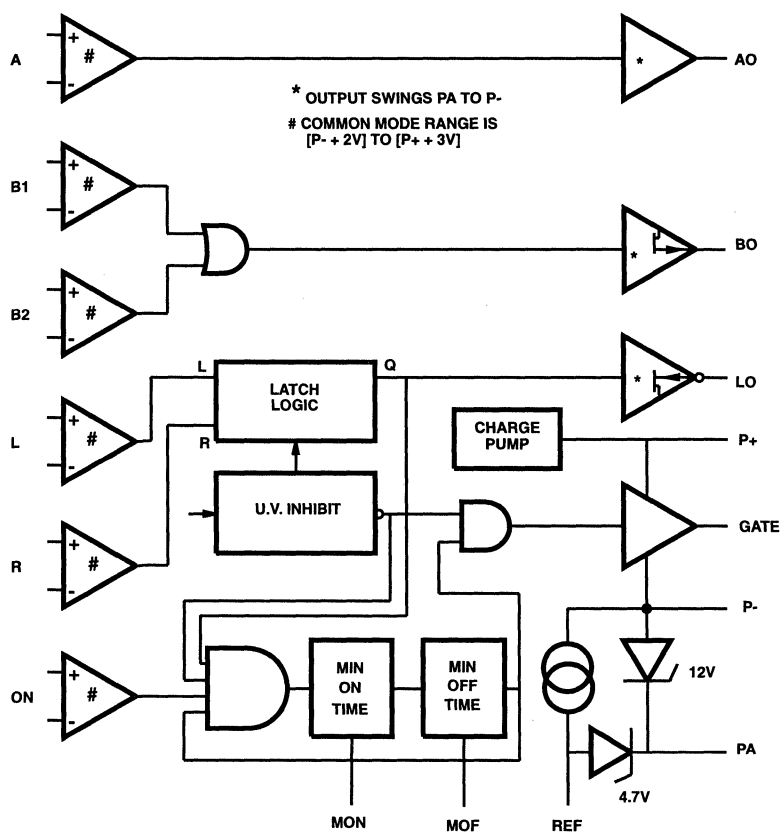


FIGURE 5.4.1 BLOCK DIAGRAM MCT DRIVER II

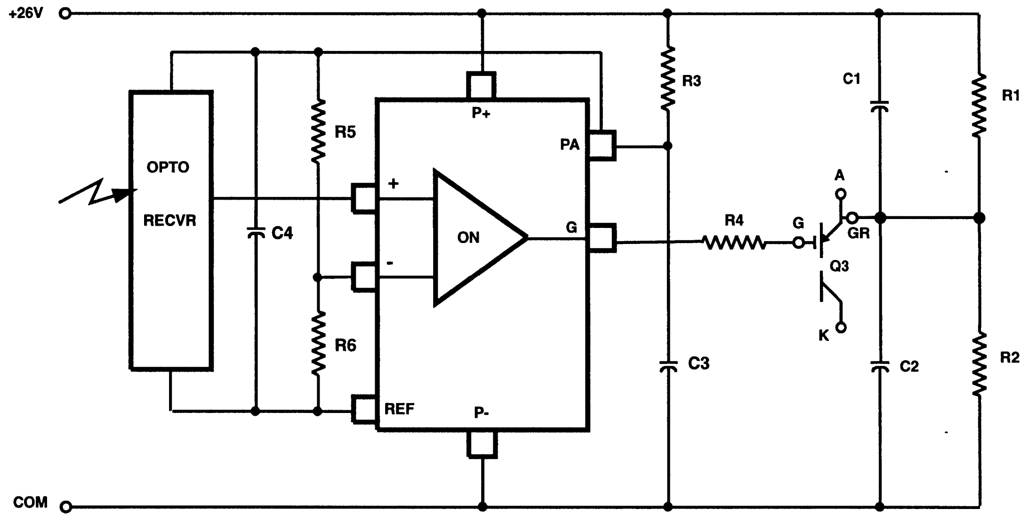


FIGURE 5.4.2. MCT GATE DRIVE CIRCUIT USING HARRIS DEVELOPMENTAL DRIVER IC

5.3.2 Circuit 2 - Using Power Driver IC

Figure 5.3.2 shows a gate drive circuit topology which uses a 35V rated FET power driver to generate the required 20V+ MCT gate signal. The transformer and diodes produce the 26V required to directly energize the power driver. The input is compatible with a variety of opto receivers. Resistor R3 provides damping of gate voltage waveform. Resistors R1 and R2 establish the division of bus voltage between positive and negative voltage applied to the MCT gate. Capacitors C1 and C2 provide bus filtering and the peak current required to switch the MCT gate capacitance. This circuit is attractive however the user should be aware that this driver has an internal thermal shutdown feature which drives the output low if the temperature exceeds +155°C. This will gate the MCT ON, which probably will be judged undesirable.

Assessment:

+ Circuit Uses Few Components.

+ Higher Output Current Drivers Available.

_ Internal Thermal Shutdown (+155°C) Gates MCT On.

5.4.0 Circuits Using Developmental Parts

5.4.1 MCT Driver II

An MCT driver IC has been developed which is not yet available commercially. This IC has been designed to provide the power circuit designer with many useful functions. Figure 5.4.1 shows a simplified diagram of this integrated circuit. The circuit contains three major blocks, power circuit, main MCT ON/OFF channel and auxiliary comparators. In this discussion all voltages are referenced to the PA terminal, which is typically connected to the MCT anode.

The IC can be powered from a negative supply (7V - 12V), internally clamped at 12V, or from center tapped supply (P- to PA to P+) or from a single ended supply (P- to P+). When using a negative supply an internal charge pump energizes the P+ terminal. A -4.7V reference voltage can sink up to 30mA and can be used to directly energize opto receivers or other control circuits. Standby current is less than 5mA for the IC.

All control signals enter the IC through comparators which require only a few mV of input signal. The common mode range includes the PA terminal and -4.7V REF terminal allowing several volts of noise rejection. The main ON channel controls the gate output which is capable of driving 4 MCT gates connected in parallel. The ON channel includes Minimum-ON-Time and Minimum-OFF-Time functions which are user programmable by adding external capacitance. These functions can be used to provide adequate snubber reset time for example.

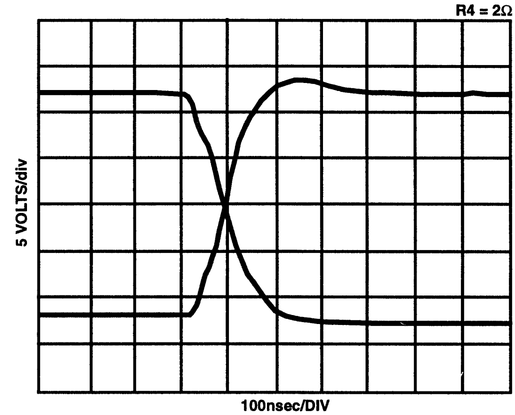
The IC contains both undervoltage inhibit and a latch which when set will force the ON channel to the MCT OFF state. The latch is set by the L comparator and is reset by the R comparator. When the latch is set the LO output will sink current (20mA max) for driving LED. With these inputs the user can implement over current or over temperature lockout functions for example.

The IC also contains two uncommitted comparator channels. The "A" channel has a totem pole output, "AO", capable of driving 20mA. The "B" channel has two comparator inputs which are OR'ed together and drive the "BO" output which will source current (20mA max) for driving an LED. These uncommitted channels can be used for detection, timing, and logic functions for example.

Figure 5.4.2 shows how this integrated circuit can be used in its simplest configuration to drive an MCT. The REF terminal can be used to power an opto receiver and provide reference voltage for the comparator input. In the arrangement shown resistors R1 and R2 establish the division of bus voltage between positive and negative voltage applied to the MCT gate. Capacitors C1 and C2 provide bus filtering and the peak current required to switch the MCT gate capacitance. Resistor R3 powers the integrated circuit. Resistor R4 provides damping the gate voltage waveform.

Figure 5.4.3 shows MCT gate voltage waveforms when driven by this IC. The + or - amplitude can be adjusted by the power supply voltage and resistors R1 and R2 to supply the desired amplitude of gate voltage.

Section 6.3 describes a DC circuit breaker which utilizes two MCTs and two of these driver ICs to implement all of the control circuits.



NOTE: + AND - AMPLITUDES CAN BE ADJUSTED TO MATCH RECOMMENDED DRIVER REQUIREMENTS.

FIGURE 5.4.3 OUTPUT VOLTAGE OF DEVELOPMENT MCT GATE DRIVER IC DRIVING ONE MCT GATE

Applications

6.0 Using The MCT

The MOS Controlled Thyristor (MCT) is a solid state unidirectional power switch that exhibits low conduction drop (2volts - 3 volts) at high current as illustrated in Figure 6.0.1. As described in section 2, the MCT requires low power to gate, has high surge current, high di/dt and dv/dt withstand capability and is able to switch at junction temperature in excess of +150°C. The MCT should be considered for power switching applications where high current capability with relatively low conduction loss are prime requirements.

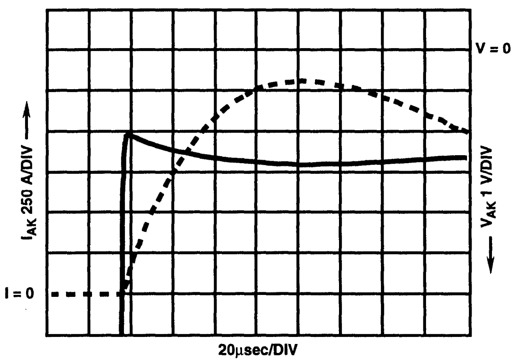


FIGURE 6.0.1. VOLTAGE ACROSS MCT DURING 1300 AMP PEAK PULSE

This section discusses key issues for successfully using the MCT in power switching circuits such as inverters, converters, motor drives, pulse circuits, etc. The discussion is divided into five categories; Hard Switching, Soft Switching, SCR circuits, AC Switch circuits and Complementary circuits.

6.1.0 Hard Switched Operation

6.1.1 Turn-OFF Stress

Hard switching circuit applications subject the switching MCT to substantial simultaneous voltage and current during switching, resulting in high instantaneous power dissipation in the MCT. Many power conversion circuits operate in the hard switched mode. The diagram in Figure 6.1.1 shows a circuit that generates hard switched stresses on the MCT and this circuit will be used as a basis for discussing hard switched operation. The circuit is operated at very low duty factor allowing the MCT to be stressed up to rated voltage and current from a low power source. The MCT can be artificially heated (hot plate) to simulate self-heating.

The MCT in Figure 6.1.1 switches inductive current pulses from a low impedance power supply. Capacitor C1 is the DC source capacitor and must be large enough to supply the current pulse with less than 5% voltage droop. In practice it may be implemented with an electrolytic capacitor paralleled by a low impedance Multi Layer Ceramic capacitor. Inductors L1a and L1b are the stray inductances associated with the circuit loop connecting C1, D1 and MCT Q1. Inductor L2 is the principal load impedance limiting current during a pulse. Diode D1 clamps the MCT voltage to the supply bus and provides a current path for current in L2 to flow when the MCT is not conducting. Components R2, D2, C2 form a polarized snubber which, under some operating conditions, may be needed to control MCT overshoot voltage or keep the V-I switching path within the allowable SOA.

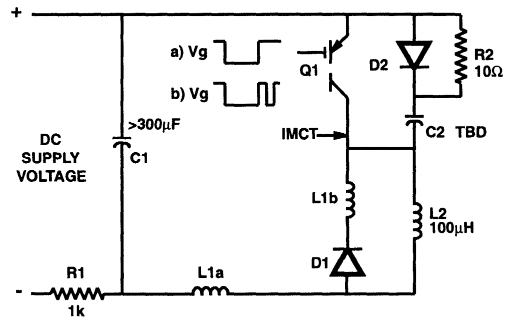


FIGURE 6.1.1 CIRCUIT THAT GENERATES HARD SWITCHING STRESS ON THE MCT

The I_{OFF} test uses wave form (a) to gate the MCT. When the MCT is gated ON current increases through inductance L2 to the desired peak current value. The ON time and the load inductance are selected to reach the desired current in about 50µs, for example. When the MCT is gated OFF the current through the MCT remains constant as the voltage increases until diode D1 conducts, clamping the cathode voltage to the negative bus. During this transition interval the MCT is subjected to high peak power dissipation. The increase in MCT voltage typically occurs rapidly (1000's V/µs) as the load current charges the equivalent capacitance of the MCT (~30nF). The turn-off of the MCT cannot be safely slowed down by reducing the gate drive as discussed in section 5.1.5.

While switching off, the instantaneous values of MCT voltage and current must stay within the safe switching area or "SOA" (Safe Operating Area) shown in Figure 6.1.2 The high current boundary of this curve is the maximum current that the MCT can turn off and is limited by the resistance of the internal OFF-FETs. The negative slope boundary is the SOA limit for the MCT. During the fast voltage transition, while switching off, stray inductance L1 will allow the MCT voltage to transiently exceed the supply voltage. For small values of stray inductance the overshoot voltage may be adequately limited by the capacitance of the MCT. For larger values of stray inductance it will be necessary to utilize a snubber network (C2, D2, R2 for example) to limit overshoot voltage.

The MCT power loss when switching off is a function of device current, peak voltage and junction temperature. In power circuit applications it may be necessary to add a snubber capacitor to keep the MCT I-V switching path within the safe switching area. In addition, snubber capacitance may be needed to reduce overshoot voltage, as previously discussed. The family of curves in Figure 6.1.3 shows typical MCT switching loss at +75°C and at +150°C, the maximum junction temperature for one of our 75P60 600V P-MCTs. These curves cover a range of peak voltage, snubber capacitor values and current enabling the estimation of switching loss under user conditions. Nine of these sets of curves are for +150°C junction temperature operation and therefore represent maximum typical losses in the MCT. The curves whose endpoints reach 120 amperes are limited by maximum turn-off ability of the MCT. The curves whose endpoints are less than 120 amperes are at or near the SOA limit of the MCT. In addition to the +150°C data, 3 sets of curves allow turn-off energy to be estimated at +75°C. Some of these measured switching loss curves extend beyond the Safe Switching Area limit shown in Figure 6.1.2. This does NOT imply that the Safe Switching Area limit can be exceeded safely for all devices.

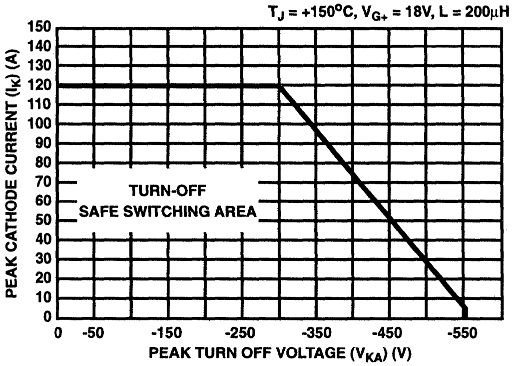


FIGURE 6.1.2. TURN-OFF CAPABILITY vs ANODE-CATHODE VOLTAGE

6.1.2 Turn ON Stress

In the hard switched case, the MCT turns on from high blocking voltage with minimal inductance to limit increase in current. This condition occurs in the circuit of Figure 6.1.1 when gate waveform (b) is used. During the initial ON interval the test current is established in the inductor as previously described. After brief (5µs) off-period, which allows the MCT to fully recover blocking, the MCT is gated ON again for 5µs. During this second turn-on the MCT may experience high di/dt while the conducting diode recovers blocking voltage. The 5µs ON-time allows the MCT to turn on fully before the final OFF-transition occurs. These switching conditions are found in many types of inverter/converter circuits.

The presence of stray inductance L1 allows the MCT voltage to fall during current transfer and reduces the magnitude of peak diode recovery current. However this is in conflict with the requirement of reducing stray inductance to limit overshoot voltage and switching losses as discussed in section 6.1.1. In practice, it is typically found that overshoot voltage is the more limiting factor. Therefore, reducing stray inductance is probably the proper design objective. Typically, with fast recovery diodes, the MCT turn-ON switching loss is relatively small. Figure 6.1.4 shows typical turn-on energy loss as a function of cathode current for 200 volts and 300 volts. The MCT current that occurs during recovery of the diode can be several hundred amperes and is typically within the surge capability of the MCT. Device failures have been observed with turn-on di/dt in the range of 6000A/µs.

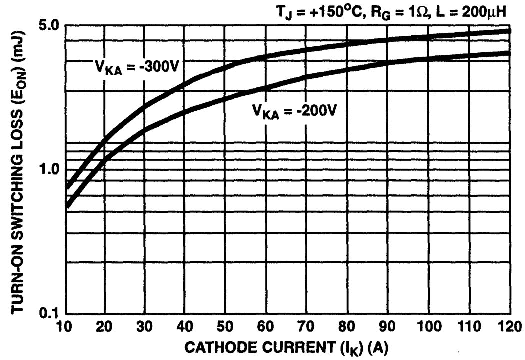


FIGURE 6.1.4. TURN-ON ENERGY LOSS vs CATHODE CURRENT (TYPICAL)

6.2.0 Soft Switched Operation

Soft switching and resonant power circuits are being employed,in part,as a means of reducing switching losses and stress on power switches thereby allowing higher operating frequency (references section 9 papers 16, 28, 33, 35). Soft switching occurs when the power switch is near zero current and/or zero voltage during the switching event. There are many different circuit topologies that limit switching stress on power switches. In these topologies the power switch is typically connected as part of an LC circuit and operated in one of two different modes. First, it can operate with the power switch in series with an inductor or second, with the power switch in parallel with a capacitor. The circuit in Figure 6.2.1 generates soft switching stresses on the MCTs and this circuit will be used as the basis for discussing soft switching operation.

6.2.1 Circuit Operation

The circuit in Figure 6.2.1 is operated in the following sequence. Initially capacitor C1 is discharged by a large value resistor R1. The switching sequence is initiated by gating MCT Q1 ON followed by gating MCT Q2 ON. Current increases linearly through the inductor as established by Vsupply/L1. When MCT Q1 is gated OFF the voltage increases across MCT Q1 as L1 and C1 ring. The peak voltage across MCT Q1 is determined by the resonant impedance of L1C1 and the value of current in the inductor L1 at the time MCT Q1 is gated OFF. When the oscillation decays C1 will be charged to the supply voltage and the current through MCT Q2 will be small (Vsupply/R1). MCT Q2 can be gated OFF and C1 will discharge through R1 completing the sequence of operation.

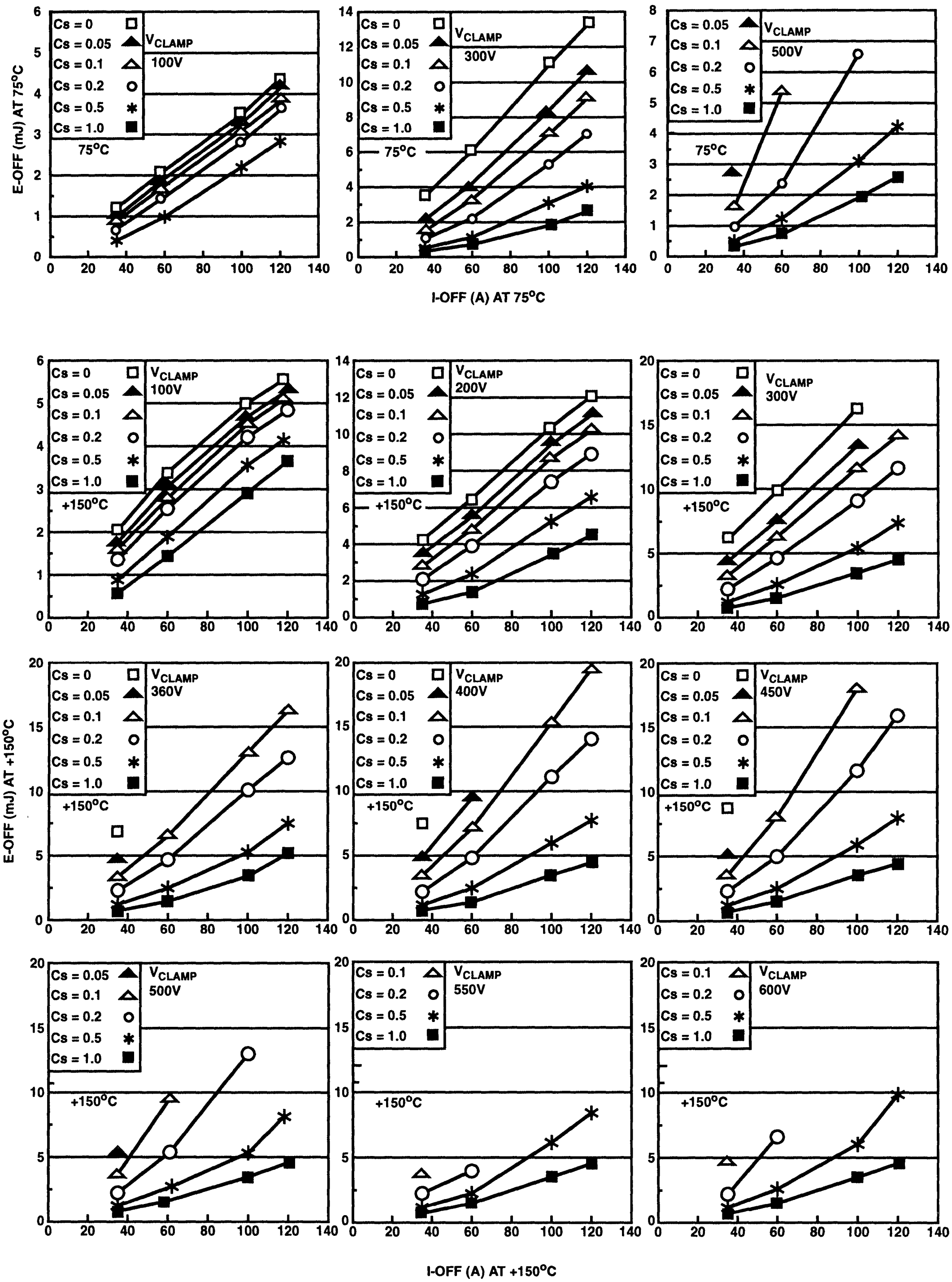


FIGURE 6.1.3. LOT 81 INDUCTIVE LOAD TURN-OFF ENERGY AS A FUNCTION OF SNUBBER CAP. AND CURRENT

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APPLICATION NOTES

6.2.2 Series Inductor Case

In the circuit in Figure 6.2.1 MCT Q2 is in series with inductor L1. Soft switching occurs if the current in the series inductor is substantially zero at the time of switching. If the inductor is larger than a few µH current increase during voltage collapse (<100ns) will be limited to a few amperes resulting in low turn-on loss.

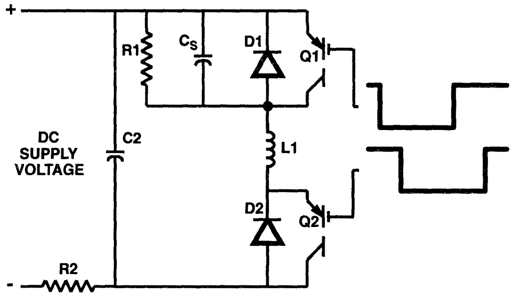


FIGURE 6.2.1 CIRCUIT THAT GENERATES SOFT SWITCHING STRESS ON THE MCT

During the circuit operating cycle inductor L1 and capacitor C1 ring causing current to flow through diode D2. MCT Q2 can be gated OFF during the oscillation while diode D2 is conducting, achieving soft switching. As the current tries to reverse both diode D2 and MCT Q2 block. If the conduction time of diode D2 has been longer than the recombination time of the MCT (<2µs) only displacement current will flow during the voltage increase across the MCT resulting in low switching loss. However, if the conduction time of diode D2 is <2µs, the MCT will not be fully recovered when forward voltage appears across the MCT. The remainder of the recombination tail current will flow, resulting in a small to moderate switching loss. In addition, since the MCT is not fully recovered, the turn-on voltage spike (discussed in section 6.2.3) will be reduced.

6.2.3 Parallel Capacitor

In the circuit in Figure 6.2.1 capacitor C1 is in parallel with MCT Q1. Soft switching occurs in MCT Q1 when the capacitor voltage is near zero at the time of switching. The ideal soft switched turn-on is degraded by the need for a small charge to flow into the MCT before it can switch ON. This will result in a voltage spike occuring across the MCT prior to turn-on. The curves in Figure 6.2.2 enable estimating the magnitude of this turn-on voltage spike. The curves show turn-on spike voltage as a function of current di/dt flowing into the parallel combination of capacitor and MCT. The test conditions duplicate circuit operation by having the MCT gated ON prior to becoming forward biased. These curves indicate that a turn-on voltage spike of several volts should be expected when switching 1kH resonant current increasing to several 10's of volts at 100kH.

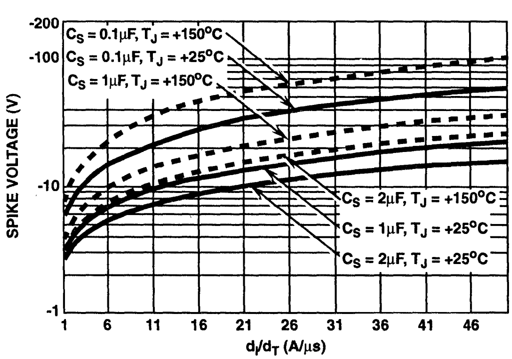


FIGURE 6.2.2. SPIKE VOLTAGE vs D_I/D_T (TYPICAL)

When the MCT switches ON it discharges the capacitor resulting in a power loss. The curve in Figure 6.2.3 shows the value of MCT switching loss as a function of current di/dt flowing into the parallel combination of capacitor and MCT. The MCT loss results from MCT current flow prior to reaching peak voltage on the capacitor plus discharge of the capacitor.

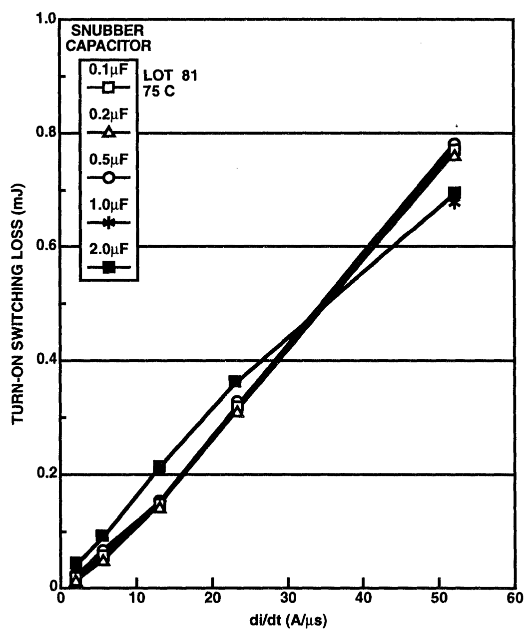


FIGURE 6.2.3. SNUBBERED TURN-ON ENERGY LOSS IN MCT vs di/dt (TYPICAL)

The parallel capacitor snubbers the MCT during turn-off. This allows circuit current to transfer from the MCT into the capacitor slowing the increase in voltage across the paralleled MCT and capacitor combination. As a result switching losses in the MCT are reduced as discussed in section 6.1.1. An upper bound of MCT turn-off switching loss can be estimated using the curves in Figure 6.1.3 for the same size capacitor.

6.2.4 MCT Dynamic Breakdown Voltage

Off-state DC blocking voltage of the P-type MCT is reduced by the presence of carriers within the device. When the MCT is blocking voltage, carriers can be present due to a) unrecombined carriers remaining in the turn-off recombination tail, b) displacement current from dv/dt and c) thermal generation current. Figure 6.2.4 shows the effect of a linear dv/dt ramp from zero voltage at +150°C on reducing DC blocking voltage. If your blocking voltage trajectory is less stringent, for example, sinewave or exponential, then it is appropriate to add some B.V. correction. This is discussed more fully below for dv/dt's that are essentially sinewaves.

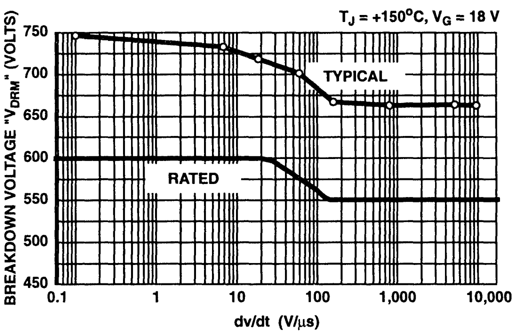


FIGURE 6.2.4. BLOCKING VOLTAGE vs dv/dt

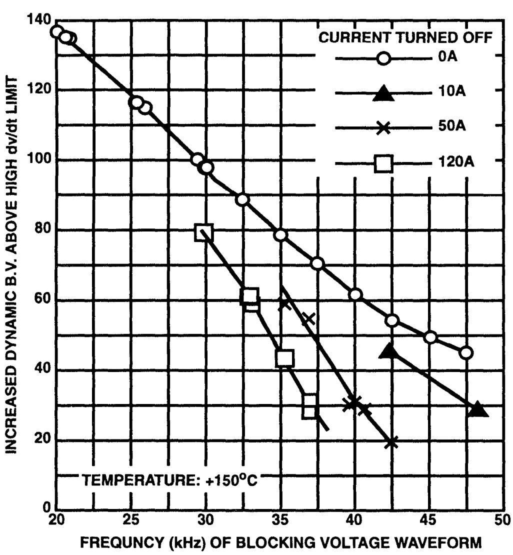


FIGURE 6.2.5. TYPICAL 75P60 600V P-MCT B. V. INCREASE ABOVE HIGH dv/dt LIMIT DUE TO "EASIER" SINEWAVE VOLTAGE dv/dt

In some circuits the MCT is paralled by the resonating capacitor. When the MCT is turned-off the voltage will typically ring up across the MCT. It might be expected that the peak MCT voltage could safely approach the DC blocking voltage since dv/dt goes to zero at the voltage peak. However, since the internal carriers have a finite lifetime the voltage blocking capability becomes a function of current turned-off and sinewave pulse width. The curves in Figure 6.2.5 show how blocking voltage inceases above the high dv/dt limit of Figure 6.2.4 for decreasing resonant frequency. Because of the current that can be remaining from the turn-off recombination tail, we have chosen to show curves and data for turn-off currents from zero to 120A, the peak rated turn-off capability of the 75P60 600V P-MCT.

In Figure 6.2.5 an MCT operated at +150°C junction temperature in which no current had to be turned off, is seen to have a dynamic breakdown voltage that increases from Figure 6.5.4's 550 volts at very high frequency to about 600 volts at 45KHz and 685 volts at 20KHz. At the other extreme the same MCT, after turning off 120A, has the same 550 volt breakdown voltage at very high frequency, a 600 volt breakdown voltage at 34KHz and a projected 670 volt breakdown voltage at 20KHz.

References - Section 9 papers 16, 28, 33, 35, 39

6.3.0 SCR Circuits

The MCT shares high surge current capability of the SCR and therefore is the ideal power switch for many thyristor applications . In addition the MCT has other superior characteristics for thyristor applications. The MCT is fabricated with thousands of turn-on cells using LSI fine geometry. This results in a device that can switch on in less than 100ns and will withstand current rise in excess of several thousand A/µs with peak current in excess of several thousand amperes. The high density of internal off-cells enables the MCT to turn off and block voltage essentially instantly. In addition the off-FETS prevent false dv/dt triggering to greater than 10,000 V/µs at +150°C operation.

Some circuit applications can effectively utilize the surge current capability of the MCT. For example, MCTs have been used to switch large capacitor banks for the purpose of generating high peak power pulses. In other applications some inverters use an auxiliary MCT to resonantly transfer load current between the main power switches of a bridge leg. Here the auxiliary MCT carries about 1.5X load current for a few microseconds during the resonant pulse. A single MCT can commutate a much higher current rated power switch.

The curve in Figure 6.3.1A shows MCT voltage drop vs current up to 2000 amperes. This data was obtained by pulsing the MCT with half sinewaves of current and measuring voltage at the current peak to avoid inductive errors. The upper current limit of the pulse test was controlled by the range of our current sensor. Note in the lower curves the good correlation with data obtained from the 400 ampere pulse curve tracer. This data was used to estimate surge current withstand capability shown in Figure 6.3.1B.

The curve in Figure 6.3.1B provides guidance in estimating allowable surge current pulses. This curve is based on a +60°C adiabatic junction temperature rise. From thyristor technology it has been established that repeated surge pulses produce micro cracks in the device die that propagate with repeated pulses to ultimately cause failure. The table in Figure 6.3.1B provides insight in estimating the number of surge pulses which will likely produce failure.

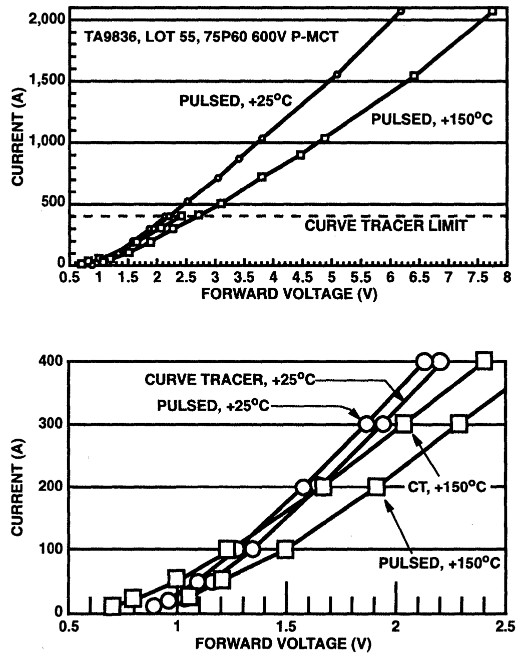
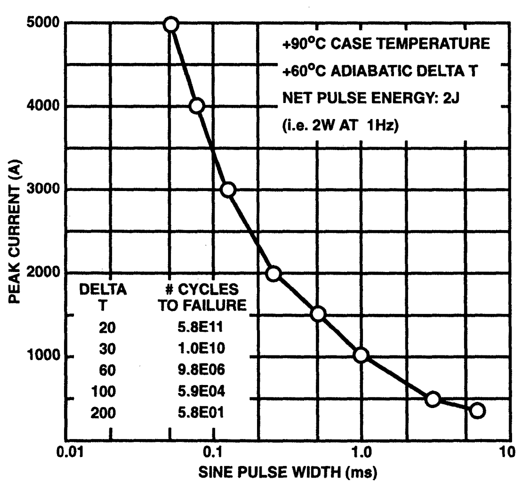


FIGURE 6.3.1A. COMPARISON OF CURVE TRACER AND PULSE VF DATA



(BASED ON 60°C JUNCTION TEMPERATURE RISE DURING THE PULSE WITH MINIMAL THERMAL SPREAD)

FIGURE 6.3.1B TYPICAL 600V P-MCT SURGE CAPABILITY

Our forward voltage drop pulse tester was also used to observe higher peak currents and very high di/dt's. Failures were observed after several pulses for 4 75P60 P-MCTs as shown below:

a) Die 48 : Ipk = 4795A di/dt = 6557A/µs

b) Die 50 : Ipk = 5328A di/dt = 6875A/µs

c) Die 54 : Ipk = 5650A di/dt = 7377A/µs

d) Die 55 : Ipk = 5902A di/dt = 8338A/µs

Although this might suggest that the allowable di/dt can be increased above the 2000A and 2000A/µs of the 75P60 600V P-MCT this does NOT indicate that all devices will survive higher than rated di/dt and surge current.

6.3.1 DC Circuit Breaker

A solid state DC circuit breaker is another application which can utilize the surge current capability and fast recovery of the MCT. In addition the control logic can be implemented using the general purpose custom MCT driver IC described in section 5.4.1. A 75 ampere instantaneous trip DC circuit breaker with 1000A interrupt capability will be described to illustrate the features and capability of the MCT driver IC and MCTs. This application utilizes developmental N-type MCTs fabricated at Harris Power R&D center (see section 8 for information on "What's ahead for MCTs"). These N-type MCTs exhibited only 10A of gated Ioff capability. This application could be as effectively implemented with the commercial P-type MCT. Its lower SOA capability compared to the N-type device would not negatively impact the application. It would, however, be necessary to slightly modify the circuit to accept opposite polarities of the P-type device.

Circuit breakers must be able to momentarily carry up to 10X to 20X rated current to handle inrush current from motor and lamp loads, for example. The N-type MCT used for this breaker application was similiar in conduction capability to the 75 ampere 75P60 MCT. These MCTs can easily carry surge current of 10X steady state rating. While the N-type MCT turn-off was limited to only 10 amperes, a second N-type MCT was used in an LC pulse circuit to commutate current in the first MCT. With this arrangement the breaker is able to interrupt fault current over 10X rated current. Of course the commutation circuit can be triggered to interrupt lower values of current. Many breakers have an inverse current/time trip characteristic which allows these momentary inrush currents to flow without tripping the breaker. That feature could be added to the instantaneous breaker. In the circuit to be described, the trip current level can be adjusted from 0.1X to over 10X steady state rated current.

Figure 6.3.2 shows the power circuit for the DC instant trip breaker. MCT Q1 carries the load current. MCT Q2, capacitor C1 and inductor L1 form the commutating circuit. The commutating capacitor C1 is maintained charged by the isolated power supply. When excess current is sensed in the load shunt the auxiliary MCT Q2 is gated on. The commutating current pulse flows from C1 through Q2, D1, and L1. During the time that diode D1 is conducting the main MCT Q1 is reversed biased. During this interval it is gated OFF. As the commutating current decreases voltage will increase

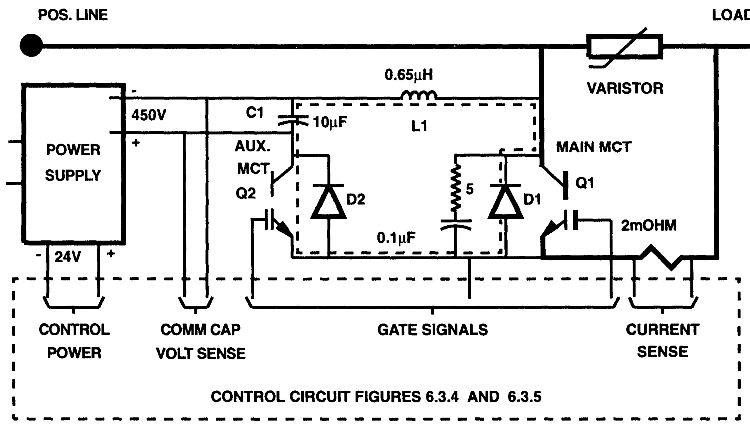


FIGURE 6.3.2. POWER CIRCUIT OF DC INSTANT TRIP BREAKER

across MCT Q1 until reactive load energy is transfered into the varistor. With this circuit arrangement the MCT can carry steady state current up to its thermal rating (~75A) and interrupt fault currents up to about 1000 amps. Because the MCT recovers within a few µs the commutating current pulse can be short, minimizing the size of the commutating capacitor. The auxiliary MCT Q2 switches the 1700A peak commutating current pulse. The MCTs are always gated OFF when they are reverse biased or carrying very low current.

Figure 6.3.3 shows a block diagram of the control circuit. Three signals (fault current, close command, commutation voltage) are processed to gate the main and auxiliary MCTs. Three LED indicators provide status indication.

The MCTs are arranged to share a common anode connection allowing the driver IC's to be electrically interconnected as shown in Figure 6.3.4. All of the active circuits needed for the instantaneous trip breaker are

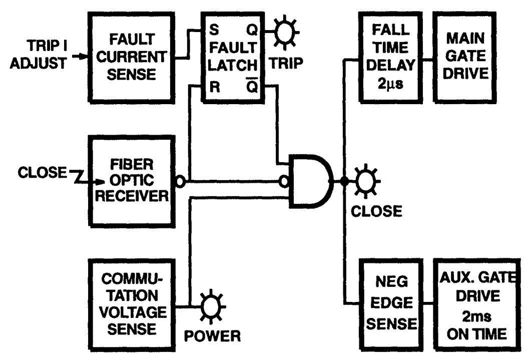


FIGURE 6.3.3. BLOCK DIAGRAM OF DC INSTANT TRIP BREAKER CONTROL

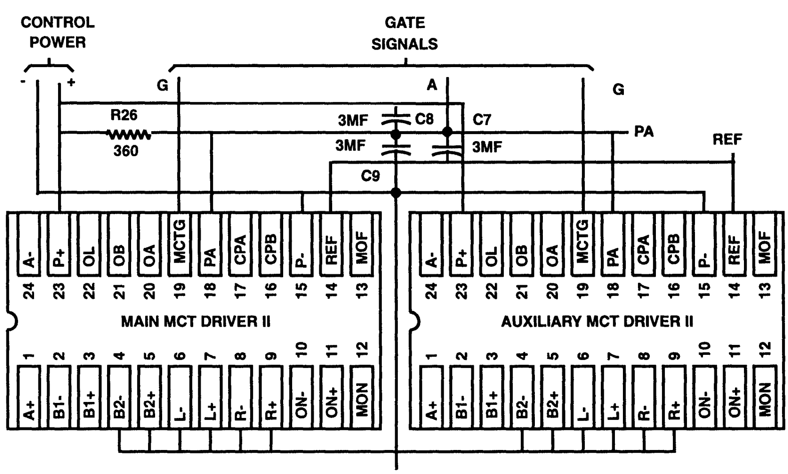


FIGURE 6.3.4. POWER SUPPLY INTERCONNECTIONS OF MCT DRIVER ICs FOR INSTANT TRIP CIRCUIT BREAKER

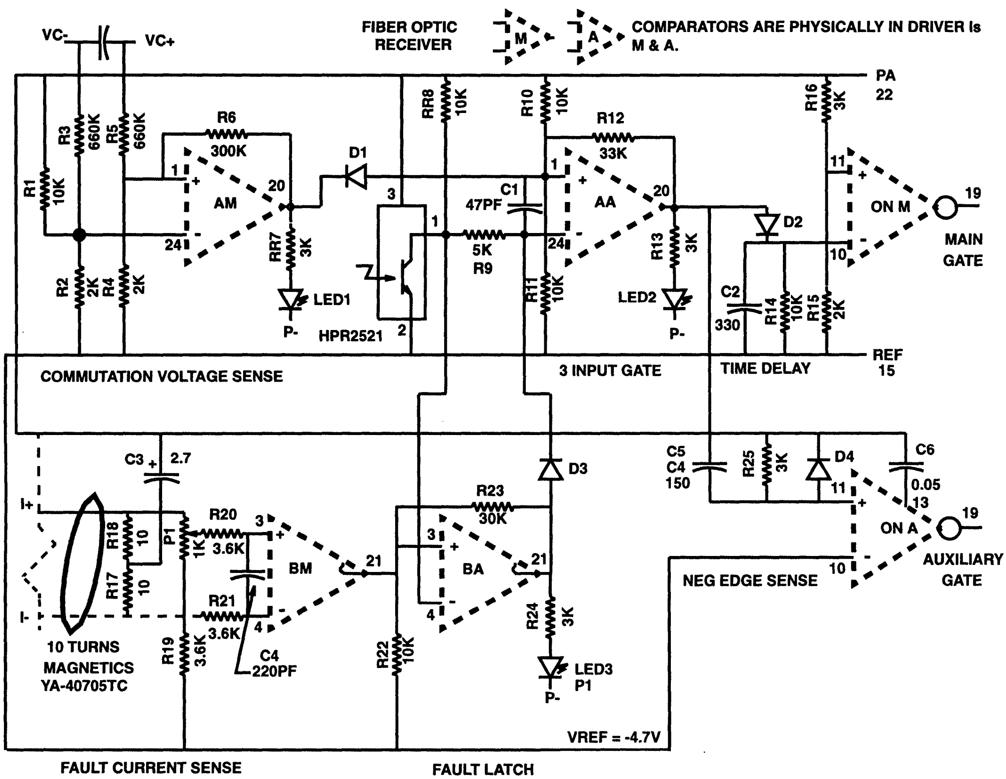


FIGURE 6.3.5. CONTROL CIRCUIT OF INSTANT TRIP BREAKER

implemented using the functions in two of the driver IC's described in section 5.4.1. Details of these control circuits are shown in Figure 6.3.5. Note that the external control circuits operate from the -4.7V reference. The Commutation Voltage Sense circuit insures that the commutation capacitor is charged to >500V before allowing the breaker to close. The Fault Current Sense circuit uses a 0.001 ohm shunt for sensing load current. The RLC filter reduces common mode noise enabling detection of the low level current signal. The OPEN/CLOSE command signal is coupled to the breaker through fiber optics. The fiber optic receiver is directly powered from the -4.7V bus. Two comparator circuits provide the latch function and the 3 input gate function. LED's are driven by the comparator outputs to show breaker status. The two ON-channels provide gate signals for the two MCTs. While this breaker provides instantaneous trip on detecting over current, additional circuits could be added to provide an inverse current-time trip response.

The waveforms in Figure 6.3.6 show operation of the breaker with an inductive load. When the breaker is closed its voltage drops to approximately 1.5V and the current increases linearly. When the load current reaches 800A, the commutating circuit is gated to produce a 1700A commutating current

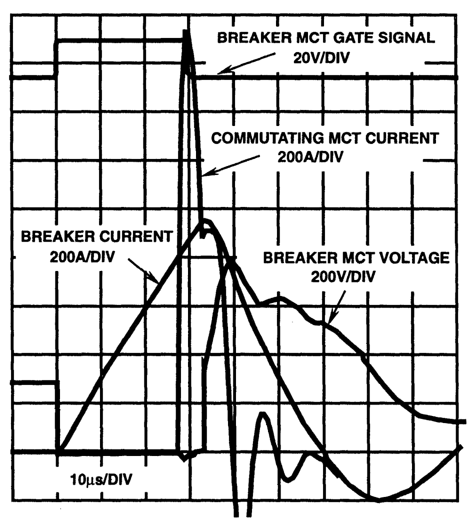


FIGURE 6.3.6. 1400V, 0.2cm^2 N-MCT SHOWN INTERUPTING 920A WITH 500V VARISTOR CLAMPED OVERSHOOT OF 300V BUS

pulse. The main MCT is gated OFF after a 2.5μs delay which insures that the commutating current will exceed the load current thereby reverse biasing the main MCT. When the commutating current becomes less than the load current, the main MCT blocks voltage and the load current decreases as inductive energy is transfered to the varistor clamp.

The particular usefulness of this driver IC lies in simplifying the implementation of control circuits that can be combined with the gate signal which is ohmically connected to the MCT. While MCTs have turn-off capability they are nearly ideal thyristors and can be used to great advantage in thyristor circuits.

6.4.0 AC Switch Circuits

The reverse blocking voltage rating for the MCT is 5 volts. Thus it is necessary to utilize a series connected diode to provide reverse blocking voltage capability. The circuit in Figure 6.4.1 shows how two MCTs and two diodes can be arranged to form an AC switch function. In this arrangement a single drive circuit can be used to gate both MCTs. If it is desired to sense current through the switch, resistor R1 provides a rectified current signal that can be used for indication and/or control of the switch.

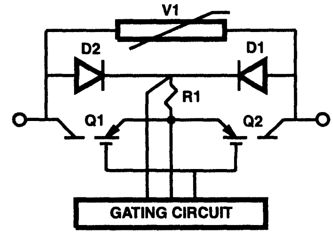


FIGURE 6.4.1. AC SWITCH USING TWO MCTs WITH COMMON GATE CIRCUIT

In most circuits the load being switched will be inductive. Thus some type of snubber may be necessary to control overshoot voltage which is developed when the MCTs are gated OFF. If the MCTs are gated OFF only at current zero, then the snubber may not be needed. When the switch is ON and the current goes through zero, a turn-on transient volt-

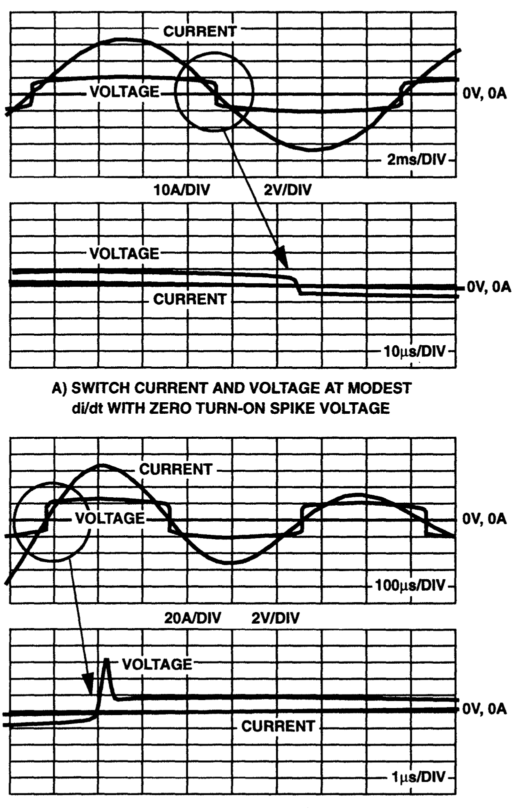


FIGURE 6.4.2. EFFECT OF di/dt ON TURN-ON VOLTAGE

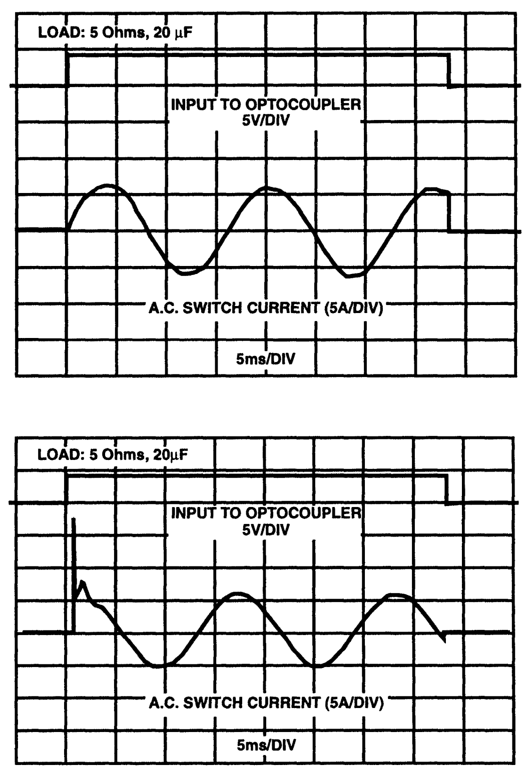


FIGURE 6.4.3. MCT AC SWITCH/BREAKER
TOP: Closing at Zero, Opening Near Mid-Cycle
BOTTOM: Closing at Mid-Cycle, Opeining Near Zero

age develops across the switch as discussed in section 6.2.3. The waveforms in Figure 6.4.2 illustrate this turn-on transient for two different values of di/dt at current zero crossing. When the switch is used to switch low frequency current (60Hz for example), the turn-on transient voltage is small and probably not of consequence.

When the switch is used with non-unity power factor loads current surges may occur. The waveforms in Figure 6.4.3 show a leading power factor (20µF/5 ohm) load being switched. When closed at voltage zero crossing (top waveform) no transient occurs. However, when closed mid-cycle (lower waveform) a relatively large inrush current occurs. Thus it is possible with some sensing to close the switch at voltage zero to eliminate leading power factor current and to open the switch at current zero to eliminate lagging power factor voltage transients.

When the switch is part of a static circuit breaker it can be closed at voltage zero crossing; however, the control circuit must typically allow normal load inrush current to flow without tripping. When a fault current is detected the switch can be opened rapidly, limiting fault current, but requiring the switch to have I-off capability and inductive energy absorbtion capability (varistor). If the anticipated fault current does not exceed the surge rating (1000's of amps per MCT) of the static switch then interruption can be delayed to current zero crossing, minimizing the need for I-off capability and inductive energy absorbtion capability.

6.5.0 Complementary Circuits

The 75P60 MCT is a P-type device. As such it has terminal polarities oppposite to N-type devices. Therefore, the opportunity exists to use the P-MCT in combination with N-type power devices such as N-IGBTs or N-FETs. The P-MCT provides superior current rating, speed and SOA compared to P-IGBTs, for example.. While N and P devices have different characteristics their use in combination provides certain advantages.

Figure 6.5.1 illustrates an AC switch circuit using a P-MCT and an N-IGBT. Resistor R1 provides a single current signal to the gate circuit, should it be required to initiate or inhibit switch operation. The varistor V1 provides a means of limiting transient voltage across the opening switch.

Figure 6.5.2 illustrates a DC bridge leg using a P-MCT and N-IGBT. This combination allows the use of a single gate circuit and power supply for each bridge leg. The gate circuit must provide appropriate gating delays to avoid short circuit current through the two power devices. Resistor R1 provides a single current signal to the gate circuit, should it be required to initiate or inhibit switch operation.

Hopefully, it will not be too long before N-MCTs are also ready for the market.

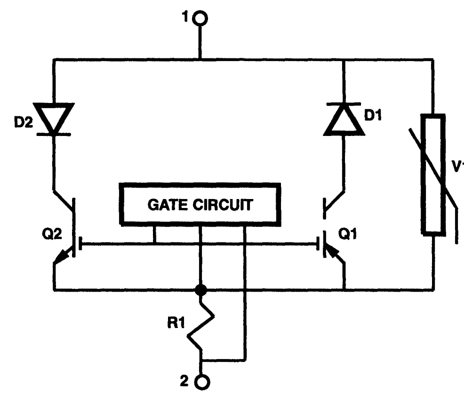


FIGURE 6.5.1. AC SWITCH USING P-MCT AND N-IGBT

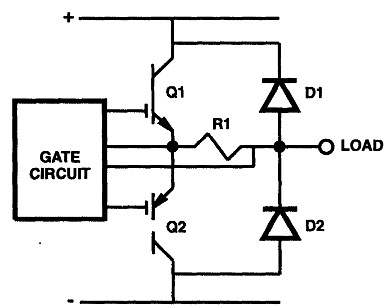


FIGURE 6.5.2. DC BRIDGE LEG USNG P-MCT AND N-IGBT

Comparison on MCT and IGBT

How does the MCT compare to other Power Switches? Where is best used? This chapter provides some general comparisons. The particular requirements of a specific circuit may heavily influence the comparison in any application.

Both IGBTs and MCTs are insulated gate, field controlled switching devices with junction temperature ratings of +150°C. Comparison of the IGBT and MCT is most pertinent as both are merged bipolar/MOS structures and are applicable to power switching circuits requiring 600 Volts or higher Switch ratings. Both are useful at higher switching frequency than is generally practical with power darlingtons. By contrast, the characteristics or Power MOS transistors (majority carrier devices) sharply differentiate their preferred applications.

In high power circuits the importance of efficiency can be most critical. While efficiency is important in minimizing the cost of energy, in high power circuits the removal of heat from only a few points of efficiency loss has a significant impact on the size and nature of the system packaging. Conduction and switching losses are therefore the first point of comparison.

Conduction Voltage Drop

The single most prominent feature of the MCT is that of low conduction drop, one third to one half that of the IGBT. This is illustrated in Figure 2.0.2 and Figure 2.0.3. Furthermore, the MCT conduction drop is diode like, increasing only modestly at very high peak currents. Use in circuits with high peak currents will not significantly worsen the average conduction loss. Because the MCT is a double injection device (with both N and P emitters), conduction drop does not increase as rapidly with the blocking voltage rating as with IGBTs. As MOS gated switches are developed above 1000 Volts, MCT technology will be even more advantageous.

The conduction loss (Rdson) of Power MOS transistors is an exponential function of the blocking voltage rating. At the 600 Volt level, the conduction drop per unit area of silicon is more than a factor of ten higher than the MCT. High voltage MOS transistors are competitive only in low power applications. However, Power MOS transistors can offer comparatively low conduction losses in lower voltage systems. If voltage drop is desirable at any cost, it is possible to operate Power MOS transistors at very low current density at less than the junction voltage drop of an MCT.

Switching - Turn ON

Turn on in the MCT is initiated by the gate signal but is completed regeneratively as in an SCR. The MCT turn on is fast and handles high di/dt and peak current with low turn on loss. The recommended gate turn on drive is stiff to ensure all cells share the turn on power loss uniformly.

Turn on in IGBTs is often intentionally slowed to control the reverse recovery of the free wheeling diode common to inductive switching circuits. The IGBT can be used to limit high peak recovery current in the diode, but at a sacrifice in turn on speed and loss. With the MCT, turn on voltage drop is not drive circuit adjustable. If reduction in rectifier peak recovery current is required, small saturating inductors may be used in the recovery circuit.

Turn on in the MOS transistor can be so much faster than for either the IGBT or the MCT that in comparable applications, MOS transistor switching losses would be negligible compared to conduction loss.

Switching - Turn OFF

The best of today's IGBTs can provide faster switching and lower loss per switch cycle than the P MCT, roughly by a factor of two, in clamped inductive switch circuits. Power MOS transistor turn off loss is the lowest among the three devices by a large margin.

Total Losses

From the above, it is clear that the device choice for lowest total loss is dependent on the relative proportion of conduction to turn off loss in the circuit. Some general guidelines are indicated in the section below on Applications.

Turn Off Safe Operating Voltage (SOA)

When turning off an inductive load, a switch circuit must sustain a voltage higher than the load driving voltage. Left to itself, the switch must sustain this voltage while conducting full current. The turn off safe operating area describes a locus of maximum permissible combinations of voltage and current across the switch during turn off which will not cause improper operation of the switch. For the P MCT, the full switching current is sustainable at 50% to 60% of the breakdown voltage rating, as are lower currents at higher percentages of breakdown voltage. Capacitive snubbers can be used to shape the combination of current and voltage seen by the MCT at switching voltages above 50% BV.

The IGBT provides better turn off Safe Operating Area than the P Type MCT. IGBTs are generally rated for switching at 80% of the static blocking device rating.

Applications

The resonant, soft switching, or zero current switching circuit configurations most often offer the lowest overall system loss. As these circuits avoid or minimize switch turn off loss, but do usually involve higher peak switch currents, the MCT will be the preferred device in such circuits, at any frequency. For instance, MCTs have been reported in the literature operating at 80KHz switching rate in 10KW inverters in this class of circuit. In these circuits turn off SOA is not a significant requirement.

Active inductive switching from full current, the so called "Hard Switch" or PWM Circuits, may favor the IGBT, particularly at switching frequencies above 10KHz. In these circuits the lower switching loss of the IGBT can outweigh the lower conduction loss of the MCT.

In PWM circuits, inductive switching usually involves clamping the inductive voltage rise to some sink, such as the DC Bus. The higher Turn Off SOA voltage of the 600 Volt IGBT, 480 Volts, may make it the preferred solution for DC bus voltages above 300 Volts to 400 Volts. With P Type MCTs, & higher voltage rated device or capacitive snubbers are reguired to allow operation at a comparable bus voltage.

The IGBT can provide fault current limiting for a few microseconds in PWM circuits, allowing for the orderly shut down of the circuit from the gate drive. For the MCT, no such mechanism is available. In resonant circuits, MCT shut down can occur at the next current zero, or low current point.

Pulse discharge circuits will generally favor the MCT, due to fast turn on speed and high peak current capability at low voltage drop.

Power MOS transistors may be the only practical power switch at a switching freguency above 50KHz in hard switch circuits or 100KHz in soft switch circuits.

Outlook, What's Ahead for MCTs

8.0 Future MCT Developments

8.1 More "Generation 1" P-MCTs

The first Harris MCT products are P-MCTs of 600V and, shortly, 1000V in a die size that can be packaged in a TO-218 or TO-247 5-pin plastic package. This die size results in about a 75A RMS rating and about a 120A turn-off current capability at +150°C. Harris plans call for an MCT of about half this size and, given enough interest, an even smaller die size that can be packaged in a TO-220 package.

Development efforts include wider ranges of voltage rating - first asymmetric MCTs down to perhaps as low as 200V and as high as 1600V and, later, high voltage MCTs for what are now typically thyristor and GTO circuits. Such high voltage P-MCTs have been described in several papers including reference 8.1. Figure 8.1.1 and Figure 8.1.2 are reproduced from that paper to illustrate our initial capability (in R&D devices) of 2500V.

8.2 Generation 2 P-MCTs

Generation 2 P-MCTs have been made at Harris' Power R&D Center that push the present P-MCT twice as close to the diode in the physics-dominated trade-off between breakdown voltage vs forward drop vs switching speed. Details of design and process change are, of course, proprietary but the bottom line is that one can expect a generation 2 P-MCT to have an additional 100 volts in SOA and to have between 2 and 3 times lower turn-off losses. Figure 8.2.1 shows some recent turn-off energy measurements on an R&D generation 2 P-MCT.

Figure 8.2.2 is a snapshot comparing switching losses at +75°C and +150°C for snubbers from 0μF to 1μF and currents to 120A for a typical generation 1 600V P-MCT compared to an early generation 2 600V P-MCT lot of the same breakdown voltage and similar die size. Unsnubbered and at very low snubber value the improvement is more than a factor of 2. At modest snubber value (0.05μF an 0.1μF) it is closer to a factor of 4. For larger snubbers and, obviously, for most resonant circuits the improvement is even greater.

8.3 N-MCT Development

N-MCT versions of almost all of our P-MCTs have been fabricated at Harris Power R&D to analyze the potential for a commercial product. At this time we have produced and delivered N-MCTs for various applications, all of which required little or no turn-off capability. This has included 1400V devices for 1000A, 1000V capacitor discharge circuits and 600V devices for zero current soft switched circuits with peak currents of about 800A.

As our P-MCTs have increased in turn-off capability from one or two hundred amperes per centimeter squared to more than 400A/cm^2 our N-MCTs have kept pace at about 1/2 to 1/3 of that value and now can be rated at about 150A/cm2 in peak turn-off current density at +150°C. Note that with the MCTs low forward drop that this is less than the device's RMS current rating. This lack of peak turn-off capability has kept us from as aggressively pursuing the N-MCT.

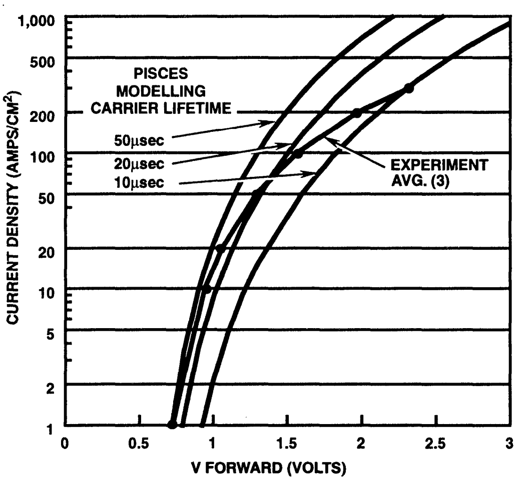


FIGURE 8.1.1. MEASURED vs MODELED FORWARD VOLTAGE (1cm^2 Active Area, >3000V Asymmetric P-MCT)

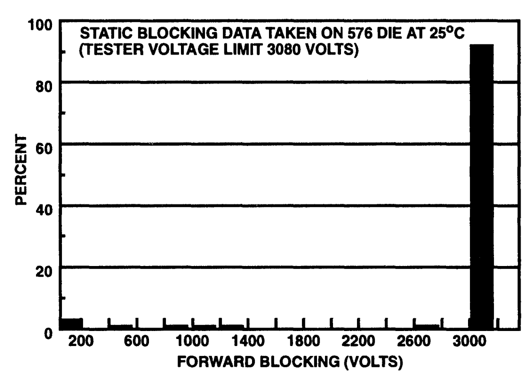


FIGURE 8.1.2. FORWARD BLOCKING DISTRIBUTION FOR A RECENT HV MCT LOT

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APPLICATION NOTES

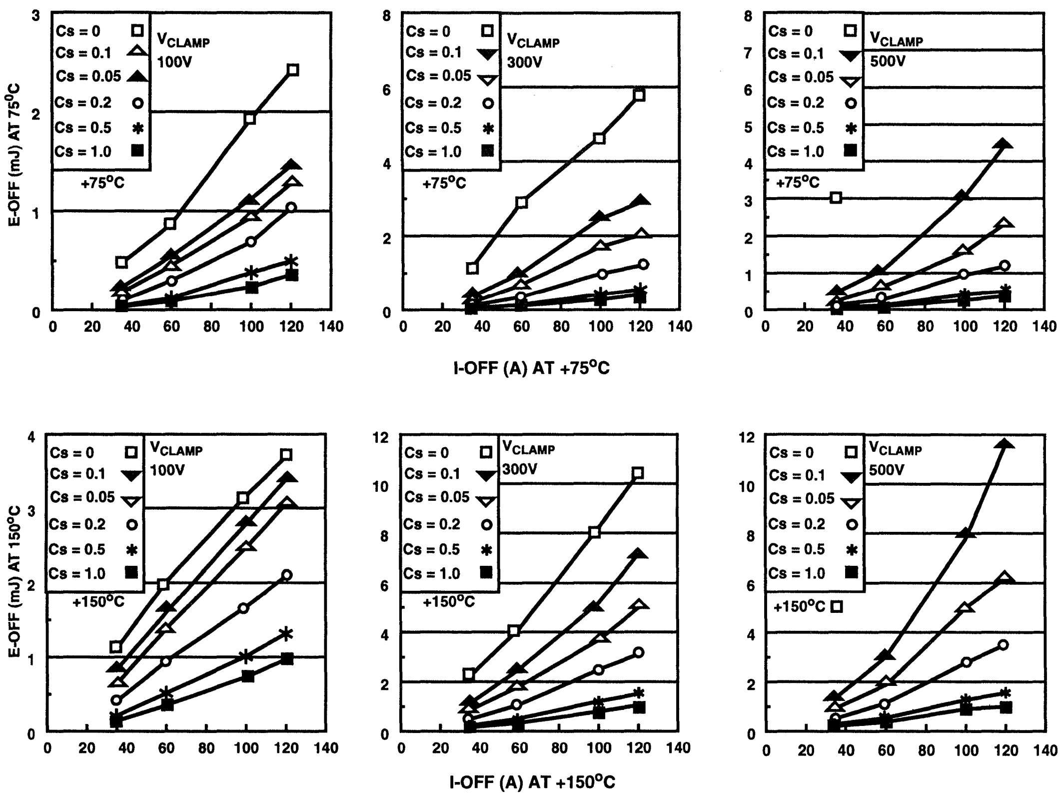

FIGURE 8.2.1. TYPICAL GENERATION 2 600V PMCT TURN-OFF ENERGY AS A FUNCTION OF SNUBBER CAP. AND CURRENT

However, as cell size and geometries become finer, turn-off capability will improve correspondingly and N-MCTs will be produced that, with their 2 times lower switching loss and 30% higher (more at high voltage) SOA, will displace P-MCTs and those N-IGBT's that our present P-MCTs cannot replace.

8.4 MCT Driver IC

In section 5 and section 6 an MCT driver IC was used to gate an MCT and, with some of its added functions, to implement an autonomous circuit breaker. The driver IC referred to was produced using a standard Harris process on that process' production line. From our own experience we have found that IC extremely valuable. Referring back to section 5, the driver IC has a voltage range of -12V to +35V with respect to the "A" terminal and has an output impedance in the neighborhood of 2 ohms. The inputs are all comparators with a wide dynamic range. The IC supports all types of OPTO-couplers both as receivers and senders and has a 4.7V regulated supply to power IC's if more "smarts" are necessary at the device. There is an on-board charge pump and an on-board zener that, within limits, allows one to power the IC using a dropping resistor from the MCT cathode supply. Our IC also includes latched and unlatched channels as well as minimum on-time and minimum off-times that can be set with external capacitors. Our present die is less than 200 mils on a side and for full function needs 24 pins. As just a driver, however, 6 or 7 pins are sufficient and we have looked at some MCT driver ICs in 7 pin TO-218 packages.

8.5 MCT Modules

MCT modules of up to 12 parallel devices, each of.4 cm2 active area, have been built and tested for various development contracts. Currently Harris is assessing 4 MCT & 2 diode and 6 MCT modules in a compact plastic module as well as industry outline modules in various current ratings. Harris will consider providing similar modules to other customers.

Although MCTs parallel reasonably well, their low forward drop and high current capability require one to be careful in selecting devices of the same forward drop and similar turn-off time and then to be very symmetric with stray impedance.

Some of our development modules include gate drive circuitry.

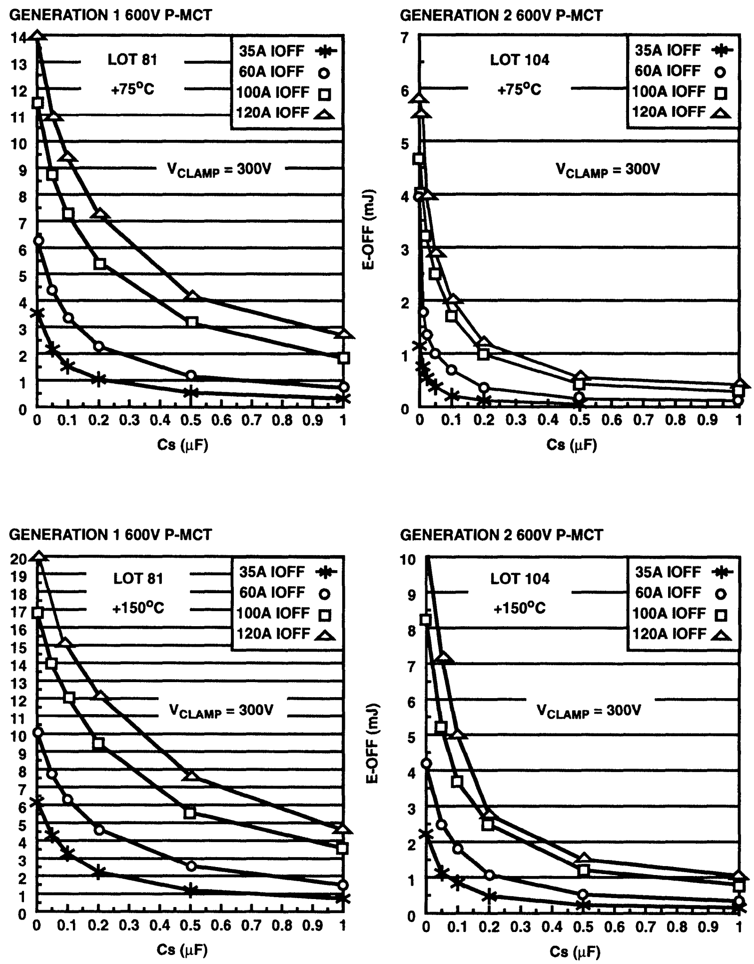

FIGURE 8.2.2. GENERATION 2 600V PMCT TURN-OFF IMPROVEMENT

8.6 Development Timetable

In summary, P-MCTs will also improve in switching capability in both SOA and turn-off time, bettering N-IGBTs in speed and turn-off loss and being at less of a disadvantage in hard switched SOA.

N-MCTs will begin to become available but with about half the peak turn-off current capability of P-MCTs. However, both P-MCTs and N-MCTs will be improving in that characteristic as improved process capability allows denser off-FET channel structure.

MCTs will go to high currents paralleled in modules of up to hundreds of amperes. These modules will first be dumb modules but will later contain some smarts with driver ICs such as that described in section 8.4 above.

The timetable for these developments depends on resources.

References

[1]. V.A.K. Temple et al, "Megawatt MOS Controlled Thyristor for High Voltage Power Circuits", IEEE PESC, Toledo, Spain, June 29-July 3, 1992, pp 1018-1025 (92CH3163-3)

MCT Reference List and Bibliography

The following is a list of references which is applicable to MCT technology. It is listed chronologically and a table sorting the references by topic is provided at the end. A reference may appear in more than one topic category, not all topics have references associated with them to date.

[1] V. Temple, "MOS Controlled Thyristor," IEDM Technical Digest, Abstract 10.7, pp. 282-285, (1984)

[2] M. Stoisiek, H. Strack, "MOS GTO A Turn Off Thyristor with MOS Controlled Emitter Shorts," IEDM Technical Digest, pp. 158-161 (1985)

[3] V. Temple and D. Pattanayak, "On-State Characteristics of the MOS Controlled Thyristor (MCT)," 44th Annual Device Research Conference, Amherst Massachusetts, June (1986)

[4] V. Temple "MOS-Controlled Thyristors a New Class of Power Devices," IEEE Transactions on Electron Devices, vol. 33, No. 10, pp. 1609-1618, October (1986)

[5] V. Temple and W. Tantraporn, "Effect of Temperature and Load on MCT Turn-Off Capability," IEEE International Electron Devices Meeting Digest, Abstract 5.5, pp. 118-121 (1986)

[6] M. Stoisiek, D. Theis "Turn-On Principles of the MOS-GTO," IEEE Transactions on Power Electronics, Vol. PE-2, No. 4, pp. 362-366, October (1987)

[7] V. Temple, "Power Device Evolution and the MOS-Controlled Thyristor," Power Conversion & Intelligent Motion, pp. 23-29, November (1987)

[8] M. Stoisiek, M. Beyer, W. Kiffe, H. Schultz et al "A Large Area MOS-GTO with Wafer Repair Technique," IEEE International Electron Devices Meeting Digest, Abstract 29.3, pp. 666-669 (1987)

[9] F. Goodenough "MOS Controlled Thyristor - A New Breed of Power Semiconductor," Electronic Design, pp.57-66, November (1988)

[10] L. Bovino, S. Schneider, J. Wright "The MOS Controlled Thyristor (MCT) as an On-Off Capacitor Bank Switch," Proceedings of the 8th Pulse Power Conference, June (1989)

[11] V. Temple, "Advances in MOS Controlled Thyristor Technology and Capability," Proceedings of Power Conversion and Intelligent Motion Conference, pp. 544-554 (1989)

[12] R. King, A. Radun, H. Chang, J. Rulison, "Numerical and Experimental Comparisons of Power Darlington, IGBT, and MCT Device as a Switch for Adjustable Speed PWM Inverter Drive Applications'" Proceedings of Power Conversion and Intelligent Motion Conference, pp. 238-248 (1989)

[13] S. Sul, F. Profumo, G. Cho, T. Lipo "MCTs and IGBTs: a Comparison of Performance in Power Electronic Circuits," 1989 IEEE Power Electronics Specialists Annual Conference, pp. 163-169 (1989)

[14] J. Hudgins, D. Blanco, S. Menhart, W. Portnoy "Comparison of the MCT and MOSFET for a High Frequency Inverter," Conference Record of 1989 IEEE Industry Applications Society Annual Meeting, pp. 1255-1259 (1989)

[15] A. Aemmer, F. Bauer, J. Burgler, W. Fichtner et al, "Multi-dimensional Simulation of MCT Structures," IEEE ISPSD 90 Tecnical Digest, pp. 20-25, (1990)

[16] F. Jones, C. Kerfoot, R. Kemerer, C. Carter "Ten Kilowatt Self Commutated Resonant Inverter using MOS Controlled Thyristors," Applied Power Electronics Conference, pp. 659-667, (1990)

[17] R. Pastore, C. Braun, M. Weiner, S. Schneider "Developmental MOS Controlled Thyristors (MCT) Behavior," IEEE 19th Power Modulator Symposium, pp. 391-399 (1990)

[18] H. Chang, A. Radun "Performance of 500V, 450A Parallel MOS-Controlled Thyristors (MCTs) in a Resonant DC-Link Circuit," Conference Record of 1990 IEEE Industry Applications Society Annual Meeting, pp. 1613-1617 (1990)

[19] C. Braun "Circuit Level Modeling of MOS Controlled Thyristors," IEEE 19th Power Modulator Symposium (1990)

[20] T. Jahns, R. De Doncker, J. Wilson, V. Temple, D. Waters "Circuit Utilization Characteristics of MOS-Controlled Thyristors," IEEE Transactions on Industry Applications, Vol 27, No. 3, pp. 589-597, May/June (1991)

[21] R. Pastore, C. Braun, M. Weiner, S. Schneider "Characterization of 3000 Volt MOS Controlled Thyristors," Proceedings of the 8th IEEE Pulse Power Conference, pp. 196-199, June (1991)

[22] C. Braun, R. Pastore "Progress Towards an MCT Based 100+ KW High Frequency Inverter," 8th IEEE Pulse Power Conference, June (1991)

[23] F. Bauer, E. Halder, K. Hafmann, H. Haddon et al "Design Aspects of MOS-Controlled Thyristor Elements: Technology, Simulation, and Experimental Results," IEEE Transactions on Electron Devices, vol. 38, No. 7, pp. 1605-1611, July (1991)

[24] Q. Huang, G. Amaratunga "Analysis of N-Channel MOS-Controlled Thyristors," IEEE Transactions on Electron Devices, vol. 38, No. 7, pp. 1612-1618, July (1991)

[25] F. Bauer, H. Haddon, T. Stockmeier, W. Fichtner, R. Vuilleumier, J. Moret "Optimization of Cathode Structures for Improved Performance of MOS Controlled Thyristors (MCT)," Joint Proceedings of the European Conference on Power Electronics and Applications and the Symposium on Materials and Devices for Power Electronics, MADEP 91, pp. 270-275, (1991)

[26] W. Fichtner, J. Burgler, H. Dettmer, H. Lendenmann, S. Muller "Turn Off Behavior of Structured MCT Cells," Joint Proceedings of the European Conference on Power Electronics and Applications and the Symposium on Materials and Devices for Power Electronics, MADEP 91, pp. 258-261, (1991)

[27] C. Ronsisvalle, G. Ferla, P. Zani "High Power MOS Controlled Thyristor Using the Parallel Contacting Technology for Devices on the Same Wafer," Joint Proceedings of the European Conference on Power Electronics and Applications and the Symposium on Materials and Devices for Power Electronics, MADEP 91, pp. 267-269, (1991)

[28] R. De Doncker, O. Demirci, S. Arthur, V. Temple, "Characteristics of GTO's and High Voltage MCT's in High Power Soft Switching Converters," Conference Record of 1991 IEEE Industry Applications Society Annual Meeting, pp. 1539-1545 (1991)

[29] H. Lendenmann, H. Dettmer, W. Fichtner, B. Baliga et al, "Switching Behavior and Current Handling Capability of MCT-IGBT Cell Ensembles", IEEE International Electron Devices Meeting Digest, pp. 149-152 (1991)

[30] S. Momota, M. Otsuki, K. Sakuri "Double Gate MOS Device Having IGBT and MCT Performances," Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, pp. 22-27, May (1992)

[31] D. Czarkowski, M. Kazimierczuk "Expression for I-V Forward Characteristic of MCTs," Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, pp. 22-27, May (1992)

[32] M. Stoisiek, K. Oppermann, R. Stengl "A 400 A/2000 V MOS-GTO with Improved Cell Design," IEEE Transactions on Electron Devices, vol. 39, No. 6, pp. 1521-1528, June (1992)

[33] R. De Doncker, T. Jahns, A. Radun, D. Watrous, V. Temple, "Characteristics of MOS-Controlled Thyristors under Zero Voltage Soft-Switching Conditions," IEEE Transactions on Industry Applications, Vol 28, No. 2, pp. 387-394, March/April (1992)

[34] B. Bose "Evaluation of Modern Power Semiconductor Devices and Future Trends of Converters," IEEE Transactions on Industry Applications, Vol 28, No. 2, pp. 403-413, March/April (1992)

[35] C. Braun, J. Carter "Progress Towards a MCT Based High Frequency Capacitor Power Supply," Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, May (1992)

[36] F. Bauer, T. Stockmeier, H. Lendenmann, H. Dettmer, W. Fichtner "Static and Dynamic Characteristics of High Voltage (3.5 kV) IGBT and MCT Devices," Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, pp. 22-27, May (1992)

[37] K. Khan Afridi, Parallel Operation and Failure Mechanisms of MOS Controlled Thyristors, Masters Thesis, Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, June (1992)

[38] V. Temple, S. Arthur, D. Watrous, R. De Doncker, H. Mehta "Megawatt MOS Controlled Thyristor for High Voltage Power Circuits," 1992 IEEE Power Electronics Specialists Conference, pp. 1018-1025, June (1992)

[39] S. Arthur, V. Temple, D. Watrous, "Forward Blocking Comparison of P and N MCTs," accepted for publication in Conference Record of 1992 IEEE Industry Applications Society Annual Meeting, Oct. (1992)

TOPICS	REFERENCE #
Device Physics & Design	1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 15, 23, 24, 25, 26, 27, 29, 30, 31, 32, 39
Hard Switching Applications	12
Soft Switching Applications	16, 28, 33, 35, 39
Device Characterization & Series/Parallel Operation	17, 18, 20, 21, 22, 37
AC Applications	
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Comparisons With Other Power Devices	12, 13, 14, 34, 36
SPICE Models of the MCT	19, 37
Miscellaneous	10, 38

Understanding Power MOSFETs

Author: Tom McNulty

Power MOSFETs (**M**etal **O**xide **S**emiconductor, **F**ield **E**ffect **T**ransistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n characteristic.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

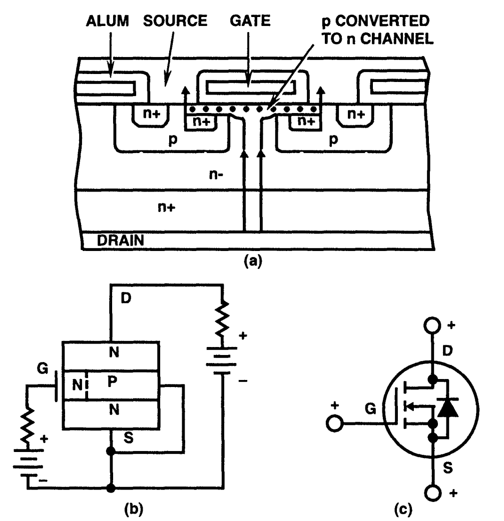


FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFETs CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS.

Structure

Harris Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_N, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

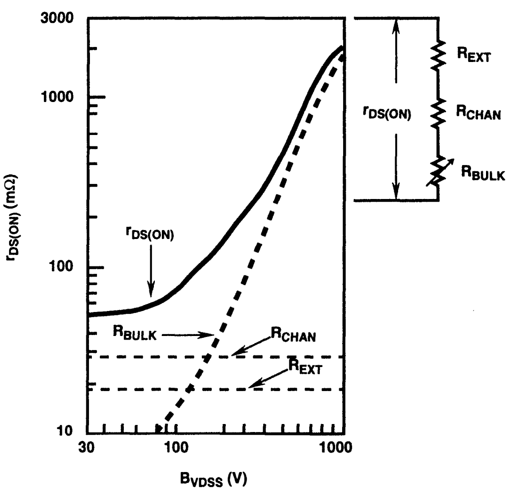


FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE ($r_{DS(ON)}$ OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS)

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two players, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT}. Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK}. Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (See Figure 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

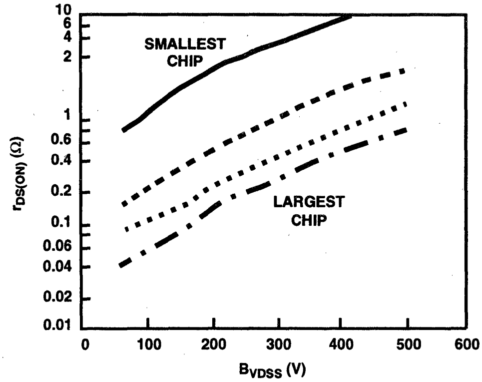


FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES, & VOLTAGE HANDLING CAPABILITY INCREASES

Effects of Temperature

The high operating temperatures of bipolar transistors area frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

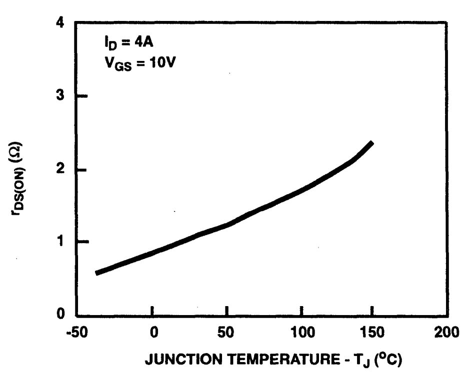


FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

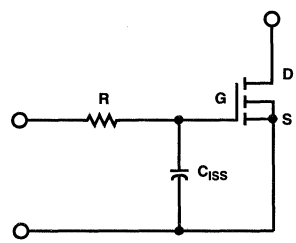


FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20W/□. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (gs). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{GS} level required to operate a MOSFET, note, from Figure 6, that the device is not turned on (no drain current flows) unless V_{GS} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an apprecia-ble increase in drain current can be expected. Generally V_{GS} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of l0V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

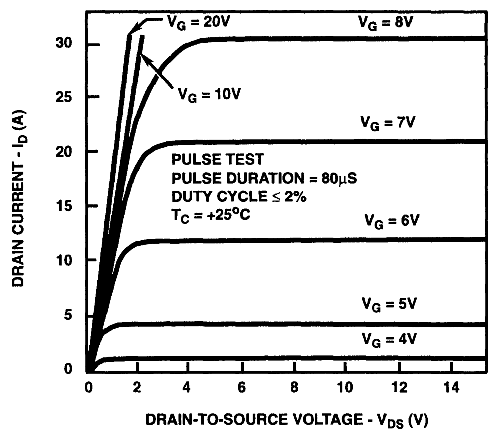


FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

Switching Waveforms Of The L²FET: A 5 Volt Gate-Drive Power MOSFET

Author: C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power MOSFET devices called Logic Level FETs (L²FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L²FET over the 10V MOSFET are demonstrated and discussed

Background

A new series of power MOSFET devices called Logic Level FETs, or L²FETs, is compatible with the 5V power supply used for logic circuitry. L²FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L²FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L²FET Characteristics Compared to Standard Types - A Brief Review

Thirty-two different power MOSFETs of the L²FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L²FET product currently available is limited to n-channel devices handling 200V or less, with 15A ratings or less.)

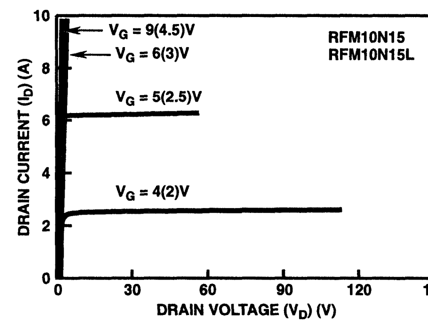


FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES

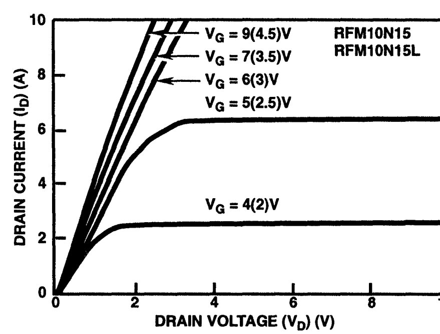


FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L²FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L²FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that RON has not been sacrificed in the L²FET. Figure 3 is the transfer characteristic comparison for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The threshold voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

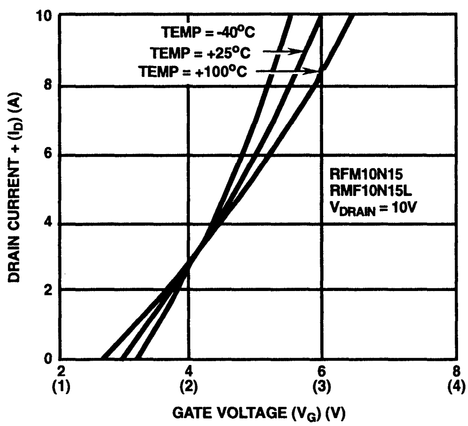


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

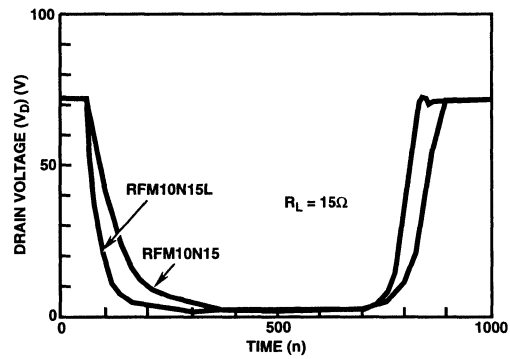
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak R_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The L^2FET is faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.

4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

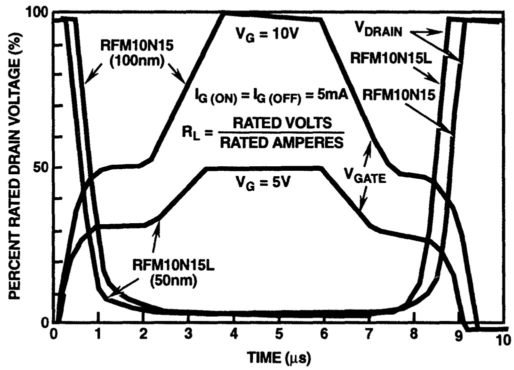


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

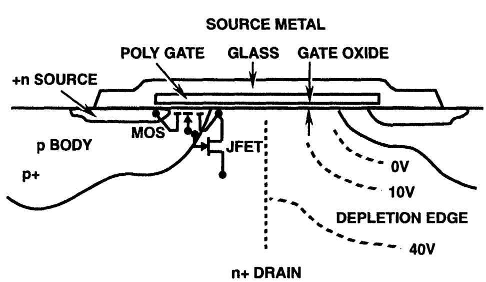


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

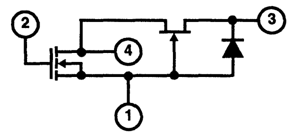


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

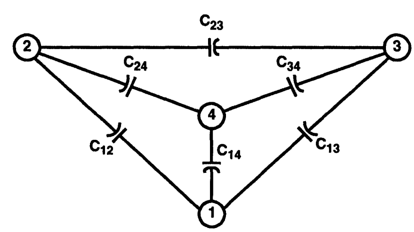


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times R_{DS}(ON).

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad \text{(EQ. 1)}$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C_{12} during the constant gate voltage plateau.

Drain Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad \text{(EQ. 2)}$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS(ON)}$.)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET sour-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad \text{(EQ. 3)}$$

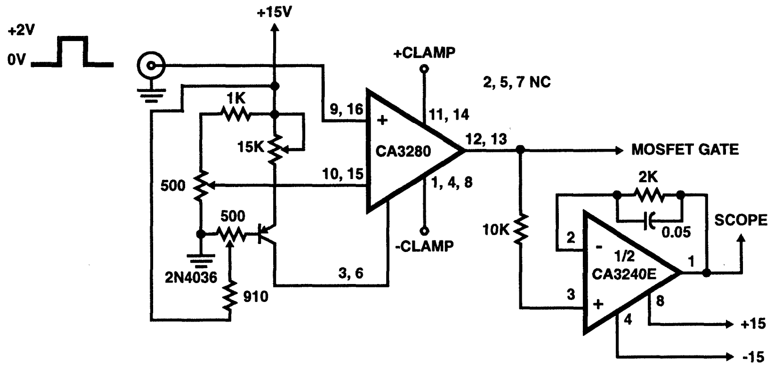


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Harris CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads parallel to the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50μs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several μs exists at the +10V level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(A) is the 3V signal to the CA3280. Figure 10(B) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(C) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(D) is a piece wise linear approximation of Figure 10(C). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100μs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

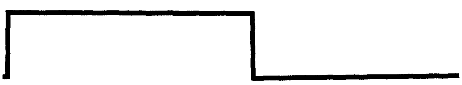


FIGURE 10A. 3V SIGNAL TO THE CA3280

FIGURE 10B. POWER MOSFET GATE CURRENT

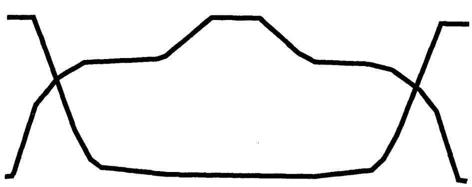


FIGURE 10C. GATE AND DRAIN VOLTAGE

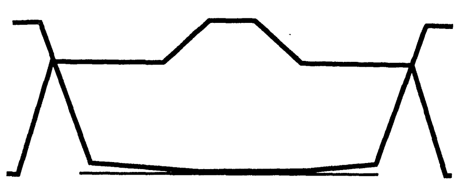


FIGURE 10D. PIECE WISE LINEAR APPROXIMATION OF FIGURE 10C

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(C), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

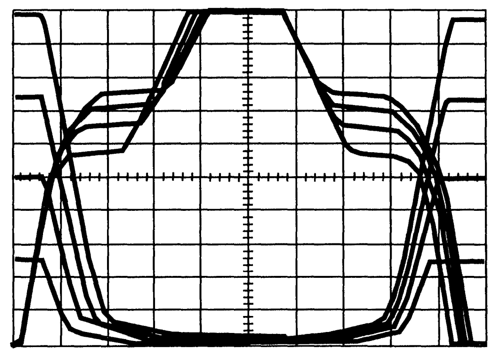


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(C) WITH DRAIN SUPPLY VOLTAGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2µA for the device of Figure 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

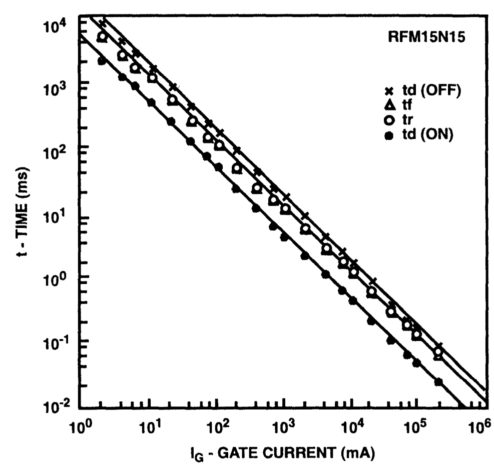


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2µA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5, 8.5, . . . 1.5, 0.5 volts. Call these segments 11, 12,... 19, 20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage waveform applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(A), (B), and (C) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(C).

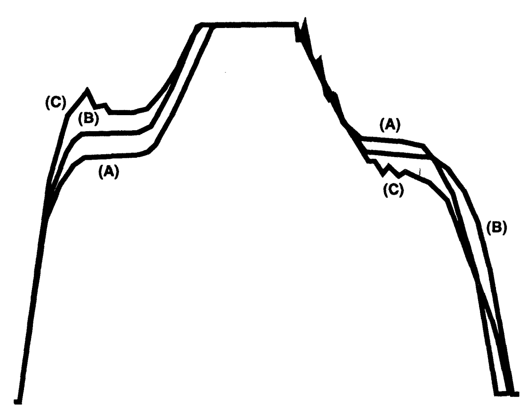


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF

GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

[1] "Power MOSFET Switching Waveforms - A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.

[2] "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

Power MOSFET Switching Waveforms: A New Insight

Author: Harold R. Ronan, Jr. and C. Frank Wheatley, Jr.

The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V00 varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

Device Models

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed. Figure 1 is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

Figure 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Figure 3. This is the model to be employed for analysis and study

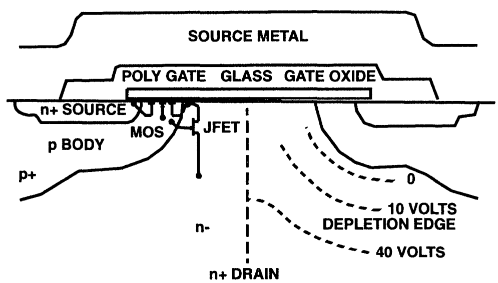


FIGURE 1. CROSS-SECTIONAL VIEW OF MOSFET SHOWING EQUIVALENT MOS TRANSISTOR AND JFET

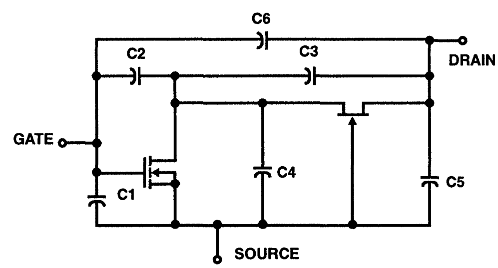


FIGURE 2. MOS TRANSISTOR WITH CASCODE-CONNECTED JFET AND ALL CAPACITORS

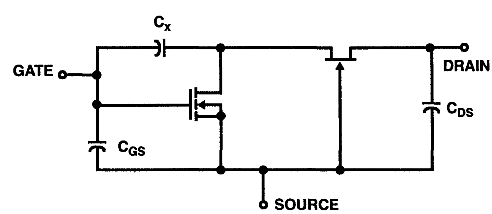


FIGURE 3. FIGURE 2 SIMPLIFIED

Gate Drive: Constant Voltage or Constant Current

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Figure 5.

(2) An instantaneous step current with infinite internal resistance, Figure 6.

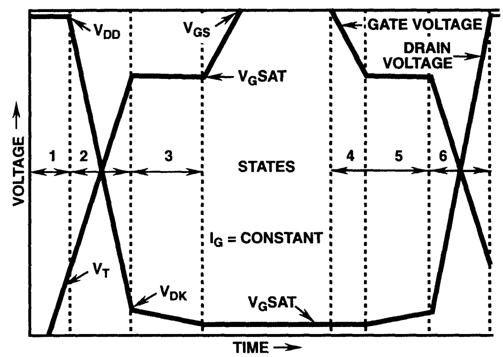


FIGURE 4. IDEALIZED POWER MOSFET WAVEFORMS

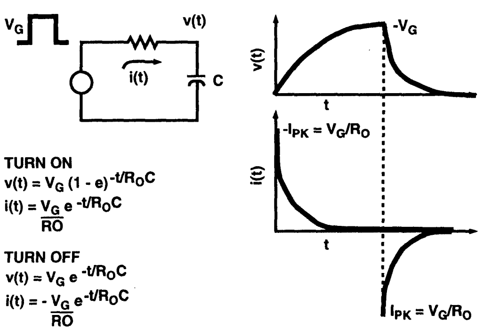


FIGURE 5. STEP-VOLTAGE FORCING FUNCTION

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Figure 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

Six States

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Figure 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated†
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

†The term saturated is taken to mean a constant low-voltage drain-source condition.

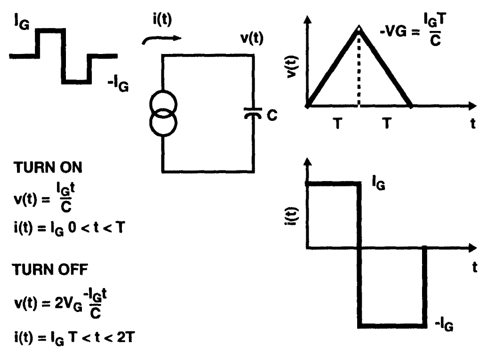
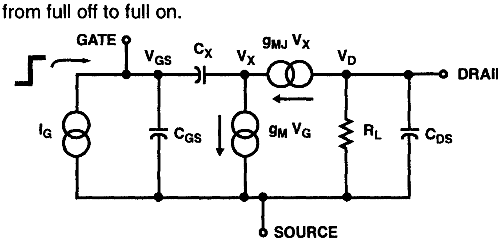


FIGURE 6. STEP CURRENT FORCING FUNCTION

Equivalent Circuit

The lumped-parameter model of Figure 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Figure 7, and the six device states investigated from full off to full on.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFET Transconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE 7. POWER MOSFET EQUIVALENT CIRCUIT

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate source capacitance. More accurately, I_G is charging C_{ISS} ($C_{ISS} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_M v_G$ and $g_{MJ} V_X$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_6. The time to reach threshold, then, is simply:

$$T = \frac{C_{ISS} V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage wave- form. Instead of having to discharge C_X from V_{DD} to ground, the lateral MOSFET need only swing v_X to ground, a much smaller voltage thanks to the grounded gate JFET. Since the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Figure 7 predicts a drain voltage change of:

$$d_{VG}/dt = g_M R_L I_G / [C_{GS} + C_X(1 + g_M/g_{MJ})]$$

In all but the smallest power-MOSFET devices, C_X is several thousand picofarads and g_M/g_{MJ} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected J FET, not because C_{RSS} ($C_{RSS} = C_{GD}$) is a small value, as zero-drain-current data- sheet capacitance values might lead one to believe. If C_{RSS} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_X(1 + g_M/g_{MJ})]/g_M R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{MJ} V_X$ current generator becomes a short circuit and the equivalent circuit predicts:

$$d_{VD}/dt = g_M R_L I_G / [C_{GS} + C_X(1 + g_M R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_M R_L$ is approximately equal to $g_M R_L$ and $C_X(1 + g_M R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_{D[SAT]}) C_X / I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{MJ} V_X$ being shorted, the $g_M V_G$ current generator is shorted, and I_G is occupied with charging C_X and C_{GS}, in parallel, from the peak value of V_G to $V_{G(SAT)}$. The time required for this is:

$$t = (V_G - V_{G(SAT)}(C_{GS} + C_X)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_X.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Figure 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Figure 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A New Device Characterization

Figure 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_X, nor does it convey how V_{DK}, g_M, g_M/g_{MJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $V_D(t)$, $V_G(t)$ for selected values of V_{DD} and I_D within device ratings.

A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $V_D(t)$, $V_G(t)$ at 100%, 75%, 50%, and 25% $V_D(max)$ would be shown.

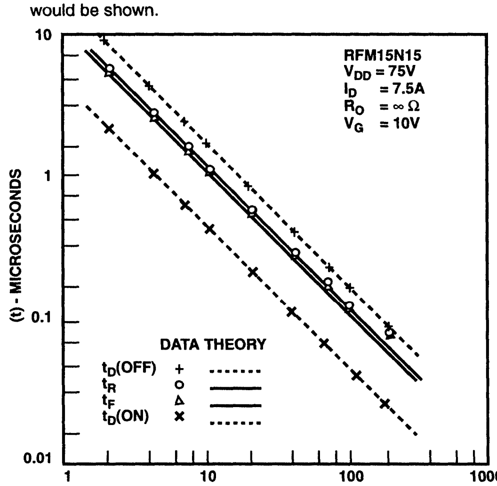


FIGURE 8. CONSTANT GATE CURRENT SWITCHING TIME

Figure 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

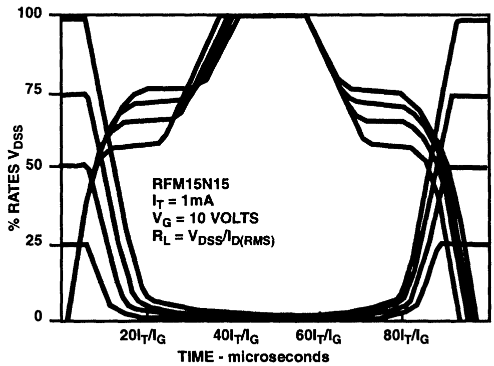


FIGURE 9. NORMALIZED RFM15N15 SWITCHING WAVEFORMS FOR CANSTANT GATE-CURRENT DRIVE.

Step-Voltage Gate Drive

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_O. Often R_O for turn-on is not the same as R_O for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R_O for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate 1G to be used in each state for relating step voltage drives to the characterization curves.

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figures 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current VU/R_O equalling the constant 1G, t6(on), t, td(off), and t1 will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t, t1 switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

TABLE 1. COMMON SWITCHING EQUATIONS

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{ISS} V_T}{I_G}$		$t = R_O C_{ISS} \ln \frac{[1]}{[1 - V_T/G_V]}$
	$I_G = I_T$	**STATE 2: ACTIVE, ACTIVE**	$I_G = (V_G - V_T)/R_O$
		$t = \frac{[V_{DD} - V_DK] [C_{GS} + C_x (1 + g_M/g_{MJ})]}{g_M R_L I_G}$	
	$I_G = I_T$	**STATE 3: ACTIVE, SATURATED**	$I_G = (V_G - V_{GSAT})/R_O$
		$t = \frac{(V_{DK} - V_{DSAT})C_X}{I_G}$	
TURN OFF	$I_G = I_T$	**STATE 4: SATURATED, SATURATED**	$I_G = -V_G/R_O$
	$t = \frac{(C_{GS} + C_X)(V_G - V_{GSAT})}{I_G}$		$t = R_O(C_{GS} + C_X) \ln (V_G/V_{GSAT})$
	$I_G = I_T$	**STATE 5: ACTIVE, SATURATED**	$I_G = (V_G - V_{GSAT})/R_O$
		$t = \frac{(V_{DK} - V_{DSAT})C_X}{I_G}$	
	$I_G = I_T$	**STATE 6: ACTIVE, ACTIVE**	$I_G = (V_G - V_{GSAT})/R_O$
		$t = \frac{[V_{DD} - V_DK] [C_{GS} + C_X (1 + g_M/g_{MJ})]}{g_M R_L I_G}$	

10 APPLICATION NOTES

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figures 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_D(on)$, t_R, $t_D(off)$, and t_F will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_R, t_F switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_{G(SAT)}}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

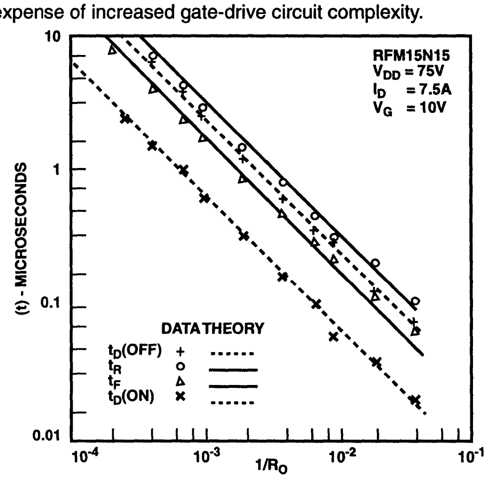


FIGURE 10. CONSTANT GATE VOLTAGE SWITCHING TIME

Using the Characterization Curves, Figure 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_O = 100 ohms, and R_L = 10 ohms, precedes as follows:

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves

$t = 100(1200 \times 10^{-12})$ in $[1/(1 - 4/10)]$

$t =$ 61 ns

State 2: MOS Active, JFET Active

$I_G = (10 - 4)/100 = 60\text{mA}$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{60} = \frac{9}{60} = 150\text{ns}$$

State 3: MOS Active, JFET Saturated

$I_G = (10 - 7)/100 = 30\text{mA}$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{30} = \frac{14}{30} = 467\text{ns}$$

State 4: MOS Saturated, JFET Saturated

$C_{GS} + C_X$ = (gate voltage slope)(test current)

= $(1.5 \times 10^{-6}\text{s}/5\text{ volts})(10\text{mA})$

= 3000pF

$t = 100(3000 \times 10^{-12})$ in [10/6.6]

$t =$ 125ns

State 5: MOS Active, JFET Saturated

$I_G = 6.6/100 = 66\text{mA}$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{66} = \frac{8}{66} = 121\text{ns}$$

Figure 11 shows RFM15N15 waveforms using the conditions specified in the example.

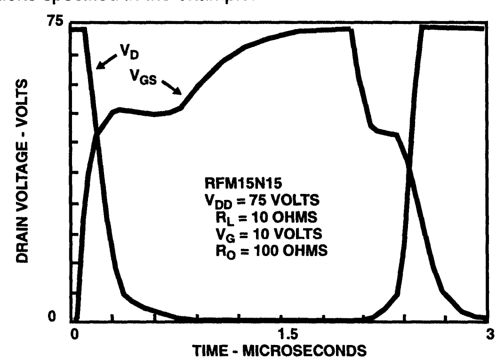


FIGURE 11. STEP GATE VOLTAGE INPUT TO AN RFM15N15

STATE	CALCULATED TIME	MEASURED TIME	RATIO
	(t_C, ns)	(t_M, ns)	(t_C/t_M)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(RMS)}$, the equations of Table 1 may be used in conjunction with slope estimates from the characterization curves for C_X and $C_{GS} + C_X(1 + g_M/g_{MJ})$ at the appropriate drain-current level.

Characterization-Curve Limits

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Figure 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Figure 9.

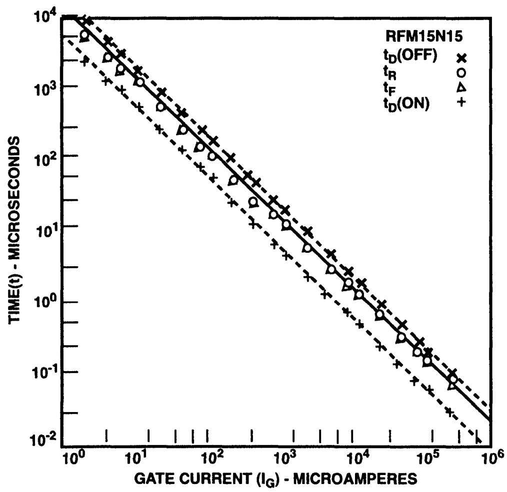


FIGURE 12. FIVE DECADES OF LINEAR RESPONSE

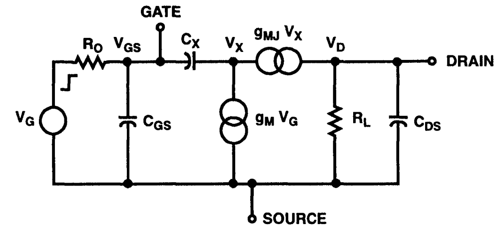
Conclusions

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual-slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

Appendix A - Analysis for Resistive Step Voltage Inputs

Step Voltage Gate Drive

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced wlth a step voltage with internal resistance R_O, Figure A-1.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFET Transconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE A-1. POWER MOSFET EQUIVALENT CIRCUIT

State 1: Mos Off, JFET Off

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{ISS} through R_O.

$$t = R_O C_{ISS} \ln(1/(1 - V_T/V_G)]$$

$$t = V_G/R_O$$

State 2: Mos Active, JFET Active

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Figure A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Figure A-2, applicable gate currents for each of the device states may be listed.

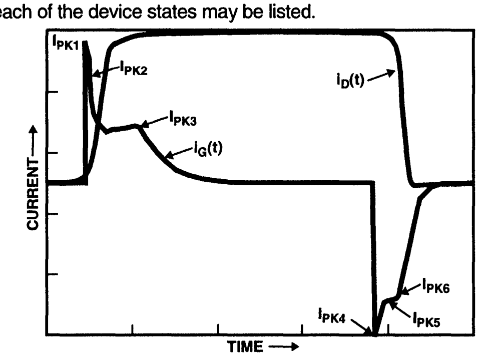


FIGURE A-2. $i_G(t)$ AND $i_D(t)$ FOR A TYPICAL POWER MOSFET DRIVEN BY A STEP GATE VOLTAGE

Turn-On

State 1: MOS Off, JFET Off

$I_{PK1} = V_G/R_O$

State 2: MOS Active, JFET Active

$I_{PK2} = (V_G - V_T)/R_O$

State 3: MOS Active, JFET Saturated

$I_{PK3} = (V_G - V_{G(SAT)})/R_O$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$I_{PK4} = V_G/R_O$

State 5: MOS Active, JFET Saturated

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: MOS Active, JFET Active

$I_{PK6} = V_{G(SAT)}/R_O$

The equivalent circuit of Figure A-1 predicts that:

$$dv_D/dt = -g_M R_L (V_G - V_T) e^{-t/T1} / T1$$

where $T1 = R_O C_{GS} + (1 + g_M/g_{MJ}) R_O C_X$

Note that $g_M R_L (V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Figure A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L \, I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_O$

State 3: Mos Active, JFET Saturated

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dV_D}{dt} = \frac{g_M R_L I_G}{C_{GS} + (1 + g_M R_L) C_X} = \frac{I_G}{C_X}$$

$$I_G = I_{PK3} = (V_G - V_{G(SAT)})/R_O$$

$$\text{and} \quad t = \frac{(V_{DK} - V_{D[SAT]}) C_x}{I_{PK3}}$$

State 4: Mos Saturated, JFET Saturated (Turn-off)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_X in parallel with C_{GS} through R_O.

$$t = R_O (C_{GS} + C_X) \ln[V_G/V_{G(SAT)}]$$

$$I_{PK4} = V_G/R_O$$

State 5: Mos Active, JFET Saturated

The JFET current generator $V_X g_{mJ}$, is operative.

$$t = \frac{[V_{DK} - V_{D[SAT]}] C_X}{I_{PK5}}$$

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: Mos Active, JFET Active

The Miller effect is now reduced by the activation of $V_G g_{MJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L \, I_{PAK6}}$$

$I_{PAK6} = V_{G(SAT)}/R_O$

Appendix B - Estimating R_O for Some Typical Gate-Drive Circuits

Case 1: Typical Pulse-Generator Drive, Figure B-1

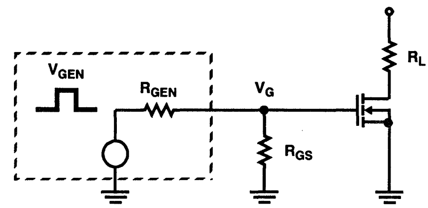


FIGURE B-1. TYPICAL PULSE-GENERATOR DRIVE CIRCUIT

Turn-On and Turn-Off

$$R_O = R_{GEN} R_{GS} / (R_{GEN} + R_{GS})$$

For the typical case where $R_{GEN} = 50\Omega$, and a coaxial-cable termination of 50 ohms, $R_O = 25\Omega$ and $V_G = V_{GEN}/2$.

Case 2: Voltage-Follower Gate Drive, Figure B-2

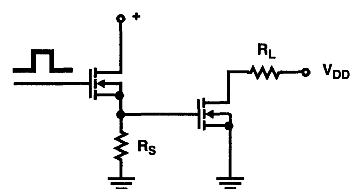


FIGURE B-2. VOLTAGE-FOLLOWER GATE-DRIVE CIRCUIT

Turn-On

R_O is approximately equal to $1/g_M$ for R_S very much greater than $1/g_M$.

gm = transconductance of driving MOSFET transistor.

Turn Off

$R_O = R_S$

Case 3: Common-Source Gate Drive, Figure B-3

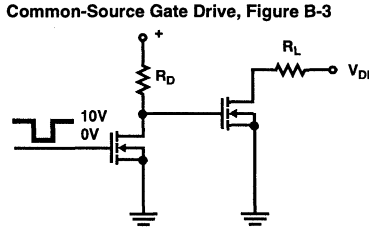


FIGURE B-3. COMMON-SOURCE GATE-DRIVE CIRCUIT

Turn-On

$R_O = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn Off

$R_O = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

Harris Semiconductor

APP NOTE

No. AN7332.1 May 1992

Harris Power MOSFETs

The Application Of Conductivity-Modulated Field-Effect Transistors

Author: Jack Wojslawowicz

Summary

The development of conductivity-modulated field-effect transistors, FETs, makes available to the system designer another solid-state device that can be used to implement power switching control. This paper reviews differences between the standard and the newly developed FET. It shows the significant advantages that the conductivity-modulated FET has over the standard FET. Several applications are presented to show that this new type of device works well in practical situations. The relative immaturity of the conductivity-modulated FET may limit its initial utilization. But as the family grows and product innovation and refinement takes place, this newest member of the power semiconductor family will become a viable alternative to the other members.

General Considerations

The development of the power field-effect transistor has made available to the power-stage designer an entire new family of power semiconductors. Over the past 5 to 6 years, the breadth of product has grown to encompass the requirements of a large number of applications. A limiting factor that has slowed the utilization of power FETs in the high-current, high-voltage applications is the fact that the on-state resistance ($R_{DS(ON)}$) in a standard FET is related to its breakdown voltage (B_{VDSS}) by a nearly cubic power, i.e., $R_{DS(ON)} \approx B_{VDSS}$ 2.8. What this implies, as Figure 1 shows, is that as the breakdown voltage increases, the on-state resistance climbs even faster.

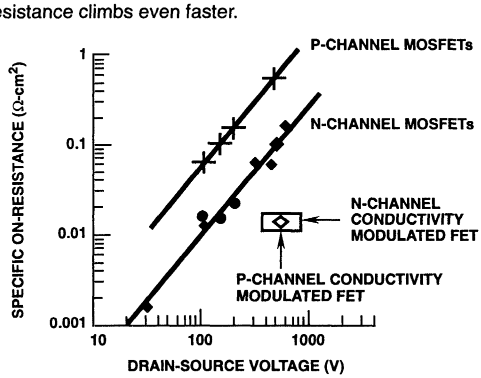


FIGURE 1. SPECIFIC ON-RESISTANCE OF P AND N-CNANNEL MOSFETS AND CONDUCTIVITY-MODULATED FETS vs FORWARD BLOCKING VOLTAGE.

The MOSFET on-state resistance is contributed to primarily by three components of the transistor: the MOS channel, the neck region, and the extended drain region. The extended drain region contributes the most to the on-state resistance in high-voltage MOSFETs. To achieve a lower on-state resistance at a given blocking voltage, the usual technique is simply to make the die larger. However, increasing the die size has its limitations from a manufacturing point of view, since MOSFETs, with their very fine horizontal geometries, are highly defect-yield sensitive. As die size increases, the likelihood of a defect resulting in a nonfunctional part increases exponentially. This tendency, combined with a smaller number of parts per wafer, limits the availability of low-on-state-resistance, high-voltage MOSFETs.

A change in the horizontal geometry of the MOSFET can lower the specific on-state resistance per unit area. By using more channel width with smaller source cells placed closer together, a reduction in on-state resistance can be achieved. A limitation on how close these cells can be placed arises from a possible localization of field concentrations that will limit the voltage breakdown of the structure to less than the theoretical rating due only to impurity concentrations. Therefore, for a given breakdown voltage, there exists a minimum spacing of the cell structure. Generally, the higher the required breakdown voltage, the further apart the cells must be placed.

As stated earlier, the extended drain region of the MOSFET generally contributes the most to the on-state resistance in high-voltage MOSFETs. As the required blocking voltage is increased, this region must be made thicker and more lightly doped to be able to support the desired voltage. It is this region's contribution to on-state resistance that the conductivity-modulated field-effect transistor drastically reduces. This reduction occurs as the result of the injection of minority carriers from the substrate and, in specific on-state resistance per unit area, is about 10 times less than in a standard MOSFET at the 400V BV_{DSS} level, as shown in Figure 1.

Further analysis has shown that the specific on-state resistance may be nearly independent of blocking-voltage level. This finding implies that at a BV_{DSS} of 1000V, the reduction in conductivity-modulated FETs over the standard MOSFETs could be perhaps 50 to 1. These reductions in on-state resistance per unit area that the conductivity-modulated FETs can achieve present the possibility that high-voltage high-current FET-type devices can become more readily available because of the smaller die sizes associated with conductivity-modulated FETs.

Comparison of Standard and Conductivity-Modulated FETs

Standard and conductivity-modulated FETs share some characteristics, but are substantially different in others. Shown in Table 1 is a listing of the major characteristics that make the conductivity-modulated FETs unique among power semiconductor families. Foremost, it is a voltage-gated device; its input characteristics are similar to standard power MOSFETs of comparable chip size. Very little drive power is required at low to moderate switching frequencies. The device remains under the control of the gate within its normal operating conditions. It exhibits the normal linear mode as well as the fully saturated on-state of conventional power MOSFETs. When the gate voltage is removed, the device turns off, unlike the thyristor family of power semiconductors, which must be either externally or naturally (internally) commutated.

TABLE 1. CONDUCTIVITY-MODULATED FET CHARACTERISTICS

Voltage Gated	Small gate power required. Similar to standard power MOSFET.
Turn Off	When gate drive is removed... Unlike an SCR!
Nonlinear On-State Voltage drop	Like that of an SCR.
Turn On Speed	Fast! Comparable to a standard power MOSFET.
Turn-Off Speed	Slow! Comparable to a bipolar transistor.
Temperature Independent On-State Voltage Drop	Unlike the typical 2x variation of a power MOSFET.

The on-state voltage drop or resistance characteristic of a conductivity-modulated FET is markedly different from that of a standard power MOSFET, and is similar to that of a thyristor family member, the SCR. There is an offset voltage component (typically 0.6V) due to the p-n junction on the drain side, and a somewhat nonlinear resistive component, both of which are in series between the drain and source terminals. This series arrangement results in a highly nonlinear equivalent resistance, unlike the linear resistive characteristic of $V_{DS(ON)}$ of a standard FET.

The structure of the conductivity-modulated FET operates during its turn on just as a standard FET does, hence its turn-on speed is very similar to that of a standard FET. With its high input impedance and its short propagation delay, the turn-on transition of the conductivity-modulated FET, as well as the standard power FET, is easily controlled by the gate driving circuit. This characteristic allows the designer the ability to control EMI and RPI generation easily. With other power semiconductors, it may be necessary to employ elaborate circuit schemes to limit rapidly rising in-rush currents.

A significant characteristic that must be considered in power switching applications is that of turn-off speed. The internal action that makes the conductivity-modulated FET such a silicon-efficient device also makes it an inherently slower device during turn-off. The injection of the minority carriers during the on-state conduction of current results in these carriers being present at the moment of turn-off. Without any way of removing these carriers by external means, they must recombine within the structure itself before the device can revert to its fully off-state condition. The quantity of these carriers and how fast they can deplete themselves determines the turn-off switching speed of the conductivity-modulated FET. This process of recombination is considerably slower than the simple discontinuance of majority carrier flow by which the standard power FET turns off. Hence, again, the conductivity-modulated FET is an inherently slower device. Its turn-off speed lies somewhere between the performance of a thyristor and that of a bipolar transistor.

The final characteristic that makes the conductivity-modulated FET different from a conventional FET is the variance of on-state voltage with temperature. The characteristic of the conductivity-modulated FET is similar to that of an SCR, varying about -0.6mV/^{o}C. The conventional FET has a positive temperature coefficient such that on high-voltage devices the $R_{DS(ON)}$ will double from its +25^{o}C value when the junction temperature reaches +150^{o}C. The system designer must take this characteristic into consideration when the heat sink is being designed for the system.

It is these similarities and differences that make the conductivity-modulated FET a unique member of the family of power-semiconductor switching devices. Applications of this alternative power switching device invariably make use of one or more of its unique characteristics.

Applications

Automotive Ignition

An application that can take advantage of the low drive-power capability of the conductivity-modulated FET is the electronic automotive ignition system. In Figure 2, the control IC takes the signal from the pickup coil located in the distributor and regulates the current through the ignition coil. At the proper time, the IC removes base drive from the bipolar transistor, which all systems currently employ as their coil driver. This removal of base drive allows the transistor to shut off which, in turn, causes a rapid decrease in the ignition-coil primary current. As the primary current decreases to zero, the energy stored in the field surrounding the primary is transferred to the secondary coil. The secondary coil, consisting of many more turns than the primary, transforms this energy into a higher voltage, resulting in a spark being generated in the cylinder. The control IC determines when this spark occurs, so as to derive usable power. With the use of a bipolar transistor, it is estimated that approximately two-thirds of the power dissipation that occurs in the control IC is the result of the need to be able to drive the required base current of the ignition output transistor. The high-impedance input of the conductivity-modulated FET virtually eliminates the base-current drive dissipation of the control IC.

With improved silicon usage, the conductivity-modulated FET brings to power semiconductor switching devices the die size necessary to attain the required voltage and current-handling capabilities of the electronic ignition. This smaller-sized die makes possible smaller modules, whether they be hybrid or standard PC-based systems, than those currently implemented with bipolar-transistor technology.

Brushless DC Motors

Another emerging application that can make use of conductivity-modulated FETs is the emerging field of brushless DC motors. In this class of application, the solid-state devices are used to electronically switch the voltage to the multiplicity of windings that are employed. The motor consists of an armature that has a number of N and S poles consisting of high-strength permanent magnets. The stator is made up of the multiplicity of windings that were mentioned above; the windings are spaced incrementally about the outside frame of the housing. The voltages to these windings are all electronically switched to create a rotating magnetic field. The armature then rotates to maintain its relative position within the moving magnetic field. The switching of the voltage on the stator windings is done by means of power semiconductor devices. A basic block diagram of such a system is shown in Figure 3.

The control logic provides the proper sequence of drive signals based on the rotation direction desired, the speed desired, and the enable input. These requirements are combined with the inputs from the hall-effect sensors to determine which power devices should be activated. Since the current through the stator windings must be bidirectional, the half-bridge or totem-pole output configuration is used to steer the current. This circuit implementation is generally performed with complementary devices, although single-polarity devices can be used with increased circuit complexity.

In a typical 120V off-line system, like the one shown in Figure 3, the switching devices must have a 300V to 400V blocking capability. For larger size motors, where larger currents are necessary, the use of power FETs generally implies the use of large die to achieve a low power dissipation to meet the heat-dissipation capability of the packaging. The conductivity-modulated FET, with its temperature-independent on-state-voltage-drop characteristic, helps this situation by keeping the dissipation lower than can be achieved with a standard power FET because of the increasing $R_{DS(ON)}$ characteristic of that device. The small die size of the conductivity-modulated FET, the result of better silicon utilization, again makes them the practical choice in motor control not only because of their electrical characteristics, but also because of the lower manufacturing cost of the die.

As stated above, system complexity can be reduced with complementary devices. Although p-channel conductivity-modulated FETs are not yet commerically available, laboratory samples have been fabricated which offers better silicon utilization efficiency than their conventional p-channel counterparts. This statement is based on the fact that p-channel MOSFETs require a 2.5 times larger area than an n-channel device for the same $R_{DS(ON)}$. The easier drive requirements for the n-channel (directly driven from the control IC) and the simplified voltage-translation circuit for driving the p-channel devices, combined with the

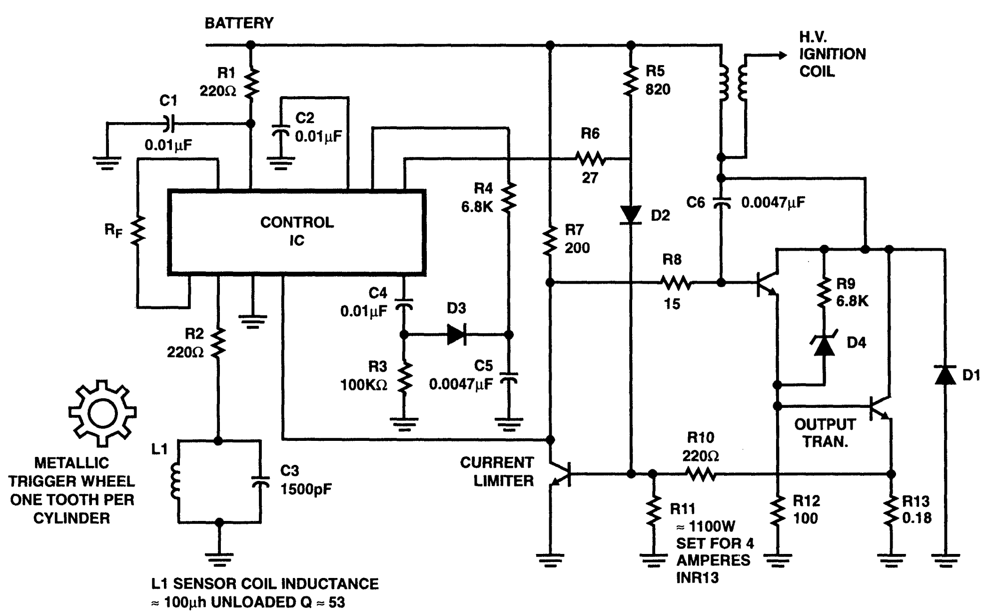


FIGURE 2. TYPICAL IGNITION SYSTEM

smaller die size with potentially lower device cost for comparable power handling capability, makes the conductivity-modulated FET a natural for the brushless DC motor application.

Switching Power Supply

One final application that has the potential for conductivity-modulated FET usage is the switching power supply. A half bridge configuration implementation is presented in Figure 4. The system shown uses a standard PWM control IC to drive the conductivity-modulated FETs through the T2 transformer. The voltage drive characteristic of these devices makes the design of transformer T2 quite simple. The control IC is more lightly loaded because it does not have to supply a continuous base drive, as would be necessary with bipolar transistors.

The operating frequency and the "dead time" are the limitations placed on this system when conductivity-modulated FETs are used. The inherent lower switching speeds of these types of devices make these limitations necessary. The system is currently limited to the 20kHz to 30kHz range, with dead times as low as 1 to 2 microseconds. This characteristic is comparable to many existing bipolar systems.

Improvements in switching speeds will occur as the conductivity-modulated FET matures. It is, however, unlikely that they will ever have the same switching speeds as standard power FETs. This limitation prohibits their use in some of the newer higher-frequency power supplies being designed now with conventional FETs. However, in higher-power supplies, where conventional FETs must be paralleled to achieve a low enough $R_{DS(ON)}$ for good efficiency, the conductivity-modulated FET may present a viable alternative with its smaller die size. Although the operating frequency of the system may have to be compromised to use them.

Conclusion

The conductivity-modulated FET represents a progression in the ever-advancing state-of-the-art development that occurs in the world of solid-state devices. The unique structure of these devices presents characteristics that make them equivalent in many ways to conventional FETs but superior in other ways. The system designer must take into account these similar and dissimilar characteristics to properly use them. The capabilities of the conductivity-modulated FETs allow them to make inroads into applications currently served by bipolar transistors, and in some cases conventional power FETs. As the devices mature through innovation and product refinement, conductivity-modulated FETs will become vital members of the family of solid-state power-semiconductor devices.

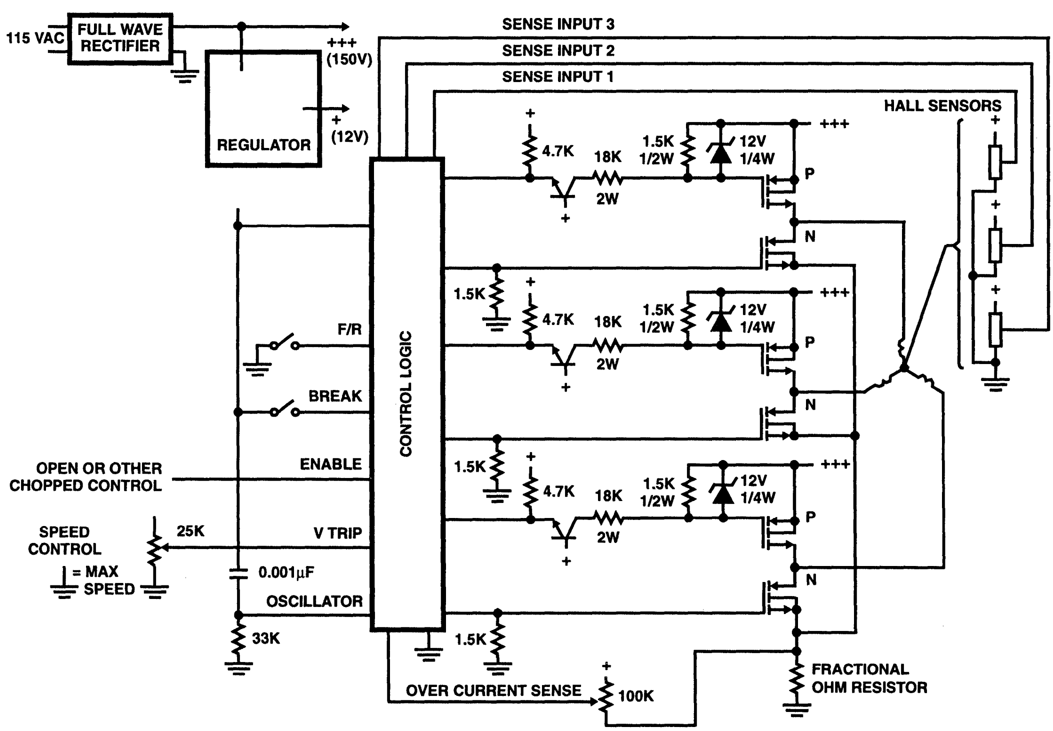


FIGURE 3. CONTROL CIRCUIT FOR THREE-PHASE BRUSHLESS DC MOTOR

Bibliography

1. J.P. Russell, L.A. Goodman, A.M. Goodman, and J.M. Neilson, "The COMFET - A New High Conductance MOS-Gated Device," IEEE Electron Device Letters EDL-4, 1983, pg. 63-65
2. A.M. Goodman, J.P. Russell, L.A. Goodman, C.J. Nuese, and J.M. Nelson, "Improved COMFETs with Fast Switching Speeds and High Current Capability," Proceeding of the IEEE International Electron Devices Mtg., Dec. 1983, pg. 79-83
3. B.J. Baliga and Marvin Smith, "Modulated Conductivity Devices Reduce Switching Losses," EDN, Sept. 29, 1983,. pg. 153-162
4. M. Smith, W. Sahm, and S. Bahu, "Insulated Gate Transistors Simplify AC Motor Speed Control," EDN, Feb. 9,1984, pg. 181-200
5. B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray, and N.D. Zammer, "The Insulated Gated Transistor a New Three Terminal MOS-Controlled Blpolar Power Device," IEEE Transactions on Electron Devices, Vol. ED-31 No. 6, June 1984, pg. 821-828

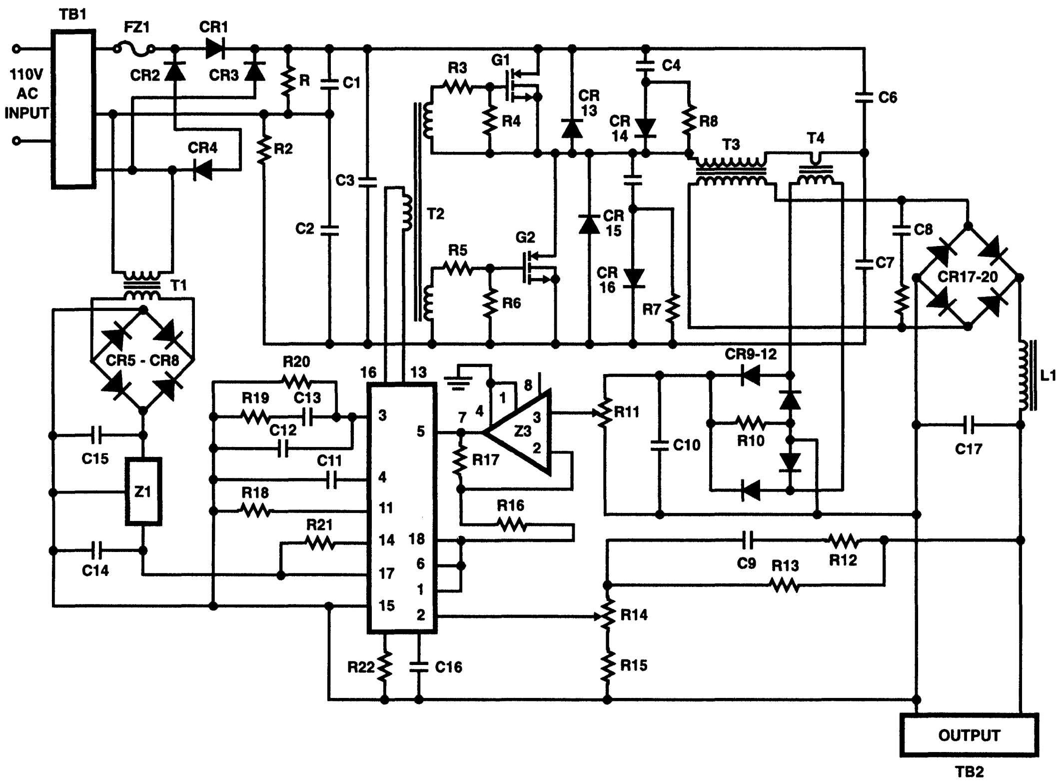


FIGURE 4. HALF-BRIDGE SWITCHING POWER SUPPLY

10

APPLICATION NOTES

Harris Semiconductor

APP NOTE

No. AN8602.1 May 1992

Harris Power MOSFETs

The IGBTs - A New High Conductance MOS-Gated Device

Author: J.P. Russell, A.M. Goodman, L.A. Goodman and J.M. Neilson

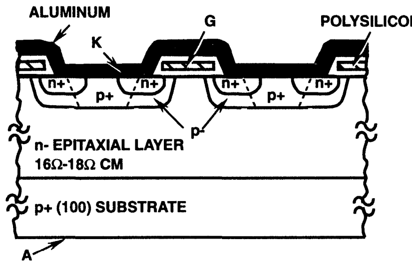
Abstract

A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n^--epitaxial layer grown on a p^+ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

Introduction

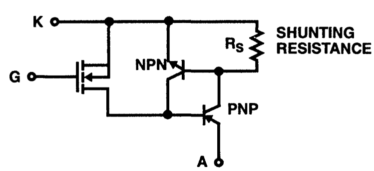
Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym IGBTs (**I**nsulated **G**ate **B**ipolar **T**ransistor).

This device, while similar in structure to the MOS-gated thyristor,[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.[6] The structure and the equivalent circuit for the IGBTs are shown in Figure 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n^--epitaxial Si layer is grown on a p^+ substrate instead of an n+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance shown in Figure 1(b). This has the effect of lowering the current gain of the n-p-n transistor (αn-p-n) so that αn-p-n + αp-n-p <1. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.[6]



REGION	THICKNESS (μm)
EPI	60 - 62
n^+	1.0 - 1.5
p^-	3.5 - 4.0
p^+	5.0 - 5.5

(A) STRUCTURE



(B) EQUIVALENT CIRCUIT

In the remainder of this note we describe the operation and characteristics of this device.

Device Operation

The IGBT is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage V_A below the breakdown level V_{BF} . When V_A < V_{BF} and the gate voltage is larger than the threshold value V_{GT}, electrons pass into the n^--region (base of the p-n-p transistor). These electrons lower the potential of the n^--region, forward biasing the p^+ - n^- (substrate-epi-layer) junction, thereby causing holes to be injected from the p+ substrate into the n^- epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n-region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps αn-p-n very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing αn-p-n to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

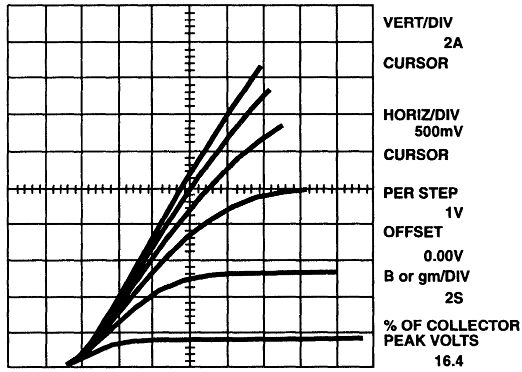
Device Characterization

Two different lots of IGBT structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5mm and 3mm square devices were fabricated using a standard HEXFET geometry[7] with a polysilicon gate electrode over an SiO_2 gate dielectric. Several hundred IGBT were mounted in standard TO-3 and TO-66 packages and characterized under DC and pulsed conditions, as described below.

With zero gate bias, the forward characteristic of a IGBTs shows very low current (<1nA) up to about 390V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p^+ substrate and the n^- epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100V because edge passivation was not used.

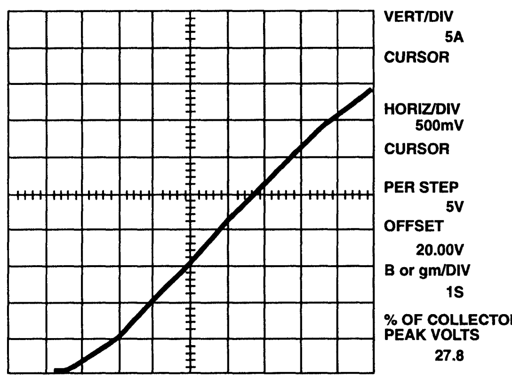
Figure 2(a) shows the MOSFET-like transfer characteristics of an IGBT in the low gate-voltage region. A noteworthy feature of the IGBT characteristic is the ~0.7V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the p^+ - n^- (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Figure 2(b) shows the i(v) characteristic of an IGBT with V_G = 20V, and demonstrates the low on-resistance of the device (~0.084Ω at 20A). The on-resistance values of nearly all of the many IGBT fabricated to date have been less than 0.1Ω (at 20A) for the 3mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Figure 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (Harris, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",[3] supplemented with some of the "best" of Harris' commercial and developmental MOSFETs. Note that the on-resistance of the IGBT is approximately 10 times less than that of a 400V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from IGBT designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present IGBT structures were designed for 600V, but V_{BF} was limited to 400V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the IGBTs on-resistance of less than 0.1Ω even more attractive for high-voltage applications.



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

FIGURE 2A MOSFET - LIKE CHARACTERISTIC



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

FIGURE 2B. IGBT i(v) with V_G = 20V

Transient Response Measurement

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Figure 4.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5μs to 20μs were observed, with the precise value depending on circuit conditions and the turn-off time of the gate pulse.

The n-p-n-p structure of the IGBTs is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10A - 30A in 3mm square chips. The magnitude of the latching current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off (~10μs) permits anode currents up to 30A without latching. However, rapid gate turn-off (≤ 1μs) leads to latching at a much lower anode current level (~10A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing αn-p-n to increase, and leading to the condition for latching, αn-p-n + αp-n-p = 1. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps αn-p-n sufficiently low to avoid latching.

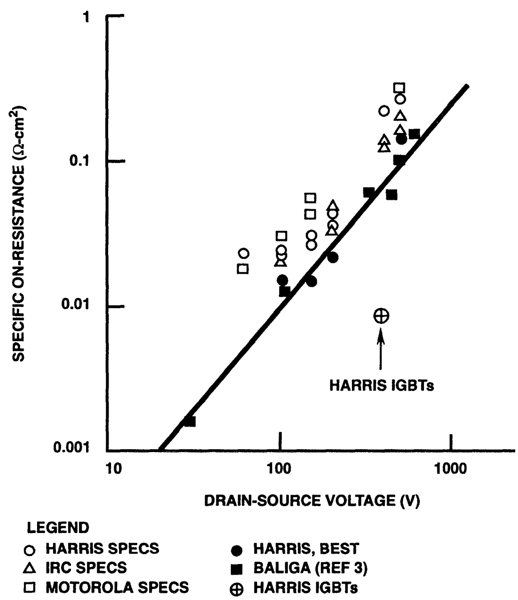


FIGURE 3. SPECIFIC ON-RESISTANCE vs DRAIN-SOURCE VOLTAGE CAPABILITY FOR STATE-OF-THE-ART POWER MOSFETS AND THE IGBTs

Summary

A new MOS-gate-controlled power device, the IGBTs, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on- resistance is due to conductivity modulation of the n epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

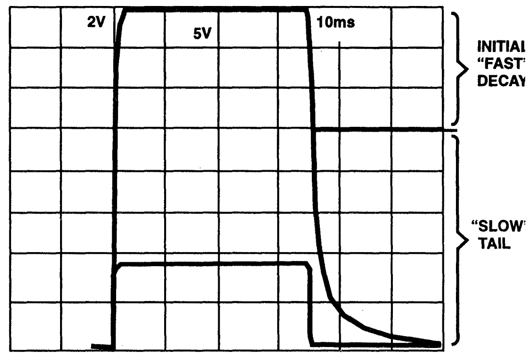


FIGURE 4. GATE VOLTAGE (LOWER TRACE) AND ANODE CURRENT (UPPER TRACE) WAVEFORMS FOR i_A(MAX) = 8A

Acknowledgment

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories. Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

References

[1] M. L. Tarng, "On-Resistance Characterization of VDMOS Power Transistors", in IEDM Tech. Dig., 1981, pp 429-433.

[2] C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage", IEEE Trans. Electron Devices, Vol. ED-26, p 243,1979.

[3] B.J. Baliga,"Switching Lots of Watts at High Speeds", IEEE Spectrum, Vol.18, p 42, Dec. 1981.

[4] J. Tihanyi, "Functional Integration of Power MOS and Bipolar Devices", in IEDM Tech. Dig., 1980, p 75-78.

[5] L. Leipold et al., "A FET Controlled Thyristor in SIPMOS technology", in IEDM Tech. Dig., 1980, pp 79-82.

[6] H.W. Becke and C.F. Wheatley, "Power MOSFET With An Anode Region", U.S. Patent 4,364,073, issued Dec.14, 1982.

[7] H.W. Collins and B. Pelly, "HEXFET, A New Power Technology Cuts On-Resistance, Boosts Ratings", Electron. Des., Vol. 12, p 36, 1979.

[8] S.M. Sze, Physics of Semiconductor Devices. 2nd Edition, New York; Wiley, 1981, p 120.

Improved IGBTs with Fast Switching Speed And High-Current Capability

Authors: A.M. Goodman, J.R. Russell, L.A. Goodman, C.J. Nuese and J.M. Neilson

Abstract

Conventional vertical power MOSFETs are limited at high voltages (>500V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called an IGBT, this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turnoff, having a fall time in the range 8 to 40μs. The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the IGBTs, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1μs and latching currents as high as 50A, while retaining on-resistance values <0.2Ω for a 0.09cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of IGBTs (with forward-blocking voltage capabilities of 400-600V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20% increase in on-resistance.

Introduction

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate. We have called this device a COMFET-an acronym for **CO**nductivity **Modu**lated **F**ield **E**ffect **T**ransistor;[4] the device has also been called an IGBT or **I**nsulated **G**ate **B**ipolar **T**ransistor.

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

When a IGBT is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, τ_F. Large values of τ resulted in anode-current fall time, t_F, in the range 8-40ms. [4,5]

The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of I_L, ≤ 10A were observed in 0.09cm^2 area devices when the gate voltage was turned off rapidly (<1ms); for slower gate voltage turnoff (~10ms), I_L values as high as ~30A were observed.

The purpose of the present work has been to reduce t_F and to increase I_L while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved t_F values as low as 100ns and I_L values as high as 50A with rapid gate voltage turnoff.

Modified Structure

A schematic diagram of the original IGBT structure[4] is shown in Figure 1(a), and the equivalent circuit is shown in Figure 1(b); they are similar to those of an MOS-gated thyristor except for the presence of the shunting resistance Rs in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n-epitaxial layer is grown on a p+ substrate instead of an n+ substrate. The heavily doped p+ region in the center of each unit cell, combined with the aluminum contact shorting the n+ and p+ regions, provides the shunting resistance RS. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that $\alpha npn + \alpha pnp < 1$, thereby preventing latching over a large operating range of anode voltage V_A and anode current i_A. However, for sufficiently large i_A, emitter injection in the n-p-n transistor will increase, accompanied by an increase in αnpn. When $\alpha npn + \alpha pnp$ increases to 1, the four-layer device will latch; the level of i_A at which this occurs is the latching current level, I_L. Thus, it can be seen that a structure modification that lowers αpnp will allow a greater range of i_A (and αnpn) without latching; that is, a reduction in αpnp corresponds to an increase in I_L.

The modified structure shown in Figure 1(C) differs from that in Figure 1(A) by the addition of a thin (~10mm) layer of n+ silicon in the epitaxial structure between the n- region and the p+ substrate. This n+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3. In addition, there is also a reduction in t_F.

These results are illustrated in Figure 2, in which t_F, is plotted versus i_A for each device structure. It should be noted that IGBTs with the modified structure can block high voltage only in the forward voltage direction since the emitter junction (p+ - n+) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.

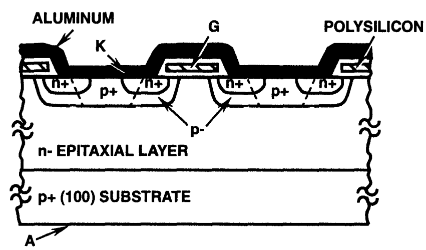


FIGURE 1A. SCHEMATIC DIAGRAM OF ORIGINAL IGBTs STRUCTURE

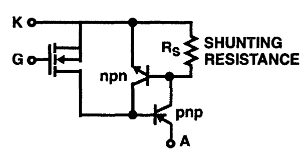


FIGURE 1B. EQUIVALENT CIRCUIT

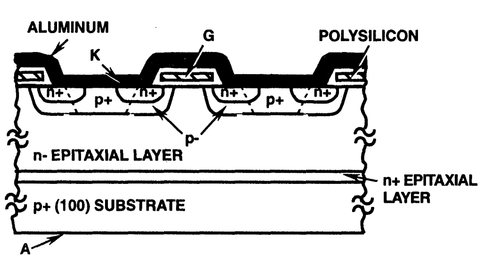


FIGURE 1C. SCHEMATIC DIAGRAM OF MODIFIED STRUCTURE

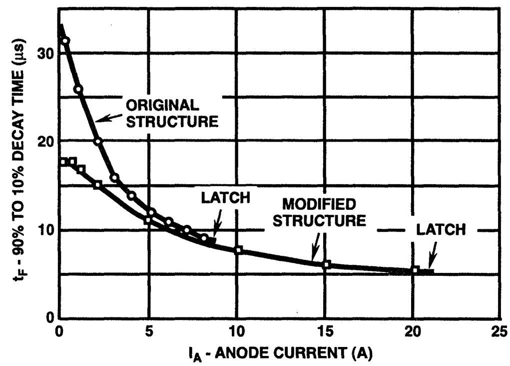


FIGURE 2. ANODE-CURRENT FALL TIME t_F VERSES ANODE CURRENT FOR ORIGINAL STRUCTURE AND MODIFIED STRUCTURE

Addition Of Recombination Centers

We have used a variety of techniques to add recombination centers to IGBTs; these include high energy electron, gamma ray, and fast neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate oxide charge, as well as those radiation induced defects in the silicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_F of the order of 1µs or less were achievable using any of the techniques.

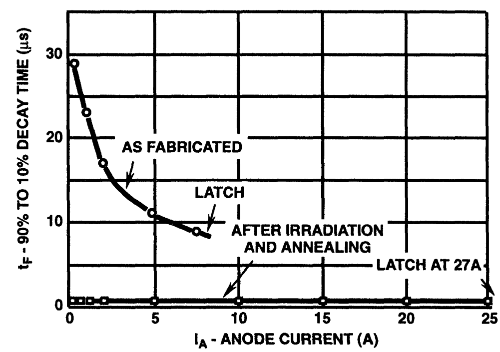
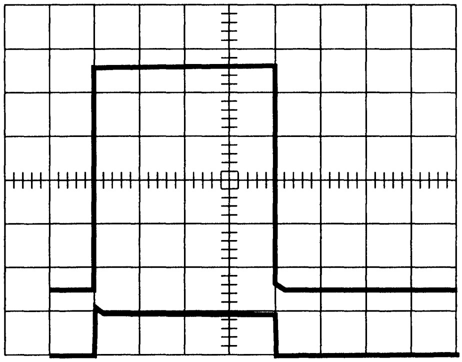
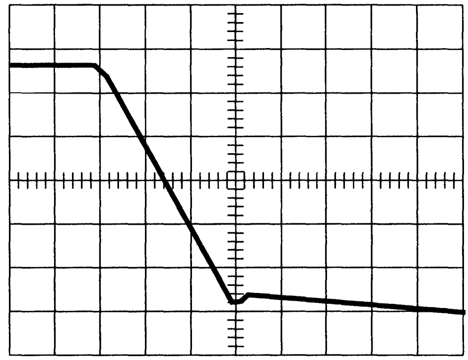


FIGURE 3. ANODE-CURRENT FALL TIME t_F VERSUS ANODE CURRENT FOR AN AS-FABRICATED DEVICE AND AFTER 14MeV NEUTRON IRRADIATION (10^{13}n/cm^2) FOLLOWED BY ANNEALING AT +300°C.

An example of the variation of tF, with iA (1) as fabricated and (2) after irradiation with 14MeV neutrons and annealing is shown in Figure 3. Here, the neutron fluence was ~10^{13}n/cm^2; this was followed by annealing at +300°C. Note that t_F, has not only been drastically reduced, but is virtually constant at ~0.6µs; i.e., almost independent of i_A.



TOP: ANODE CURRENT, 5A/DIV
BOTTOM: GATE VOLTAGE, 20V/DIV
5μs/DIV



ANODE CURRENT ON
EXPANDED TIME SCALE
5A/DIV
100ns/DIV
t_{FALL} ~ 160ns

FIGURE 4. IGBTs ANODE CURRENT AND GATE VOLTAGE WAVEFORMS

It is possible to lower t_F, still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_F, that we have obtained for fully stabilized IGBTs is in the range 100ns to 200ns. This is illustrated in Figure 4.

The reduction in minority carrier lifetime that allows faster switching also carries with it a penalty higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of an IGBT, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Figure 5 we plot the on-resistance (at i_A = 20A) of a series of devices with 0.09cm^2 chip area against their t_F, values after irradiation and annealing. All t_F, values shown were obtained at i_A = 5A; for the devices with short switching times, t_F, is virtually independent of i_A. Clearly, there is a trade-off involved, and the optimum choice of a value for t_F, and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2Ω is approximately an order-of-magnitude less than that of comparably sized n-channel MOSFETs.

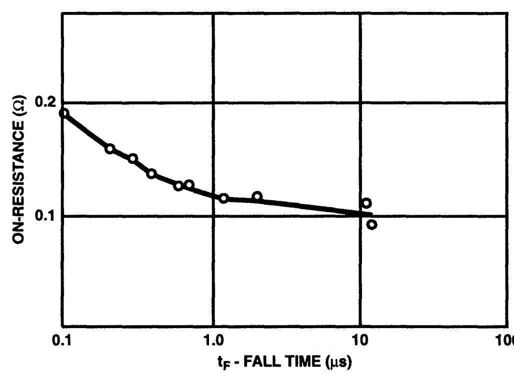


FIGURE 5. ON-RESISTANCE vs. ANODE-CURRENT FALL TIME t_F FOR A SERIES OF IGBTs AFTER VARIOUS IRRADIATION AND ANNEALING TREATMENTS

Temperature Dependence of T_F, and I_L

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Figure 6 the variation of t_F and I_L for a device that has been irradiated and annealed is plotted versus temperature in the range +25°C to +150°C. This behavior is typical of all of the devices we have tested; i.e., t_F increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval +25°C to +150°C.

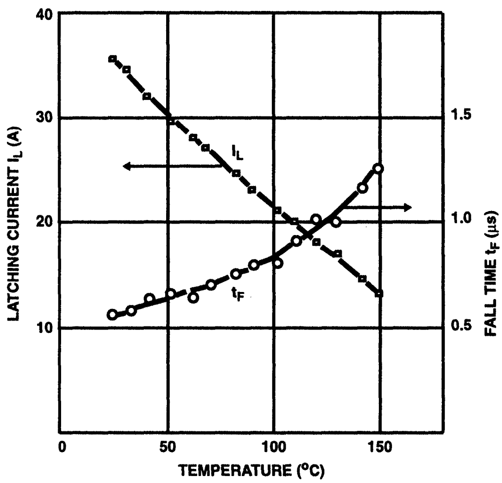


FIGURE 6. VARIATION OF ANODE-CURRENT FALL TIME t_F AND LATCHING CURRENT I_L WITH TEMPERATURE

Summary

By modification of the epitaxial structure of the IGBT and the addition of recombination centers, we have achieved anode-current fall times as low as 100ns in IGBTs with latching currents as high as 50A for a 0.09cm^2 chip area. We have described the trade-off between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

Acknowledgment

The authors are indebted to D. Bergman, R. Ford, F. DiGeronimo, G. Looney, P. Robinson, W. Romito, L. Skurkey, M. Snowden, R. Stolzenberger, and the staff of the Integrated Circuit Technology Center at RCA Laboratories for their various contributions to the fabrication and characterization of the IGBTs. A special thank you goes to F. Taft, Z. Streletz, and H. Hendel who carried out the device irradiations.

References

[1] M. L.Tarng, "On-Resistance Characterization of VDMOS Power Transistors", IEDM Tech. Dig., 1981, pp 429-433.

[2] C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage", IEEE Trans. Electron Devices ED-26, p 243, (1979).

[3] B. Jayant Baliga, "Switching Lots of Watts at High Speeds", IEEE Spectrum 18, p 42 (Dec. 1981).

[4] J.P. Russell, A. M. Goodman, L. A. Goodman and J. M. Neilson, "The IGBTs - A New High Conductance MOS-Gated Device", IEEE Electron Device Letters EDL-4, pp 63-65(1983).

[5] B. J. Baliga, M. S. Adler, P. V. Gray, R. P. Love and N. Zommer, "The Insulated Gate Rectifier (IGR): A New Power Switching Device", IEDM Tech. Dig., 1982, pp 264-267.

[6] H. W. Becke and C. F. Wheatley, "Power MOSFET With An Anode Region", U. S. Patent 4,364,073, issued Dec. 1982.

[7] S. K. Ghandi, Semiconductor Power Devices (John Wiley, New York, 1977) p 296.

Harris Semiconductor

APP NOTE

No. AN9318 September 1993

Harris Power

Insulated-Gate Transistors Simplify AC-Motor Speed Control

Authors: Marvin Smith, William Sahm and Sridhar Babu

An IGT's few input requirements and low On-state resistance simplify drive circuitry and increase power efficiency in motor-control applications. The voltage-controlled, MOSFET-like input and transfer characteristics of the insulated-gate transistor (IGT) (see EDN, September 29, 1983, pg 153 for IGT details) simplify power-control circuitry when compared with bipolar devices. Moreover, the IGT has an input capacitance mirroring that of a MOSFET that has only one-third the power-handling capability. These attributes allow you to design simple, low-power gate-drive circuits using isolated or level-shifting techniques. What's more, the drive circuit can control the IGT's switching times to suppress EMI, reduce oscillation and noise, and eliminate the need for snubber networks.

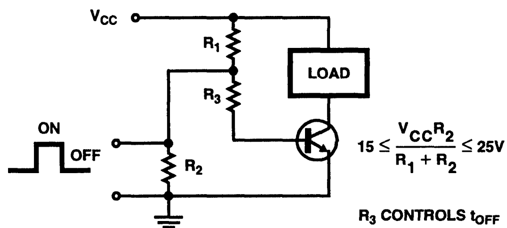


FIGURE 1A. SIMPLE DRIVING AND TRANSITION-TIME CONTROL

Use Optoisolation To Avoid Ground Loops

The gate-drive techniques described in the following sections illustrate the economy and flexibility the IGT brings to power control: economy, because you can drive the device's gate directly from a preceding collector, via a resistor network, for example; flexibility, because you can choose the drive circuit's impedance to yield a desired turn-off time, or you can use a switchable impedance that causes the IGT to act as a charge-controlled device requiring less than 10 nanocoulombs of drive charge for full turn-on.

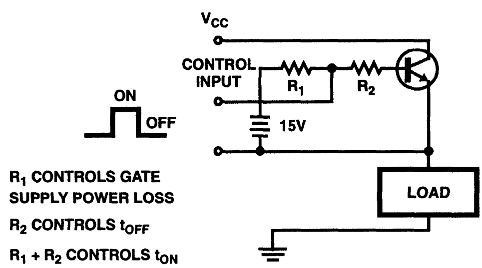


FIGURE 1B. A SECOND POWER SUPPLY

Take Some Driving Lessons

Note the IGT's straightforward drive compatibility with CMOS, NMOS and open-collector TTL/HTL logic circuits in the common-emitter configuration Figure 1A. R_3 controls the turn-off time, and the sum of R_3 and the parallel combination of R_1 and R_2 sets the turn-on time. Drive-circuit requirements, however, are more complex in the common-collector configuration Figure 1B.

In this floating-gate-supply floating-control drive scheme, R_1 controls the gate supply's power loss, R_2 governs the turn-off time, and the sum of R_1 and R_2 sets the turn-on time. Figure 1C shows another common-collector configuration employing a bootstrapped gate supply. In this configuration, R_3 defines the turn-off time, while the sum of R_2 and R_3 controls the turn-on time. Note that the gate's very low leakage allows the use of low-consumption bootstrap supplies using very low-value capacitors. Figure 1 shows two of an IGT's strong points. In the common-emitter Figure 1A, TTL or MOS-logic circuits can drive the device directly. In the common-collector mode, you'll need level shifting, using either a second power supply Figure 1B or a bootstrapping scheme Figure 1C.

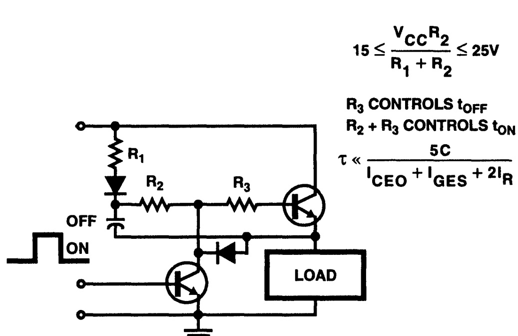


FIGURE 1C. BOOTSTRAPPING SCHEME

In the common-collector circuits, power-switch current flowing through the logic circuit's ground can create problems. Optoisolation can solve this problem (Figure 2A.) Because of the high common-mode dV/dt possible in this configuration, you should use an optoisolator with very low isolation capacitance; the H11AV specs 0.5pF maximum.

For optically isolated "relay-action" switching, it makes sense to replace the phototransistor optocoupler with an H11L1 Schmitt-trigger optocoupler (Figure 2B).) For applications requiring extremely high isolation, you can use an optical fiber to provide the signal to the gate-control photodetector. These circuit examples use a gate-discharge resistor to control the IGT's turn-off time. To exploit fully the IGT's safe operating area (SOA), this resistor allows time for the device's minority carriers to recombine. Furthermore, the recombination occurs without any current crowding that could cause hot-spot formation or latch-up pnpn action. For very fast turn-off, you can use a minimal snubber network, which allows the safe use of lower value gate resistors and higher collector currents.

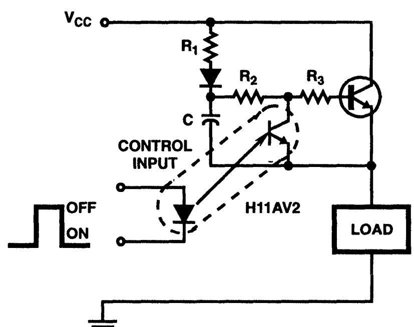


FIGURE 2A. AVOID GROUND-LOOP PROBLEMS BY USING AN OPTOISOLATOR. THE ISOLATOR IGNORES SYSTEM GROUND CURRENTS AND ALSO PROVIDES HIGH COMMON-MODE RANGE.

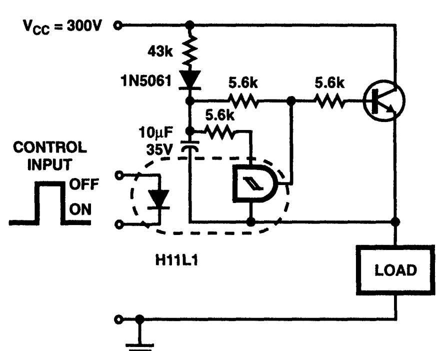


FIGURE 2B. A SCHMITT-TRIGGER OPTOISOLATOR YIELDS "SNAP-ACTION" TRIGGERING SIMILAR TO THAT OF A RELAY.

Pulse-Transformer Drive Is Cheap And Efficient

Photovoltaic couplers provide yet another means of driving the IGT. Typically, these devices contain an array of small silicon photovoltaic cells, illuminated by an infrared diode through a transparent dielectric. The photovoltaic coupler provides an isolated, controlled, remote dc supply without the need for oscillators, rectifiers or filters. What's more, you can drive it directly from TTL levels, thanks to its 1.2V, 20mA input parameters.

Available photovoltaic couplers have an output-current capability of approximately 100µA. Combined with approximately 100kΩ equivalent shunt impedance and the IGT's input capacitance, this current level yields very long switching times. These transition times (typically ranging to 1 msec) vary with the photovoltaic coupler's drive current and the IGT's Miller-effect equivalent capacitance.

Figure 3 illustrates a typical photovoltaic-coupler drive along with its transient response. In some applications, the photovoltaic element can charge a storage capacitor that's subsequently switched with a phototransistor isolator. This isolator technique - similar to that used in bootstrap circuits provides rapid turn-on and turn-off while maintaining small size, good isolation and low cost.

In common-collector applications involving high-voltage, reactive-load switching, capacitive currents in the low-level logic circuits can flow through the isolation capacitance of the control element (eg, a pulse transformer, optoisolator, piezoelectric coupler or level-shift transistor). These currents can cause undesirable effects in the logic circuitry, especially in high-impedance, low-signal-level CMOS circuits.

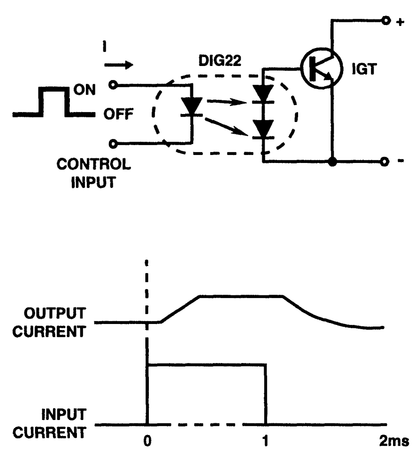


FIGURE 3. AS ANOTHER OPTICAL-DRIVE OPTION, A PHOTOVOLTAIC COUPLER PROVIDES AN ISOLATED, REMOTE DC SUPPIY TO THE IGT'S INPUT. ITS LOW 100µA OUTPUT, HOWEVER, YIELDS LONG IGT TURN-ON AND TURN-OFF TIMES.

The solution? Use fiber-optic components Figure 4 to eliminate the problems completely. As an added feature, this low-cost technique provides physical separation between the power and logic circuitry, thereby eliminating the effects of radiated EMI and high-flux magnetic fields typically found near power-switching circuits. You could use this method with a bootstrap-supply circuit, although the fiber-optic system's reduced transmission efficiency could require a gain/speed trade-off. The added bipolar signal transistor minimizes the potential for compromise.

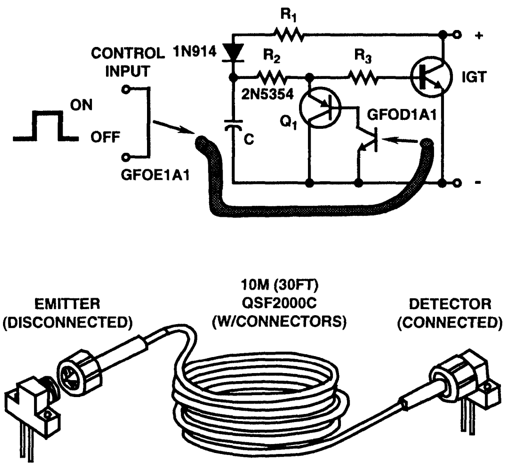


FIGURE 4. ELIMINATE EMI IN HIGH-FLUX OR NOISE ENVIRONMENTS BY USING FIBER-OPTIC COMPONENTS. THESE PARTS ALSO ALLEVIATE PROBLEMS ARISING FROM CAPACITIVE COUPLING IN ISOLATION ELEMENTS.

Piezos Pare Prices

A piezoelectric coupler operationally similar to a pulse-train drive transformer, but potentially less costly in high volume is a small, efficient device with isolation capability ranging to 4kV. What's more, unlike optocouplers, they require no auxiliary power supply. The piezo element is a ceramic component in which electrical energy is converted to mechanical energy, transmitted as an acoustic wave, and then reconverted to electrical energy at the output terminals Figure 5A.

The piezo element's maximum coupling efficiency occurs at its resonant frequency, so the control oscillator must operate at that frequency. For example, the PZT61343 piezo coupler in Figure 5B's driver circuit requires a 108kHz, ±1%-accurate astable multivibrator to maximize mechanical oscillations in the ceramic material. This piezo element has a 1W max power handling capability and a 30mA p-p max secondary current rating. The 555 timer shown provides compatible waveforms while the RC network sets the frequency.

Isolate With Galvanic Impunity

Do you require tried and true isolation? Then use transformers; the IGT's low gate requirements simplify the design of independent, transformer-coupled gate-drive supplies. The supplies can directly drive the gate and its discharge resistor Figure 6, or they can simply replace the level-shifting supplies of Figure 2. It's good practice to use pulse transformers in drive circuitry, both for IGT's and MOSFETs, because these components are economical, rugged and highly reliable.

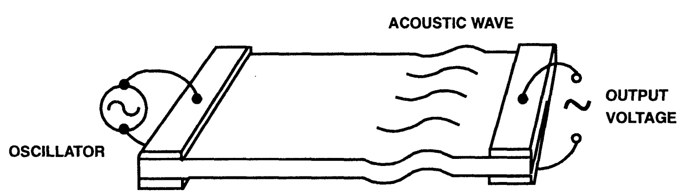


FIGURE 5A. YIELDING 4-kV ISOLATION, A PIEZOELECTRIC COUPLER PROVIDES TRANSFORMER-LIKE PERFORMANCE AND AN ISOLATED POWER SUPPLY.

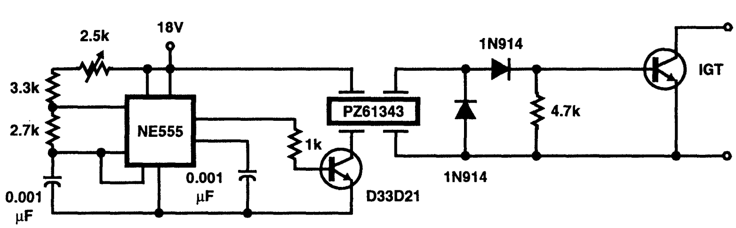


FIGURE 5B. THIS CIRCUIT PROVIDES THE DRIVE FOR THIS ARTICLE'S MOTOR-CONTROL CIRCUIT.

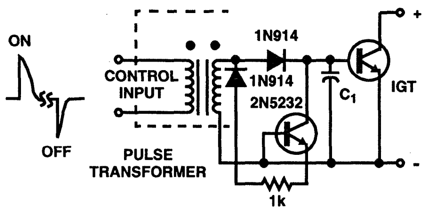


FIGURE 6A. PROVIDING HIGH ISOLATION AT LOW COST, PULSE TRANSFORMERS ARE IDEAL FOR DRIVING THE IGT. AT SUFFICIENTLY HIGH FREQUENCIES, C_1 CAN BE THE IGT'S GATE-EMITTER CAPACITANCE ALONE.

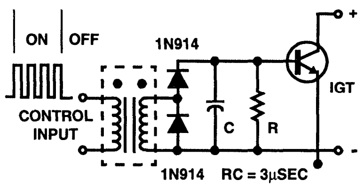


FIGURE 6B. A HIGH-FREQUENCY OSCILLATOR IN THE TRANSFORMER'S PRIMARY YIELDS UNLIMITED ON-TIME CAPABILITY.

In the pulse-on, pulse-off method Figure 6A, C_1 stores a positive pulse, holding the IGT on. At moderate frequencies (several hundred Hertz and above), the gate-emitter capacitance alone can store enough energy to keep the IGT on; lower frequencies require an additional external capacitor. Use of the common-base n-p-n bipolar transistor to discharge the capacitance minimizes circuit loading on the capacitor. This action extends continuous on-time capability without capacitor refreshing; it also controls the gate-discharge time via the 1kΩ emitter resistor.

Piezoelectric Couplers Provide 4-kV Isolation

Using a high-frequency oscillator for pulse-train drive Figure 6B yields unlimited on-time capability. However, the scheme requires an oscillator that can be turned on and off by the control logic. A diode or zener clamp across the transformer's primary will limit leakage-inductance flyback effects. To optimize transformer efficiency, make the pulses' voltage x time products equal for both the On and the Off pulses. In situations where the line voltage generates the drive power, a simple relaxation oscillator using a programmable unijunction transistor can derive its power directly from the line to provide a pulse train to the IGT gate.

The circuit shown in Figure 7 accommodates applications involving lower frequencies (a few hundred Hertz and below). The high oscillator frequency (greater than 20kHz) helps keep the pulse transformer reasonably small. The voltage-doubler circuitry improves the turn-on time and also provides long on-time capability. Although this design uses only a 5V supply on the primary side of a standard trigger transformer, it provides 15V gate-to-emitter voltage.

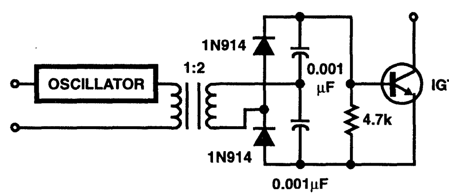


FIGURE 7. THIS DRIVING METHOD FOR LOW-FREQUENCY SWITCHING PROVIDES 15V TO THE IGT'S GATE, YET WORKS FROM A 5V SUPPLY. THE HIGH DRIVE VOLTAGE RESULTS IN FAST IGT TURN-ON TIME.

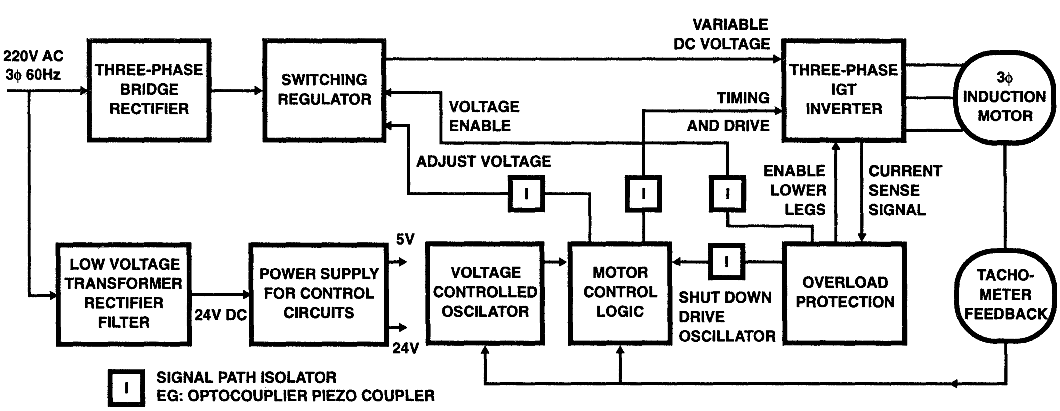


FIGURE 8. THIS 6-STEP 3-PHASE-MOTOR DRIVE USES THE IGT-DRIVE TECHNIQUES DESCRIBED IN THE TEXT. THE REGULATOR ADJUSTS THE OUTPUT DEVICES' INPUT LEVELS; THE VOLTAGE-CONTROLLED OSCILLATOR VARIES THE SWITCHING FREQUENCY AND ALSO PROVIDES THE CLOCK FOR THE 3-PHASE TIMING LOGIC. THE V/F RATIO STAYS CONSTANT TO MAINTAIN CONSTANT TORQUE REGARDLESS OF SPEED.

Polyphase motors, controlled by solid-state, adjustable-frequency ac drives, are used extensively in pumps, conveyors, mills, machine tools and robotics applications. The specific control method could be either 6-step or pulse-width modulation. This section describes a 6-step drive that uses some of the previously discussed drive techniques (see page 11, "Latch-Up: Hints, Kinks and Caveats").

Figure 8 defines the drive's block diagram. A 3-phase rectifier converts the 220V ac to dc; the switching regulator varies the output voltage to the IGT inverter. At the regulator's output, a large filter capacitor provides a stiff voltage supply to the inverter.

The motor used in this example has a low slip characteristic and is therefore very efficient. You can change the motor's speed by varying the inverter's frequency. As the frequency increases, however, the motor's air-gap flux diminishes, reducing developed-torque capability. You can maintain the flux at a constant level (as in a dc shunt motor) if you also vary the voltage so the V/F ratio remains constant.

Fiber-Optic Drive Eliminates Interference

In the example given, the switching regulator varies the IGT inverter's output by controlling its dc input; the voltage-controlled oscillator (VCO) adjusts the inverter's switching frequency, thereby varying the output frequency. The VCO also drives the 3-phase logic that provides properly timed pulsed outputs to the piezo couplers that directly drive the IGT.

Sensing the dc current in the negative rail and inhibiting the gate signal protect the IGT from overload and shoot-through (simultaneous conduction) conditions. If a fault continues to exist for an appreciable period, inhibiting the switching regulator causes the inverter to shut off. The inverter's power-output circuit is shown in Figure 9A; the corresponding timing diagrams show resistive-load current waveforms that indicate the 3-phase power Figure 9B and waveforms of the output line voltage and current Figure 9C.

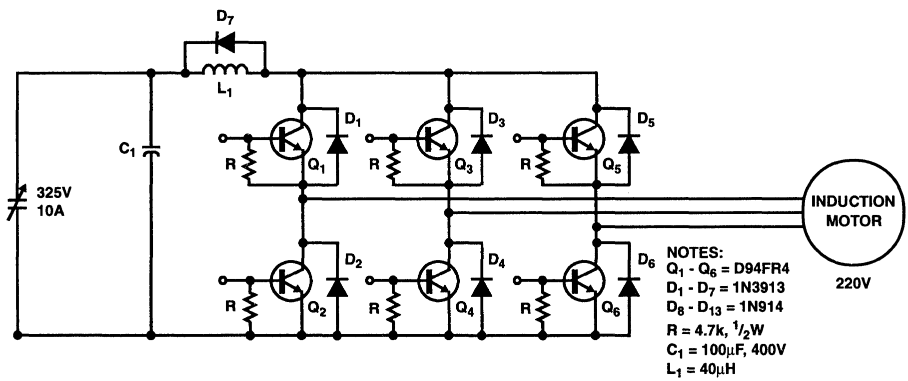


FIGURE 9A. THE POWER INVERTER'S DRIVE CIRCUIT USES SIX IGTS TO DRIVE A 2-HP MOTOR.

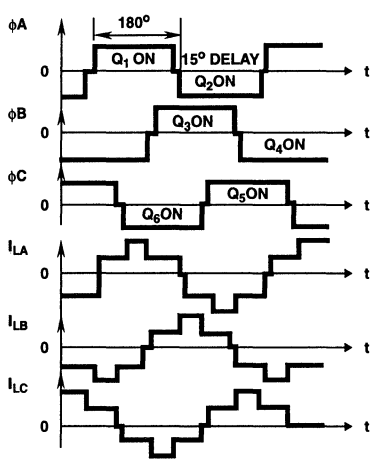


FIGURE 9B. THE TIMING DIAGRAM SHOWS THAT EACH IGT CONDUCTS FOR 165° OF EVERY 360° CYCLE; THE DELAY IS NECESSARY TO AVOID CROSS CONDUCTION.

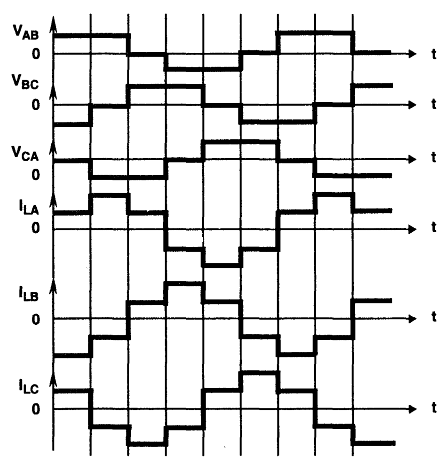


FIGURE 9C. THE THREE WINDINGS' VOLTAGES AND CURRENTS ARE SHOWN. NOTE THAT ALTHOUGH COSTLY SNUBBER NETWORKS ARE ELIMINATED, FREEWHEELING DIODES ARE NEEDED; THE IGTS HAVE NO INTRINSIC OUTPUT DIODE.

In Figure 9's circuit, it appears that IGTs Q_1 through Q_6 will conduct for 180°. However, in a practical situation, it's necessary to provide some time delay (typically 10° to 15°)during the positive-to-negative transition periods in the phase current. This delay allows the complementary IGTs to turn off before their opposite members turn on, thus preventing cross conduction and eventual destruction of the IGTs.

Because of the time delay, the maximum conduction time is 165° of every 360° period. Because the IGTs don't have an integral diode, it's necessary to connect an antiparallel diode externally to allow the freewheeling current to flow. Inductor L_1 limits the di/dt during fault conditions; freewheeling diode D_7 clamps the IGT's collector supply to the dc bus.

The peak full-load line current specified by the motor manufacturer determines the maximum steady-state current that each transistor must switch. You must convert this RMS-specified current to peak values to specify the proper IGT. If the input voltage regulator had a fixed output voltage and a constant frequency, each IGT would be required to supply the starting locked-rotor current to the motor. This current could be as much as 15 times the full-load running current.

It's impractical, however, to rate an inverter based on locked-rotor current. You can avoid this necessity by adjusting the switching regulator's output voltage and by providing a fixed output-current limit slightly higher than the maximum full-load current. This way, the current requirements during start-up will never exceed the current capability of an efficiently sized inverter.

For example, consider a 2-hp, 3-phase induction motor specifying V_L at 230V RMS and full-load current (I_{LFL}) at 6.2A RMS. For the peak current of 8.766A, you can select IGT type D94FR4. This device has a reverse-breakdown SOA (RBSOA) of 10A, 500V for a clamped inductive load at a junction temperature of 150°C. A 400V IGT could also do the job, but the 500V choice gives an additional derating safety margin. You must set the current limit at 9A to limit the in-rush current during start-up. Note that thanks to the IGT's adequate RBSOA, you don't need turn-off snubbers.

Use 6-Step Drive For Speed-Invariant Torque

Figure 10A shows the inverter circuit configured for this example. Diodes D_1 through D_6 carry the same peak current as the IGTs; consequently, they're rated to handle peak currents of at least 8.766A. However, they only conduct for a short time (15° to 20° of 180°), so their average-current requirement is relatively small.

External circuitry can control the IGT's current fall time. Resistor R controls t_{F1} Figure 10B; there's no way to control t_{F2}, an inherent characteristic of the selected IGT. In this example, a 4.7-kΩ gate-to-emitter resistor provides the appropriate fall time. The choice of current-limiting inductor L_1 is based on the IGT's overload-current rating and the action time (the sum of the sensor's sensing and response time and the IGT's turn-off time) in fault conditions.

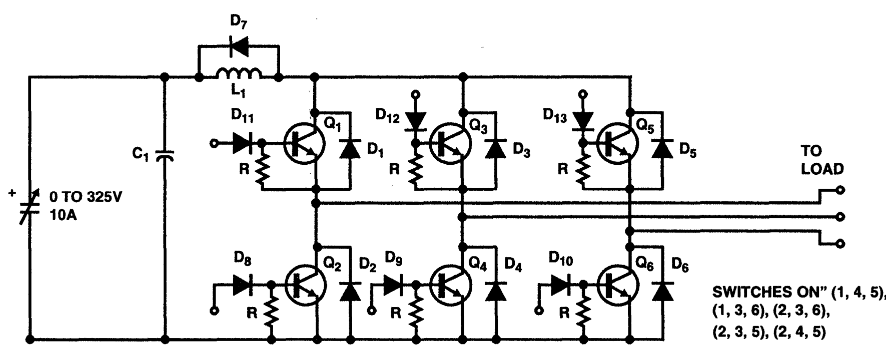


FIGURE 10A. COMPONENT SELECTION IS IMPORTANT. THE IGT SELECTED CIRCUIT HANDLES 10A, 500V AT 150°C. THE ANTI-PARALLEL DIODES HAVE A SIMILAR CURRENT RATING.

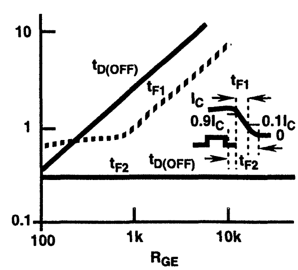


FIGURE 10B. SELECT R TO YIELD THE DESIRED TURN-OFF TIME. FINALLY, L1'S VALUE DETERMINES THE FAULT-CONDITION ACTION TIME.

You could use a set of flip flops and a multivibrator to generate the necessary drive pulses and the corresponding 120° delay between the three phases in Figure 10's circuit. A voltage-controlled oscillator serves to change the inverter's output frequency. In this circuit, IGTs Q_1, Q_3 and Q_5 require isolated gate drive; the drive for Q_2, Q_4 and Q_6 can be referred to common. If you use optocouplers for isolation, you'll need three isolated or bootstrap power supplies (in addition to the 5V and 24V power supplies) to drive the IGTs. Another alternative is to use transformer coupling.

165° Conduction Prevents Shoot-Through

Consider, however, using Figure 11A's novel, low-cost circuit. It uses a piezo coupler to drive the isolated IGT. As noted, the coupler needs a high-frequency square wave to induce mechanical oscillations in its primary side. The 555 oscillator provides the necessary 108-kHz waveform; its output is gated according to the required timing logic and then applied to the piezo coupler's primary. The coupler's rectified output drives the IGT's gate; the 4.7kW gate-to-emitter resistor provides a discharge path for C_{GE} during the IGT's turn-off. The circuit's logic-timing diagram is shown in Figure 11B.

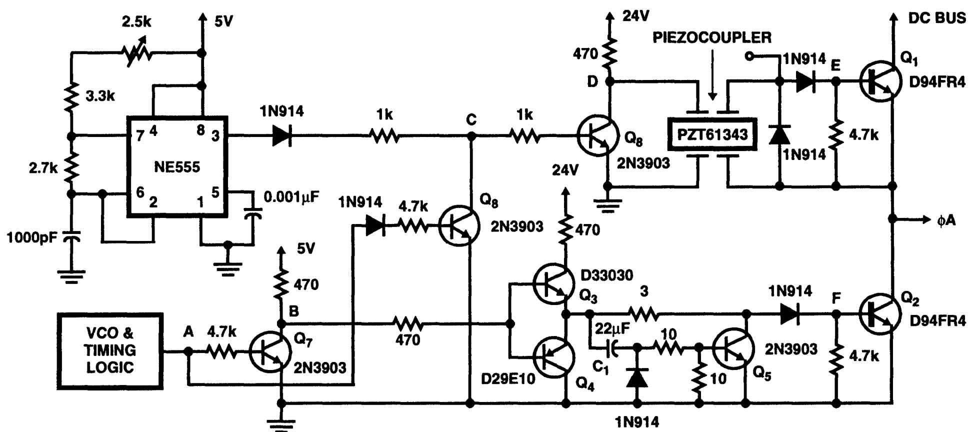


FIGURE 11A. PROVIDING PROPERLY TIMED DRIVE TO THE IGTS, THE CIRCUIT USES PIEZO COUPLING TO THE UPPER POWER DEVICE. THE 3-TRANSISTOR DELAY CIRCUIT PROVIDES THE NEEDED 15° LAG TO THE LOWER IGT TO AVOID CROSS CONDUCTION.

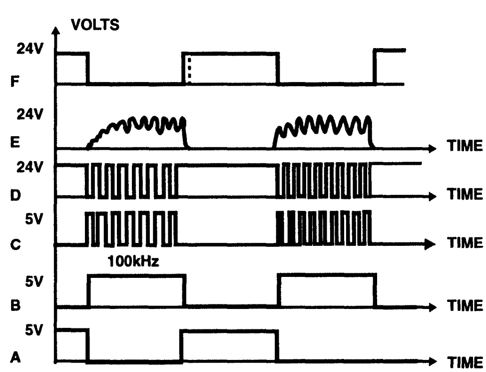


FIGURE 11B. THE TIMING DIAGRAM SHOWS THE 555'S 108-KHz DRIVE TO THE PIEZO DEVICE AND THE LATTER'S SLOW RESPONSE.

The piezo coupler's slow response time Figure 12A contributes approximately 2° to the 15° to 20° turn-on/turn-off delay needed to avoid shoot-through in the complementary pairs. The corresponding collector current is shown in Figure 12B. C_1 and its associated circuitry provide the remaining delay as follows.

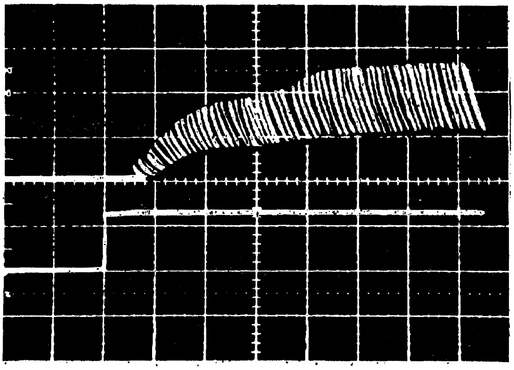


FIGURE 12A. THE PIEZO COUPLER'S SLOW RESPONSE IS NOT A DISADVANTAGE IN THIS ARTICLE'S CIRCUIT. IN FACT, IT CONTRIBUTES 2° TO THE REQUIRED 15° TURN-ON/TURN-OFF DELAY.

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200µSEC/DIV
B	5V/DIV	200µSEC/DIV

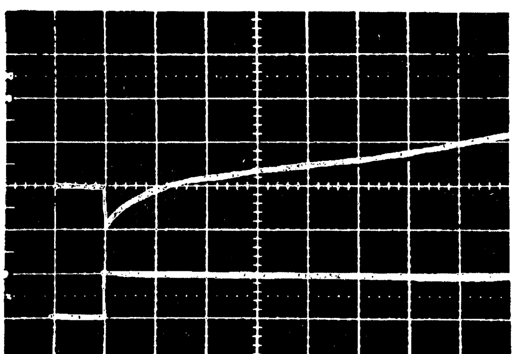


FIGURE 12B. THE DRIVEN IGT'S COLLECTOR CURRENT IS SHOWN.

TRACE	VERTICAL	HORIZONTAL
A	3A/DIV	200µSEC/DIV
B	5V/DIV	200µSEC/DIV

When Q_3's base swings negative, C_1 - at this time discharged - turns on Q_5. Once C_1 is charged, Q_5 turns off, allowing a drive pulse to turn the IGT on. When Q_7's base goes to ground, Q_4 turns on and discharges C_1, initiating the IGT's turn-off. Figure 13 shows the motor current and corresponding line voltage under light-load Figure 12A and full-load Figure 12B conditions.

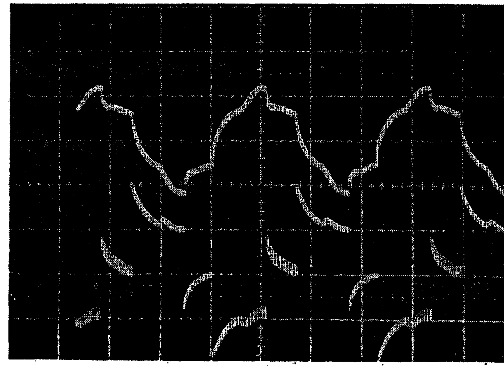


FIGURE 13A. MOTOR CURRENT AND VOLTAGE ARE SHOWN HERE, FOR LIGHT LOADS

TRACE	VERTICAL	HORIZONTAL
A	1A/DIV	1mSEC/DIV
B	50V/DIV	1mSEC/DIV

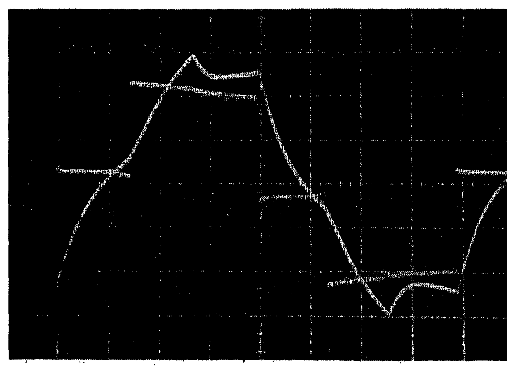


FIGURE 13B. MOTOR CURRENT AND VOLTAGE ARE SHOWN HERE, FOR HEAVY LOADS.

TRACE	VERTICAL	HORIZONTAL
A	3A/DIV	2mSEC/DIV
B	100V/DIV	2mSEC/DIV

To complete the design of the 6-step motor drive, it's necessary to consider protection circuitry for the output IGTs. The drive receives its power from a switching supply already containing provisions for protection from line over-voltage and under-voltage and transient effects. However, you still have to guard the power switches against unwanted effects on the output lines and the possibility of noise or other extraneous signals causing gate-drive timing errors.

The best protection circuit must match the characteristics of the power switch and the circuit's bias conditions. The IGT is very rugged during turn-on and conduction, but it requires time to dissipate minority carriers when turning off high currents and voltages. An analysis of the possible malfunction conditions shows that a current-sensing over current-protection circuit (combined with a di/dt-limiting inductor) provides the most complete protection.

Tailor R_{GE}'s Value To Avoid Latch-up

To protect against turn-on into a shorted output, you must coordinate the response time of the sensing circuit and the di/dt-limiting inductance. Moreover, the sensing must be accurate, allow tight control, and have low losses and low cost. The system in Figure 14 uses such a sensor - a 2mΩ resistor formed from 1 inch of #24 AWG copper wire with Kelvin contacts. The voltage across this resistor is chopped and ac-amplified, using the 108-kHz gate-supply oscillator as a timing source.

Low-Cost Sensor Monitors Load Current

Amplified signals exceeding 1V p-p amplitude set a latch, removing gate drive from the IGTs and simultaneously turning off the switching regulator via the 3524 control IC. Automatic reset occurs after 10 msec, and it repeats if the line current stays below the set limit during the high-voltage supply's turn-on. If the restarting line current is higher than normal, the circuit latches off during the first reset attempt and stays off until the mains voltage shuts down.

The chopped current-sensing technique proves less costly and performs better than Hall-effect sensing systems. Figure 15 gives a detailed schematic of the protection circuitry. It has sufficient bandwidth to provide a 10μsec system response time and features ±2% reproducibility. The circuit is cost effective, easily meets system accuracy and speed requirements, and operates from the system's frequency source and power supply (adding only 0.5W dissipation). The dominant cost-determining factors are the di/dt inductor and the associated flyback diode (required for most protection schemes anyway).

An overview of the protection circuit starts at the current-sensing resister in the high-voltage supply's ground return Figure 15A. The two H11F3 bilateral analog FET optoisolators chop the voltage across the resistor at a 50% duty cycle. The H11F3s' inputs are driven by a square wave derived from a 2-transistor bistable multivibrator that's clocked from the 108kHz 555 timer Figure 15B serving as the piezoelectric couplers drive source.

The chopped voltage waveform, a square wave of 1mV peak amplitude per ampere of summed motor current, is amplified 50 to 100 times by a 2-transistor amplifier; its peak value is then compared to a 1V reference via a Darlington-SCR comparator. The temperature coefficients of the reference and comparator compensate for the copper-wire sensing resistors TCR (approximately 400 ppm/°C). Note, however, that you can change the TC characteristics to suit a particular system's temperature requirements.

If the amplified signal exceeds the comparator's reference level, the SCR latches on, drawing the lower IGT power switches' gates Low (via the steering diodes) and turning the two H11AV2 optoisolators on. These isolators, featuring extremely low dielectric capacitance, remove the 108kHz signal from the piezo couplers' inputs, thereby halting power flow to the upper IGTs' gates. The isolators also supply 5V to the shutdown pin on the 3524 regulator Figure 15C that controls the variable high-voltage supply, thereby turning the inverters' input power off.

Providing three independent shutdown functions (lower and upper IGTs and high-voltage supply) yields foolproof protection from any foreseeable failure. An RC network times the protection circuit's reset (an action effected by firing an ST4 pnpn threshold switch) by using the timing capacitor to turn the SCR comparator off. If the load current remains above limit during the restart time, both the ST4 and the SCR remain on, preventing the reset from repeating. This action ensures permanent shutdown and prevents repeated power cycling of the power switches under shorted-load conditions.

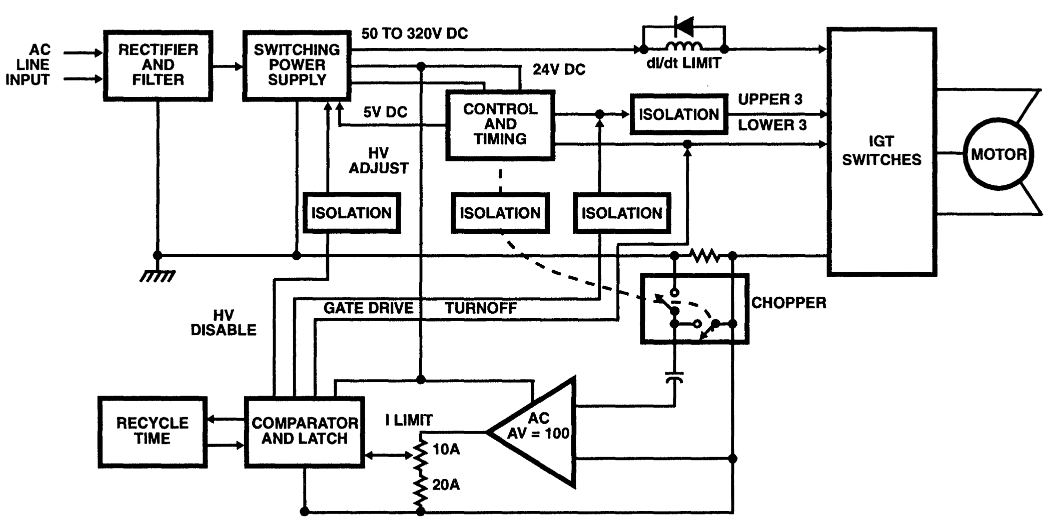


FIGURE 14. THE LOWEST COST SENSOR IMAGINABLE, A PIECE OF COPPER WIRE SERVES AS THE CURRENT MONITOR IN THIS SYSTEM. THE CHOPPED AND AMPLIFIED VOLTAGE DROP ACROSS THE WIRE TRIGGERS A GATE-DRIVE SHUT-OFF CIRCUIT UNDER FAULT CONDITIONS.

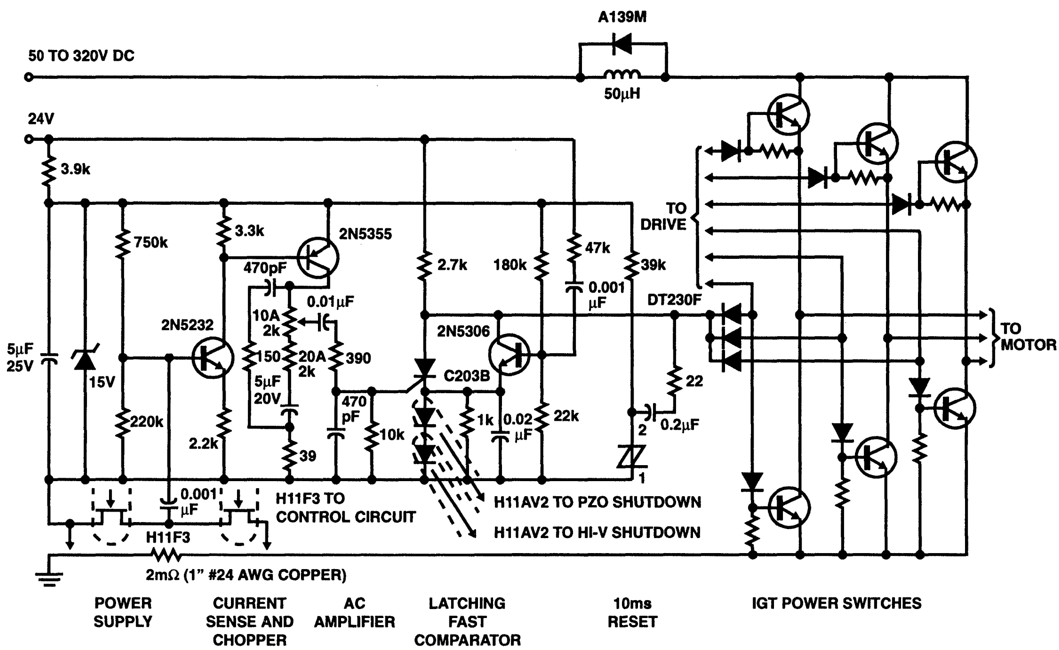


FIGURE 15A. THIS ALL-ENCOMPASSING PROTECTION SYSTEM PROVIDES THREE INDEPENDENT SHUTDOWN FUNCTONS - ONE EACH FOR THE UPPER AND LOWER IGTS AND THE HIGH-VOLTAGE SUPPLY.

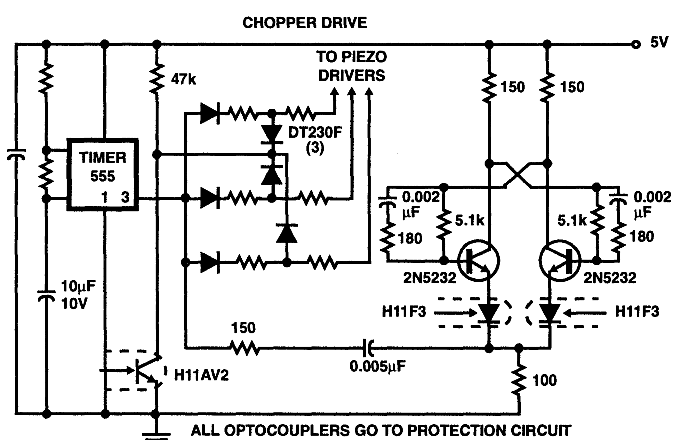


FIGURE 15B. THIS CIRCUIT PROVIDES CHOPPER DRIVE FOR THE COPPER-WIRE SENSOR IN FIGURE 15A.

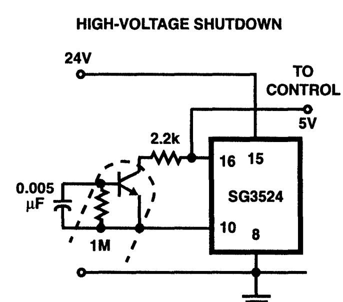


FIGURE 15C. SHOWS THE HIGH-VOLTAGE SHUTDOWN CIRCUIT.

Latch-Up: Hints, Kinks and Caveats

The IGT is a rugged device, requiring no snubber network when operating within its published safe-operating-area (SOA) ratings. Within the SOA, the gate emitter voltage controls the collector current. In fact, the IGT can conduct three to four times the published maximum current if it's in the ON state and the junction temperature is +150°C maximum.

However, if the current exceeds the rated maximum, the IGT could lose gate control and latch up during turn-off attempts. The culprit is the parasitic SCR formed by the pnpn structure shown in Figure 16. In the equivalent circuit, Q_1 is a power MOSFET with a normal parasitic transistor (Q_2) whose base-emitter junction is shunted by the low-value resistance R_1.

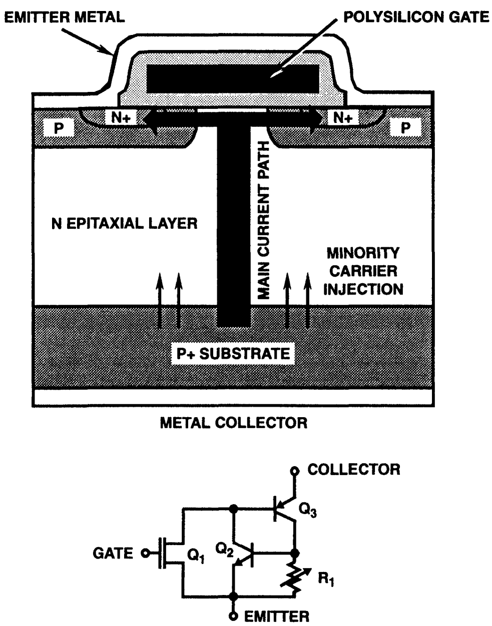


FIGURE 16. THE IGT'S PARASITIC SCR IS RESPONSIBLE FOR THE DEVICE'S LATCH-UP CHARACTERISTICS.

For large current overloads, the current flowing through R_1 can provoke SCR triggering. In the simplest terms, R_1 represents the equivalent of a distributed resistor network, whose magnitude is a function of Q_2's V_{CE}. During normal IGT operation, a positive gate voltage (greater than the threshold) applied between Q_1's gate and source turns the FET on. The FET then turns on Q_3 (a pnp transistor with very low gain), causing a small portion of the total collector current to flow through the R_1 network.

To turn the IGT off, you must reduce the gate-to-emitter voltage to zero. This turns Q_1 off, thus initiating the turn-off sequence within the device. Total fall time includes current-fall-time one (t_{F1}) and current-fall-time two (t_{F2}) components. The turn-off is a function of the gate-emitter resistance, Q_3's storage time and the value of V_{GE} prior to turn-off. Device characteristics fix both the delay time and the fall time.

Forward-Bias Latch-Up

Within the IGT's current and junction-temperature ratings, current does not flow through Q_2 under forward-biased conditions. When the current far exceeds its rated value, the current flow through R_1 increases and Q_3's V_{CE} also increases because of MOSFET channel saturation. Once Q_3's $I_C R_1$ drop exceeds Q_2's $V_{BE(ON)}$, Q_2 turns on and more current flow bypasses the FET.

The positive feedback thus established causes the device to latch in the forward-biased mode. The value of I_C at which the IGT latches on while in forward conduction is typically three to four times the device's maximum rated collector current. When the collector current drops below the value that provokes Q_2 turn-on, normal operation resumes if chip temperature is still within ratings.

If the gate-to-emitter resistance is too low, the Q_2-Q_3 parasitic SCR can cause the IGT to latch up during turn-off. During this period, R_{GE} determines the drain-source dV/dt of power MOSFET Q_1. A low R_1 causes a rapid rise in voltage - this increases Q_2's V_{CE}, increasing both R_1's value and Q_2's gain.

Because of storage time, Q_3's collector current continues to flow at a level that's higher than normal for the FET bias. During rapid turn-off, a portion of this current could flow in Q_2's base-emitter junction, causing Q_2 to conduct. This process results in device latch-up; current distribution will probably be less uniform than in the case of forward-bias latch-up.

Because the gains of Q_2 and Q_3 increase with temperature and V_{CE}, latching current - high at +25°C - decreases as a function of increasing junction temperature for a given gate-to-emitter resistance.

How do you test an IGT's turn-off latching characteristic? Consider the circuit in Figure 17. Q_1's base-current pulse width is set approximately 2µsec greater than the IGT's gate-voltage pulse width. This way, the device under test (DUT) can be switched through Q_1 when reverse-bias latch-up occurs. This circuit allows you to test an IGT's latching current nondestructively.

The results? Clamped-inductive-load testing with and without snubbers reveals that snubbering increases current handling dramatically: With RGE = 1kΩ, a 0.02µF snubber capacitor increases current capability from 6A to 10A; with RGE = 5kΩ, a 0.09µF snubber practically doubles capacity (25A vs 13A).

Conclusions? You can double the IGT's latching current by increasing RGE from 1kΩ to 5kΩ, and double it again with a polarized snubber using CS < 0.1µF. The IGT is therefore useful in situations where the device must conduct currents of five to six times normal levels for short periods.

Finally, you can also use the latching behavior to your advantage under fault conditions. In other words, if the device latches up during turn-off under normal operation, you could arrange it so that a suitable snubber is switched electronically across the IGT.

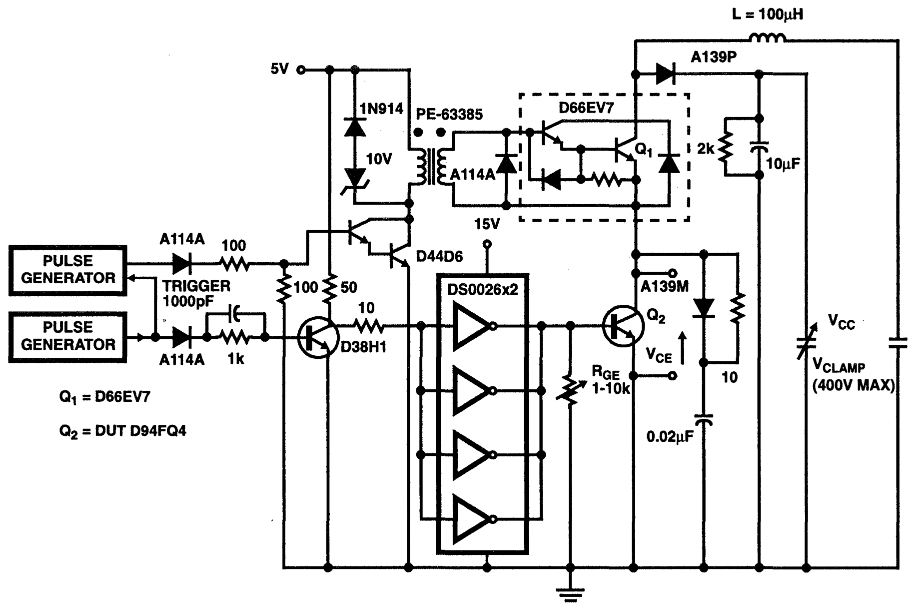


FIGURE 17. USE THIS LATCHING-CURRENT TESTER TO TEST IGTS NONDESTRUCTIVELY. Q_1'S BASE-DRIVE PULSE WIDTH IS GREATER THAN THAT OF THE IGT'S GATE DRIVE, SO THE IGT UNDER TEST IS SWITCHED THROUGH Q_1 WHEN REVERSE-BIAS LATCH-UP OCCURS.

No. AN9319 September 1993

Harris Power

Parallel Operation Of Insulated Gate Transistors

Author: Sebald R. Korn, Consulting Applications Engineer

In the November issue of Powertechnics, the general considerations of paralleling semiconductor switches were presented. Some of the important factors include the characteristics of different types of load reactances and the action of the switching device during its turn-on delay, rise time and turn-off delay times. Different types of switching devices must be handled differently when operated in parallel. Power bipolar transistors, SCRs, MOSFETs and IGTs all have different characteristics which must be taken into consideration. The IGT transistor combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors. Like MOSFETs, the output characteristics of IGTs are generated by plotting collector-emitter current, collector-emitter voltage and gate voltage. Unlike the MOSFET, there is an offset voltage generated by the collector-emitter junction of the npn transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSFET. A steady state equivalent circuit is shown in Figure 1. Total device current equals MOSFET current (I_{MOS}) plus bipolar current (I_{BIT}) and since the MOSFET current is the base current of the pnp, these current components are related by the gain of the pnp.

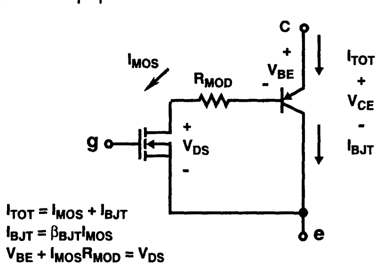


FIGURE 1. N-CHANNEL IGT TRANSISTOR STEADY STATE EQUIVALENT CIRCUIT

To understand the unusual behavior of its temperature coefficient, negative at low current, almost zero at normal current, and positive at high current, we analyzed the IGT by treating the two branch currents comprising the conduction path as two separated devices. The IGT's on-state voltage drop is composed of the MOSFET voltage drop plus the bipolar V_{BE} drop apparently parallel by a pnp-transistor. Note that the only part of the bipolar in parallel to the MOSFET and modulation resistance is the base-collector junction, but the base-emitter junction is common to both branches.

We also know from measurements, the MOSFET's temperature coefficient in the epi-resistance is positive. We know further that as the device temperature increases, the bipolar transistor's gain increases, the V_{BE} drop decreases, which both tend to reduce on-voltage drop. On the other hand, the MOSFET and epi-resistance voltage drop will increase with temperature, tending to increase on-voltage voltage.

These effects cancel and the net result is that the IGT exhibits much less variation of on-voltage voltage with temperature than either bipolars or MOSFETs. The temperature coefficient goes from a bipolar like negative (at low currents) to zero (at rated current) and to a MOSFET-like positive coefficient as current density increases (Figure 2).

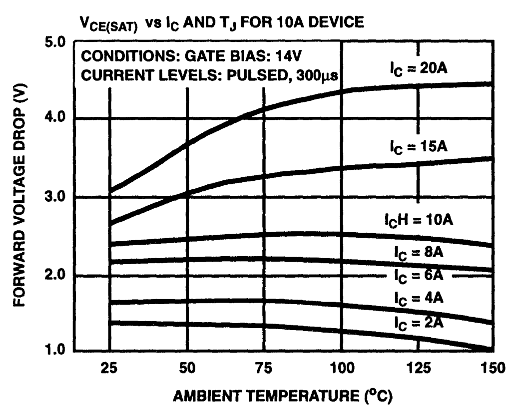


FIGURE 2. V_{CE} vs T_A OF IGT, AT DIFFERENT COLLECTOR CURRENT

Turn-On Switching Performance

Like the MOSFET, the IGT gate presents a capacitive load to the drive circuit. The IGT capacitive elements and their typical variation with voltage is analogous to the MOSFET, hence the IGT turn-on interval can be divided into three distinct regions (refer to Figure 3). In region I, the input capacitance is charged until the gate voltage reaches the value needed to initiate collector current conduction. In region II, turn-on is essentially completed as the collector voltage falls rapidly to the 10% level. The effective capacitance increases dramatically in this region due to the Miller effect. In region III, the collector voltage slowly settles to its saturation level. At the start of Section III, the effective input capacitance remains high because as the collector voltage is driven below the gate voltage, the polarity of the collector gate voltage reverses and C_{GC} increases dramatically. When the collector reaches the saturation voltage level, the gate rises to the gate-emitter supply level (typically 15 volts).

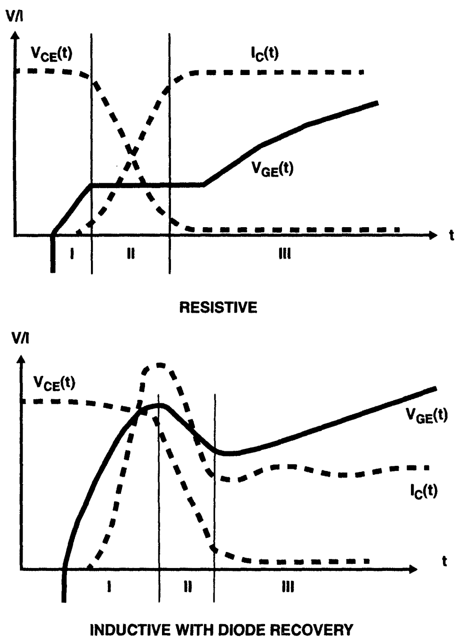


FIGURE 3. IGT TRANSISTOR TURN ON WAVEFORM

Turn-Off Switching Performance

The turn off interval is also composed of three regions as shown in Figure 4 for the case of an inductive load. Region I represents the discharge of the gate to the point where the gate voltage just sustains the collector current.

Region II corresponds to reversing the voltage on C_{GC} whose value is very high at this point. The gate voltage changes very little during this period and the collector-emitter voltage begins to rise slightly. Taken together, regions I and II represent a turn-off delay. Referring back to the equivalent circuit of Figure 1 when the device is fully on, the MOSFET voltage prevents the base-collector junction of the pnp from becoming forward biased. Thus the pnp contributes no significant storage time delay during turn off. In region III, the collector voltage rises rapidly at a rate controlled by the amount of current supplied by the gate drive to reverse charge C_{GC}.

The turn off current fall exhibits two distinct phases: an initial fast drop followed by a slow exponential fall. The initial fast drop is due to the fast cutoff of the MOSFET current. After the MOSFET channel cuts off, the pnp transistor undergoes an open base turn off. The gate drive circuit only controls the initial turn off delay and the slope of the MOSFET current fall by how fast it withdraws gate charge. The pnp exponential turn off tail is a characteristic of the device design.

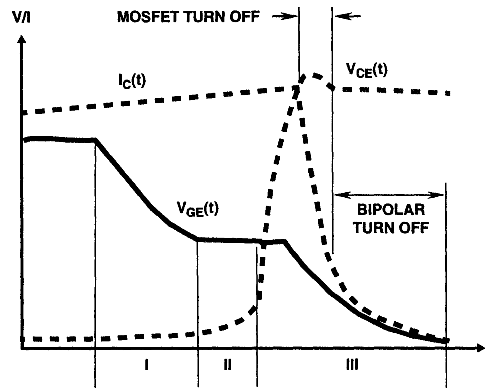


FIGURE 4. IGT TRANSISTOR TURN OFF WAVEFORMS

Device Design To Optimize Turn Off

The bipolar current tail was the cause of the excessive switching times of the first-generation IGT. Turn off of the pnp transistor is a function of the stored base charge and the lifetime of carriers in the base region.

Shortening the pnp turn-off time involves decreasing the bipolar current component and/or reducing the carrier lifetime. The carrier recombination rate can be reduced by localized techniques such as electron or proton irradiation. In addition to a faster decay rate, an irradiated device will have a power pnp gain. By decreasing the bipolar current component, the MOSFET current and the amount of initial drop in the turn-off waveform both increase, resulting in a substantially lower current level for the bipolar decay.

Turn-Off SOA Optimization

The dynamic equivalent circuit of the IGT includes a parasitic pnp thyristor (Figure 5). When the sum of the current gains of the npn and pnp exceeds one, the four layer pnp structure latches on and gate control is lost. The npn is effectively shorted by the emitter metal but there is a finite well resistance, P_{WELL}, below the surface. The npn gain is very low until sufficient current flows through P_{WELL} to exceed its V_{BE} threshold. Thus, $V_{BE(ON)} = (I_{WELL})(P_{WELL})$ provides a latching criteria.

The R_{WELL} resistance increases with temperature due to falling carrier mobility in the P_{WELL} region. The I_{WELL} current is the pnp collector current and hence depends upon the pnp gain. I_{WELL} can be increased dramatically by displacement currents from high dv/dt. Increased temperature causes increased pnp gain and hence increased I_{WELL}. The $V_{BE(ON)}$ threshold will decrease with increasing temperature.

Clearly, high-temperature, fast turn-off of an inductive load represents a worse case test. Second generation IGT are SOA limited and not latching-current limited. They will fail due to operation outside the power related current at 150°C under the fast (R_{GE} = 100Ω), inductive turn off conditions. This performance has been achieved by minimizing P_{WELL} through cell design and the addition of a deep p+ diffusion and by utilizing the buffer layer structure to lower pnp gain.

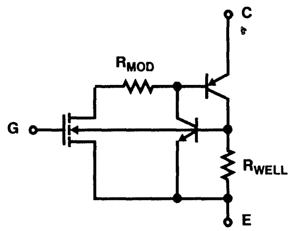


FIGURE 5. DYNAMIC EQUIVALENT CIRCUIT OF THE IGT TRANSISTOR

Results Of Paralleling IGT

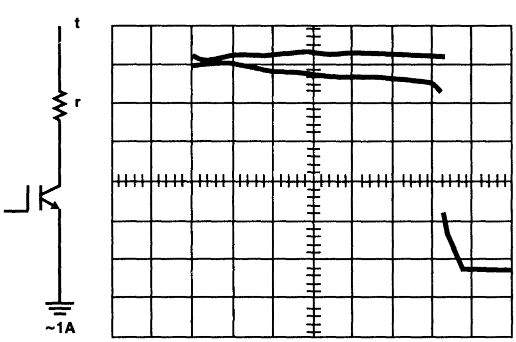
From our experience with paralleling devices like bipolars and MOSFETs, there seemed to be no reason why IGTs should not perform reasonably well.

To perform the measurement, we used the IGT-4E10 and the IGT-4E11 both rated at I_C = 10A at T_C = 100°C and a V_{CE} = 500V. We also used a 20A device the IGT-6E21.

The parameters we considered important for parallel operation, the saturation voltage $V_{CE(SAT)}$ which we measured at different current levels and a gate voltage V_{GE} = 14V. Gate threshold voltage ($V_{G(TH)}$) which we measured at 250μA and 1A (at that level, we can call it an input voltage versus output current) and transconductance (G_{FS}).

TABLE 1.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
44 48	2.35 2.55	5.38 5.50	4.3 3.8	10.5 9.5	51 51	225 236	250 230	402 381
Δ%	85%	22%	13%	10%	0%	4.8%	8.6%	5.5%



DEVICE 44/48 (2A/DIV 2μs/DIV)

The circuit we used consisted of HP pulse generators 222 and 214A driving a logic gate (7402N) and the memory driver D50026 connected to the gate through resistors R_1 and R_2 to the gate of the IGT, a Tektronix scope 7854 and current probes 6021 and 6302.

Device 44 and 48 were selected as an average combination and deltas of the different parameters can be seen in Table 1. Parallel operation is good, delta I = 1A at 9.5A and 10.5A in each device. We see clearly the FET and bipolar turn off.

The same devices were used to increase the current to about 40A, checking for latching problems, which did not occur.

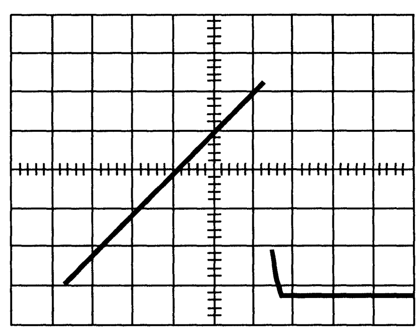
We then changed the gate resistor from 50Ω to 4.7Ω and increased case temperature to the rated 150°C. Still no problems became apparent. Note that the peak current was over four times the rated continuous current.

The same pair was also used to switch on an inductive load (L = 182μH). Excellent parallel operation is achieved with this combination. Even 500ns resolution did not reveal any problems.

The first interesting combination 14 specified T_{FMAX} = 1μs and 15 specified t_{FMAX} = 605μs. The trade-off in switching speed versus $V_{CE(SAT)}$ can be seen in Table 2.

TABLE 2A.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
19 20	2.15 2.15	5.55 4.95	4.7 4.3	10.2 9.8	58 46	244 252	277 269	835 871
Δ%	0%	12%	9%	4%			2.9%	4.3%



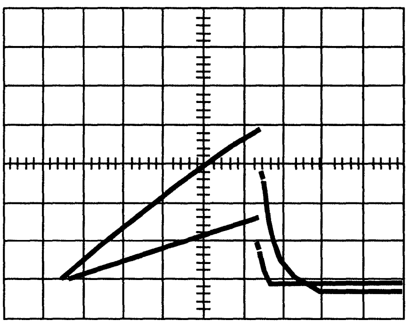
DEVICE 14/15 60% DIFFERENCE ≈ $V_{CE(SAT)}$ AND LARGE DIFFERENCE IN SWITCHING TIME

Excellent parallel operation is achieved with this combination, even the 500ns resolution does not reveal any problems.

Device 20 having the lower $V_{CE(SAT)}$ and lower $V_{G(TH)}$ is taking the higher share of current. Both parameters $V_{CE(SAT)}$ and $V_{G(TH)}$ are important in the overall performance. Turn off showing is excellent, but the 500ns time scale shows the result of the difference in the t_{DELAY} off, of 23ns and the difference in device 15 and 16, are the devices having low $V_{CE(SAT)}$ and long turn off times. If paralleled with the proper device (same type), excellent parallel operation is achieved.

TABLE 2B.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
14	2.25	5.75	4.3	6.0	53	264	246	750
15	1.40	5.35	5.7	14.8	54	228	436	4317
Δ%	60%	7%	32%	47%	1.8%	16%	102%	575%



CURRENT SHARING OF DEVICE 19/20 (2A/DIV, 5μs/DIV)

Note that 15 paralleled before with the much faster 14 showing extremely poor current sharing.

The 38 and 48 were paralleled to show an inductive load and the recovery current of diode. This is a realistic waveform found in many applications.

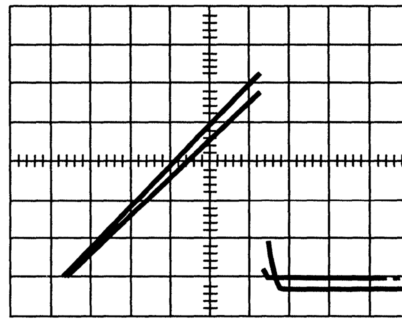
Here we paralleled two 20A IGT transistors. Also excellent current showing which is confirmed at the 500μs/div time scale in.

We paralleled the device 50 and 14 which have a relatively large delta 78% in fall time.

They can be operated in parallel and share much better than we might expect. The large deltas in fall time are the result of the relatively large delta at the current tail in comparison to the rest of the fall time.

TABLE 3.

NO.	$V_{CE(SAT)}$ 10A	$V_{G(TH)}$ 1A	G_{FS}	I	T_{DELAY} ON	T_R	T_{DELAY} OFF	T_F
14	2.25	5.75	4.3	9.2	53	264	246	750
15	2.15	4.95	4.3	10.4	46	252	269	871
Δ%	5%	16%	0%	13%			9.3%	16%



CURRENT SHARING OF DEVICE 14/20 (2A/DIV, 5μs/DIV)

Conclusion

All the conventional wisdom applied in the past to parallel bipolar type devices and MOSFET type devices can be applied to parallel operation of IGT Transistors.

1. $V_{CE(SAT)}$ voltage should be compared at rated current and should not exceed approximately 20% difference.
2. Gate threshold voltage which we measured and compared is important, but could be replaced by V_{GATE} vs I_C at rated current. Maximum differences should not exceed 10-20%.
3. Transconductance g_{FS} differences are not as critical as assumed and may be ignored.
4. $t_{D(ON)}$ and rise time are important for current sharing when switching resistive or inductive loads with reverse recovery currents at turn on, but tolerances are small, seldom posing a problem. Check FBSOA. Note that the fastest device takes most of the current. Emitter inductors can be inserted.
5. $t_{D(OFF)}$ and fall time show also small tolerances, but don't seem to pose a problem. Different device types and different manufacturers should never be paralleled. Note that the slowest device takes most of the current. Removal rate of gate voltage may become a factor. Emitter inductors less than 100μH show excellent results [3].
6. Circuit layout should be mechanically and electrically symmetrical. All lead length and differences in lead length become a factor (12-15nH/inch). Separate the gate circuit from the collector circuit (to avoid magnetic coupling).

7. Always use separate gate resistor to avoid oscillation. We did not see a problem of rated current but we have not made sufficient measurements to insure no problems.

8. Close thermal coupling is recommended (common heat-sink) resulting in only small differences in junction temperature.

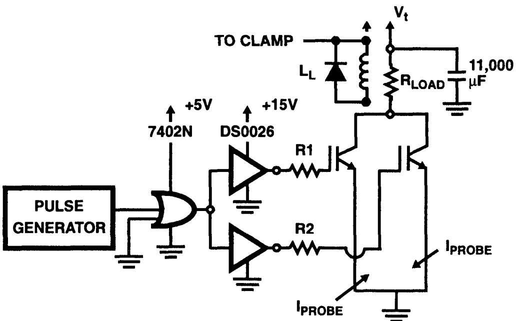


FIGURE 6. TEST CIRCUIT TO EVALUATE PARALLEL OPERATION OF IGT TRANSISTOR

The IGT's key parameters show relatively close distribution making it difficult to establish exact limits for parallel operation but following the above recommendations will give very good results. Additional measurements were made and in no instances did I exceed 2.5A.

IGT Transistors can be paralleled with a relatively small amount of difficulty. Some current derating may be advisable, which tends to improve current sharing. (We can see on the inductive switching waveform up to 6A sharing is almost perfect.)

In the future, switching modules rated at 100A and 200A or higher having blocking voltages of 500V or 1200V are realistic possibilities.

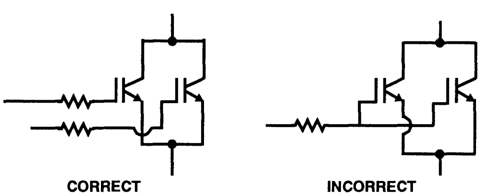


FIGURE 7. PROBLEM GATE CONNECTION

References

[1] SCR Manual, 6th Edition, General Electric Semiconductor Department, Auburn, New York, Chapter 6.2, Parallel Operation of SCR's.

[2] Use Equations to Parallel Transistors. Otto R. Buhler, IBM, Boulder, Colorado, Electronics Design 4, February 15,1977.

[3] Parallel Operations of Power Transistors in Switching Applications. Sebald R. Korn, General Electric Company, Application Note 660.39, 10/79.

[4] Paralleling Switching Bipolar Power Transistors, J. T. Hutchinson, PCIM, September 1985.

[5] Paralleling High Current Darlingtons, Warren Schulz, Motorola, Phoenix, Arizona, Powertechnics Magazine, December1985.

[6] Paralleling Power MOSFET's in Switching Applications, by Kim Gauen, Motorola, Application Note AN-918, 1984.

[7] Parallel Operation of MOSFET's in DC-DC Converters, Rudy Severns, Siliconix, Powertechnics Magazine, June 1985.

[8] A Chopper for Motor Speed Control Using Parallel Connected Power HEXFET's, by S. Clemente, B. Pelly, IR.

[9] MOS Power Applications Handbook, Siliconix, Inc., Chapter 5.3, Parallel Operation of Power MOSFET's (TA84-5).

[10] Motor Control Applications of Second Generation IGT Power Transistors, by Donald J. MacIntyre, Jr., Application Note 200.95.

[11] Non-destructive Forward Biased Second Breakdown Testing, No. 78-3, by Sebald Korn, Internal General Electric Report.

TABLE 4. RESULTS OF PARALLELING IGT TRANSISTORS

DEVICE NUMBER	$V_{CE(SAT)}$ AT V_{GE} = 14V 2A	5A	10A	GATE THRESHOLD 250µA	1A	TRANS-CONDUC-TANCE G_{FS}	RESISTIVE T_{DELAY} ON	T_R	INDUCTIVE T_{DELAY} OFF	T_F
TO-3 LOT 14353										
37	1.42V	1.82V	2.30	3.60V	5.50	4.3	51ns	230ns	23ns	390
38	1.54	2.05	2.70	3.70	5.75	4.2	53	253	230	427
42	1.4	1.78	2.25	3.75	5.60	5.4	45	223	226	421
44	1.42	1.82	2.35	3.50	5.38	4.3	51	225	250	402
47	1.50	1.98	2.60	3.75	5.75	4.2	58	238	226	422
48	1.49	1.94	2.55	3.50	5.50	3.8	51	236	230	381
50	1.45	1.87	2.40	3.62	5.60	4.4	58	232	240	389
Δ MAX			0.45		0.25	1.6				

DEVICE NUMBER	$V_{CE(SAT)}$ AT V_{GE} = 14V 2A	6A	10A	GATE THRESHOLD 250µA	1A	TRANS-CONDUC-TANCE G_{FS}	RESISTIVE T_{DELAY} ON	T_R	INDUCTIVE T_{DELAY} OFF	T_F
TO-3 LOT 14933.1 — IGT 6E11										
13	1.34	1.79	2.13	3.70	5.90	4.7	55	261	277	808
14	1.37	1.85	2.25	3.94	5.75	4.4	53	264	246	750
19	1.32	1.78	2.15	3.75	5.55	4.7	58	244	277	835
20	1.30	1.78	2.15	3.10	4.95	4.3	46	252	269	871
Δ			0.18		0.8	0.4				
TO-3 LOT (X) — IGT 6E10										
15	0.95	1.20	1.40	4.00	5.35	5.7	54	228	496	4317
16	0.96	1.21	1.42	3.95	5.30	5.7	58	227	515	4190

No. AN9320 June 1993

Parallel Operation Of Semiconductor Switches

Author: Sebald R. Korn, Consulting Applications Engineer

In uninterruptable power supplies demands for current handling capability to meet load current requirements plus margins for overload and reliability purposes often exceed the capability of the largest semiconductor device type considered and paralleling may become an attractive alternative. All switching power semiconductors starting with SCR's [1], bipolar transistors [2-4] darlingtons [5] and field effect transistors [6-10], have been successfully paralleled, but proper precaution had to be taken. We will review some of these methods, describe the characteristics of the insulated gate transistors, and show the proper methods to operate this relatively new family of devices in parallel.

All semiconductor circuits using parallel connected devices to switch a higher load current can easily be analyzed by using Kirchoff's law. As long as all voltage drops in the parallel branches are equal, the currents through the branches are equal.

This sounds sensible and logical, but as soon as we consider the different stages every switching device has to assume and we consider the parameters of each switching device which guarantees equal voltage drops in the branches over the required temperature range and over the duration of the switching cycle, complications begin to appear.

At first glance, each switching device has only two functional states, an "off- state" and an "on-state". But by closer examination, we have to consider how we get from "off" to "on" and back to "off", the "dynamic" area of the switching waveform (Figure 1). The dynamic area is only a fraction of the total waveform, but it is by far the most important when it comes to parallel operation.

In power electronics, there are three different load types; resistive, capacitive, and inductive. The resulting waveforms are sufficiently different to require either different switching devices or the circuit designer may have to change the switching circuit to meet the different requirements, especially when devices are operated in parallel.

Off-State

The off-state is probably the least demanding state in parallel operation of semiconductor devices. As long as leakage current is low, even differences of more than 100% would not create any difficulties.

On-State

The on-state is again a relatively uncritical and uneventful period (Figure 2). Most devices in switching applications are overdriven and differences in gain or transconductance do not translate into proportional output current.

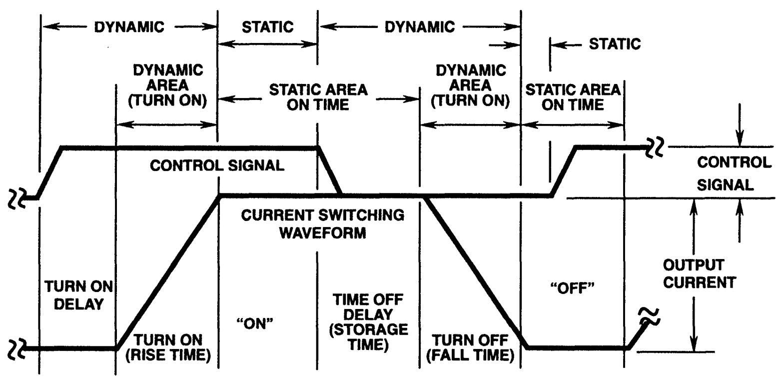


FIGURE 1. SWITCHING WAVEFORM DEFINITIONS

Even if a bipolar device takes a larger share of the total current, the rapid fall-off in gain and the increase in V_{SAT} as it takes the higher share will prevent disaster. Thermal runaway in bipolar applications is not as frequent as we may believe [2-4].

For bipolar devices, the parameter having a clear negative temperature coefficient is V_{BE}. $V_{CE(SAT)}$, on the other hand, can have positive or negative temperature coefficient depending on the device type (npn or pnp) and operating point.

The ease of paralleling of power FETs has been pointed out by many authors [6-9], and has been demonstrated in many applications, although each application requires analysis of both dynamic and static sharing.

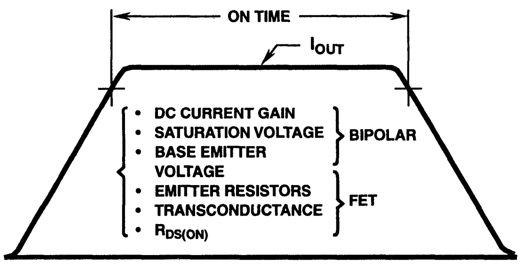


FIGURE 2. ON TIME OF SWITCHING WAVEFORM AND CONTROLLING PARAMETERS

Turn-On Delay Time

Turn-on delay time is the time from where the control signal is applied, reaches 10% amplitude, to the point where the switched current rises to the 10% amplitude (Figure 3).

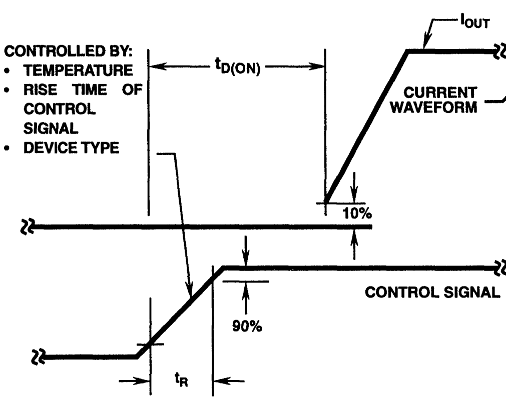


FIGURE 3. DEFINITION OF TURN-ON, DELAY TIME, $t_{D(ON)}$ AND CONTROLLING PARAMETERS

Fortunately, differences is turn-on delay are relatively small. Although this delay is significant in large-area SCR's, but it is much less a problem with bipolars or power FET's. It is less important when switching inductive loads, but should be monitored when devices to be paralleled switch resistive load, discharge capacitor or have to carry the recovery current of a diode.

Needless to say, it is desirable to have small turn-on delays for parallel operation. To reduce deltas in $t_{D(ON)}$, it is advisable to drive devices with fast rising control signals and use devices from the same mask design. The same device type number does not guarantee that they are made from the same mask design. Therefore, devices from different manufacturers should not be intermixed.

Rise Time

Rise time is an interesting part of the switching waveform (Figure 4). The device operates in an analog domain, although for a very short time, but nevertheless, analog.

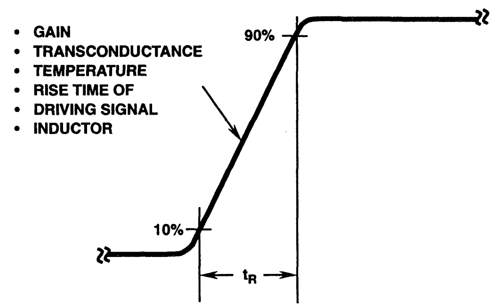


FIGURE 4. RISE TIME OF I_{OUT} WAVEFORMS AND PARAMETERS INFLUENCING IT

Again, transconductance and junction temperature become important considerations, but junction temperature differences as a result of rise time differences are relatively small. Inductors inserted into the emitter lead on bipolars, source lead on FET's or cathode lead on diodes, can be extremely effective [3]. All differences in turn-on delay and rise time become visible at thin part of the waveform. Differences which may exist, although small, require the evaluation of the forward biased safe operating area (FBSOA).

In most cases, transistors have almost rectangular FBSOA for the short durations they remain in the analog domain of the turn-on period. Problems seldom exist, but precautions should not be ignored either.

Note that the device with the shortest turn-on delay and the shortest rise-time will take most of the current. Most transistors have a negative temperature coefficient of input voltage and Miller effect feedback which can cause current begging if power dissipation is high during turn on.

Turn-Off Delay Time (Storage Time)

Turn-off delay time is the prelude to the most important part of the switching waveform, especially on bipolar devices (Figure 5). On bipolar devices, it is important to remove the stored charge as fast as possible, which may require more expensive drive circuitry. Especially on large power darlingtons, negative bias or baker clamps result in significant reduction of storage time and improve parallel operations.

The transition time of the base current signal from positive to negative (npn device) is important in the removal rate of the stored charge.

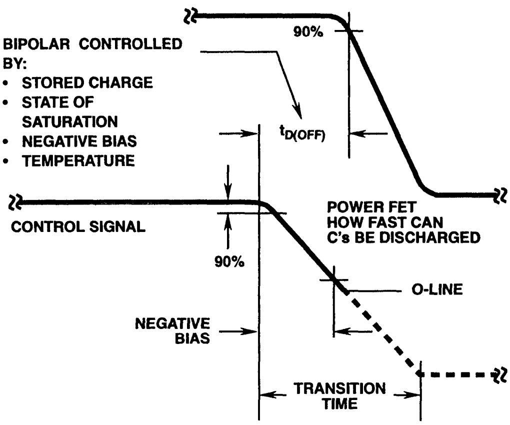


FIGURE 5. TURN-OFF WAVEFORM AND PARAMETERS INFLUENCING IT

Fall Time

Parameters which reduce storage time will also reduce fall time (Figure 6). For paralleled devices, differences in turn-off delay or storage time will have a noticeable effect on fall time.

When inductive loads are turned off, the reverse biased safe operating area (RBSOA) must be considered on bipolar devices. Hot spot formation [11] which results in sudden reduction of the V_{BE} and further increase in I_B could result in permanent damage.

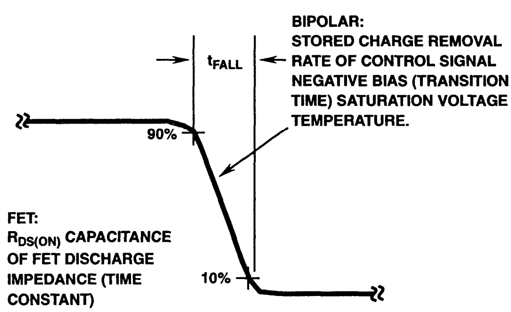


FIGURE 6. FALL TIME AND INFLUENCING PARAMETERS

The Insulated Gate Transistor

The insulated gate transistor (IGT) combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors, making it an ideal device for many power electronics switching control applications.

IGT Structure and Operation

The basic device structure is illustrated by the unit cell cross section of Figure 7. Like the MOSFET, the IGT consists of many individual cells connected in parallel. Processing of the IGT is similar to the vertical D-MOS technology used in MOSFETs. In the steady state, the n-channel IGT may be modeled as a bipolar pnp driven by an n-channel MOSFET. The MOSFET supplies base current to the pnp thus the MOSFETs gate voltage controls the total current.

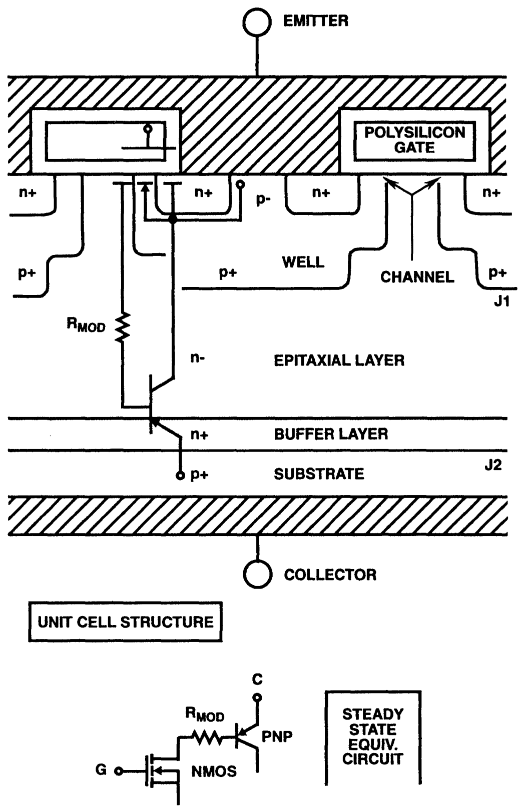


FIGURE 7. UNIT CELL CROSS SECTION AND STEADY STATE EQUIVALENT CIRCUIT OF IGT TRANSISTOR.

In normal operation, the emitter is grounded, the collector biased positive and with no gate-emitter voltage applied; J1 is reverse biased. The device is in the forward blocking mode. When a positive voltage is applied to the gate with respect to the emitter, an inversion channel is formed under the gate and MOSFET current flows from the n+ source region into the n-epi-layer to become the base current for the pnp. Junction J2 becomes forward biased and the device enters the conduction state. Holes are injected from the bottom percent region into the n-epi-layer. The injected minority carrier density is 100 to 1000 times higher that the doping level of the n-type epi-region. This conductivity modulation allows the IGT to operate at a forward conduction current density 20 times that of an equivalent MOSFET. It is primarily in the thick epi, high-voltage devices where conductivity modulation has its major impact to reduce on-resistance.

The typical output characteristics and the symbol of the IGT are shown in Figure 8. Like on MOSFETs, the output characteristics curves are generated by plotting collector emitter currents, collector emitter voltage. Unlike the MOSFET, there is an offset voltage generated by the collector emitter junction of the npn-transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSET.

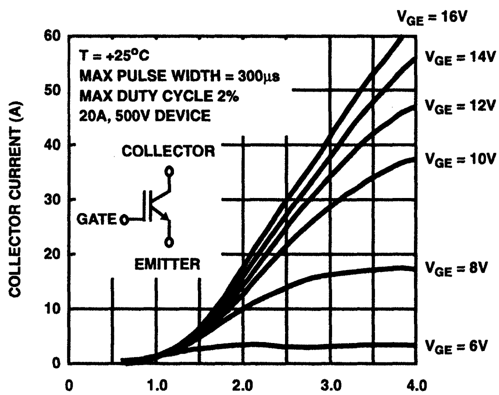


FIGURE 8. OUTPUT CHARACTERISTICS AND CIRCUIT SYMBOL FOR N-CHANNEL IGT TRANSISTOR

References

[1] SCR Manual, 6th Edition, General Electric Semiconductor Department, Auburn, New York, Chapter 6.2, Parallel Operation of SCR's.

[2] Use Equations to Parallel Transistors. Otto R. Buhler, IBM, Boulder, Colorado, Electronics Design 4, February 15,1977.

[3] Parallel Operations of Power Transistors in Switching Applications. Sebald R. Korn, General Electric Company, Application Note 660.39, 10/79.

[4] Paralleling Switching Bipolar Power Transistors, J. T. Hutchinson, PCIM, September 1985.

[5] Paralleling High Current Darlingtons, Warren Schulz, Motorola, Phoenix, Arizona, Powertechnics Magazine, December 1985.

[6] Paralleling Power MOSFET's in Switching Applications, by Kim Gauen, Motorola, Application Note AN-918, 1984.

[7] Parallel Operation of MOSFET's in DC-DC Converters, Rudy Severns, Siliconix, Powertechnics Magazine, June 1985.

[8] A Chopper for Motor Speed Control Using Parallel Connected Power HEXFET's™, by S. Clemente, B. Pelly, IR.

[9] MOS Power Applications Handbook, Siliconix, Inc., Chapter 5.3, Parallel Operation of Power MOSFET's (TA84-5).

[10] Motor Control Applications of Second Generation IGT™ Power Transistors, by Donald J MacIntyre, Jr., Application Note 200.95.

[11] Non-destructive Forward Biased Second Breakdown Testing, No. 78-3, by Sebald Korn, Internal General Electric Report.

Harris Semiconductor

APPNOTE

No. AN9408.2 November 1994

Harris Intelligent Power

The HIP2030 MCT/IGBT Gate Driver Provides Isolated Control Signals To Switch Power Devices

Author: J. K. Azotea

Introduction

Optically isolated gate drivers, that supply low level signal voltages to drive power switches, provide many technical advantages. These advantages are: high voltage isolation, low capacitive coupling, immunity to magnetic pickup, and the ability to remotely control gate drives without the effects of inductive lead length. The gate driver must also supply the required gate voltage and output current needed to slew a specified dv/dt across a given gate capacitance. The Harris HIP2030 MCT/IGBT Gate Driver, used with fiber-optic links or photo-couplers, provides an isolated gate drive that is ideal for switching MCT or IGBT devices in power circuits.

The Harris Fiber-Optic Isolated Gate Driver (HFOIGD) is designed to operate reliably at high isolation voltages, dv/dt's, and di/dt's. The HIP2030 provides a dual polarity voltage swing of ±15V while delivering peak output currents in excess of 6A. The HFOIGD circuitry is illustrated in Figure 1 and provides minimum driver chip functionality with an electronic part count of two IC's and seven discrete parts.The HFOIGD circuit is described in five subcircuits: a HIP2030 MCT/IGBT Driver Chip, a Single Supply DC Bias, a Regulated Voltage Divider Reference, a Fiber-Optic Receiver, and a Local Energy Source Capacitance.

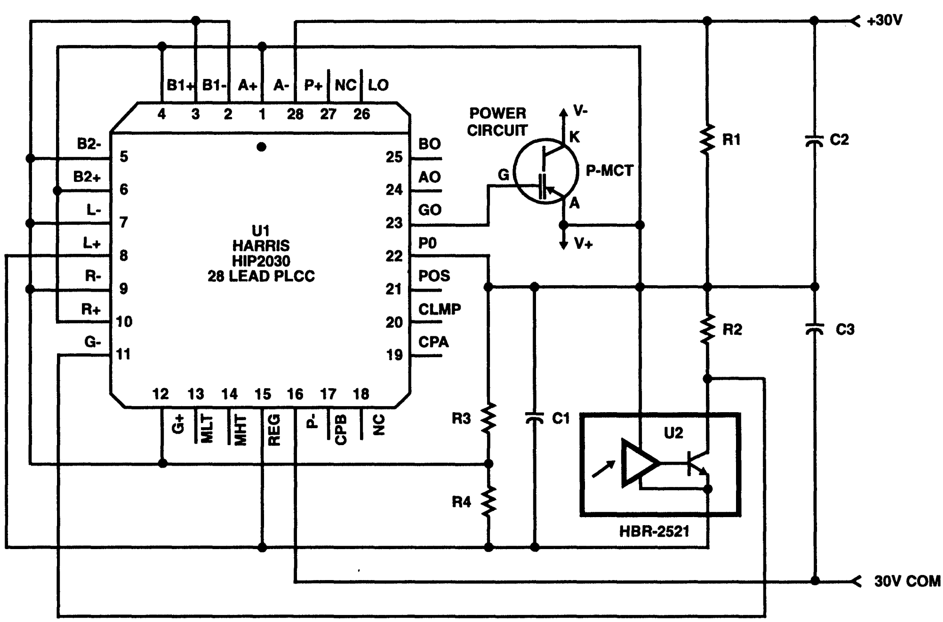


FIGURE 1. FIBER-OPTIC LINK ISOLATED MCT/IGBT GATE DRIVER

TABLE 1. G-CHANNEL OPERATION

CHANNEL	COMPARATOR INPUTS		OUTPUT
	+	-	
A	0V	2.5V	VP-
B1	2.5V	0V	VP0
B2	2.5V	0V	VP0
L	-2.5V	0V	No Latch
R	2.5V	0V	Reset
G	0V	2.5V	VP+

NOTES:

1. Midpoint Bias Voltage = 0V; High State = 2.5V; Low State = -2.5V.
2. High and Low state voltages are measured with respect to Midpoint bias of R3 and R4.

TABLE 2. LOGIC

INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

H = High
L = Low

LS = Last State
U = Undefined

The HIP2030 MCT/IGBT Driver Chip is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dv/dt's). This device is optimized for driving 60nF of MOS capacitance at $30V_{P-P}$ in less than 200ns. The architecture of the HIP2030 includes four comparator input channels, a 5V regulator, and a high side charge pump. The HIP2030 provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (A and B) that can be used as monitors (temperature sensing), indicators (LED's or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators. A functional block diagram for the HIP2030 is illustrated in Figure 2.

The HFOIGD, illustrated in Figure 1, is a dual polarity gate driver configured for G-Channel Operation (GCO). In GCO mode, the inputs of L and R channels are initialized to disable internal latch logic; which allows the G channel output (GO) to switch as a function of the G channel inputs (G+ and G-). The input voltages required for GCO are given in Table 1.

The driver chip can also be configured to control GO as a function of channel inputs L, R, and G. This mode of operation may be used to drive GO to an "OFF state" after sensing "Over Current levels" in a power circuit application. Table 2 lists the complete logic table for channels G, L, and R.

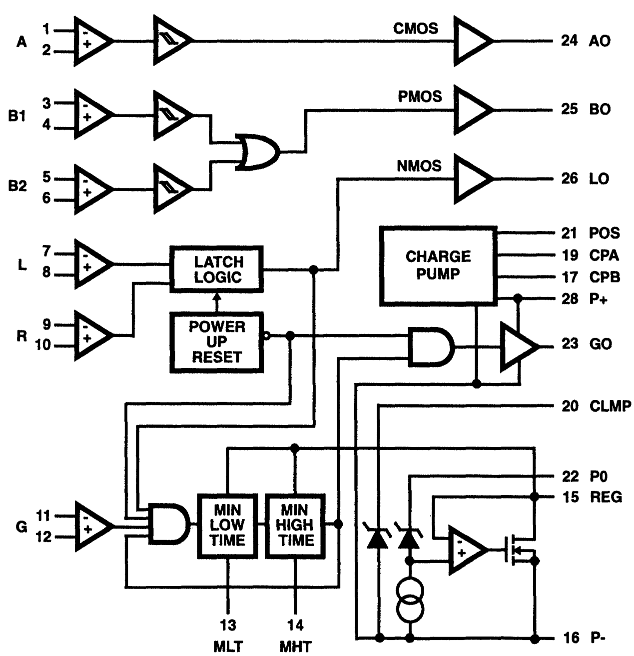


FIGURE 2. HIP2030 FUNCTIONAL BLOCK DIAGRAM

The Single Supply DC Bias Circuit, shown in Figure 1, consists of a single external dropping resistor (R1) connected between pins P+ (U1 - 27) and P0 (U1 - 22). When input voltage (V_{IN}) is applied across pins P+ and P- (U1 - 16), R1 forms a resistive divider network with the input impedance located between pins P0 and P- (R_{VP0}). This allows the circuit designer to adjust the value of R1 to obtain a desired bias voltage between Pins P0 and P- (V_{P0}). The value of R_{VP0} can be calculated by evaluating the equivalent Quiescent Input Impedance (R_Q) and 5V regulator impedance (R_R) as parallel resistances. The values for R1, R_Q, R_R, and R_{VP0} can be determined by using Equations 1, 2, 3, and 4 as shown in Appendix A, exercise 1.1.

The Regulated Voltage Divider Reference is comprised of two resistors (R3 and R4) connected in series and are located across pins P0 and REG. This voltage divider provides a stable voltage reference to all of the HIP2030 comparator inputs. Resistors R3 and R4 are selected equal in value to create a midpoint bias reference between the peak to peak input signal of U2. Also, the midpoint bias method ensures that input signals generated from U2 and midpoint bias reference voltages are within a safe common mode voltage range of the comparators.

The Fiber-Optic Receiver consists of components U2, R2, and C1. U2 is a fiber-optic receiver used to translate light pulses to low voltage input signals. U2 is used in combination with R2 to generate voltage levels from VP0 to V_{REG}. This signal is routed to the G- input of U2 and is used to control the output of GO. C1 is a despiking capacitor and prevents oscillations in the output of U2. C1 also serves as a noise rejection component for U2 and the HIP2030 5V regulator (U1 - 15).

The Local Energy Source Capacitances, C2 and C3, are needed to supply the charge required to drive large capacitance loads at high dv/dt's. The HFOIGD circuit uses low cost "oversized" tantilum capacitors (C = 10µF) for C2 and C3. If rise times and overshoot are critical, ceramic capacitors with low ESL and ESR will improve most gate drive signals. In a power circuit, where the gate driver is exposed to high dv/dt's, the network of C2 and C3 directs noise current away from the HIP2030. This allows the HFOIGD circuit to operate well in half bridge power circuits that use a transformer coupled power source.

The HFOIGD is an excellent choice for power switching applications that require a high isolation voltage and a low capacitive coupled gate signal. Power switching circuits, that operate at slower dv/dt's and require less isolation voltage, can use lower cost photo-coupled devices.

The Photo-Coupler Isolated Gate Driver (HPCIGD) circuitry, shown in Figure 3, provides a cost effective isolated gate driver with an electronic part count of two IC's and eleven discrete parts.

The basic HPCIGD circuit contains five subcircuits: HIP2030 MCT/IGBT Driver Chip, a single Supply DC bias, a regulated voltage divider reference, a local energy source, and a photo-coupled receiver. In this configuration, the input signal is sent through a Photo-coupler instead of a fiber-optic receiver.

The Photo-Coupled Receiver subcircuit consists of U2, R5, C4, and R6. U2 is a photo-coupler which combines an infrared emitter diode (IRED) and a high speed photo detector to translate light pulses to low voltage input signals. These signals are routed to the G channel and are used to control the output GO. Component R5 is used to limit the DC current through the IRED when the input signal voltage switches to its most positive level. A wide range of input voltages may be accommodated by varying R5 to limit the IRED current to 25mA. C4 is a speed up capacitor and is selected to match the forward bias capacitance of the IR diode. The last component, R6, is an optional part and is intended to be a termination resistor with the value set by the user.

The HPCIGD is an excellent choice for power switching applications that require less than 3000VDC isolation and dv/dt's less or equal to 10,000V/µs.

The Harris HIP2030 Evaluation Board (HIP2030EVAL) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030EVAL circuit enables the user to conveniently populate the PCB for either HPCIGD or HFOIGD circuitry. In addition, the PCB layout has provisions for "on board prototyping" and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030. The schematic of the HIP2030EVAL is illustrated in Figure 4.

HIP2030 Evaluation Board Application Information

Initial HIP2030EVAL Configuration

The HIP2030EVAL is populated with HPCIGD components and is configured as a dual polarity gate driver. To operate the driver board, the user must provide a damping resistor, an isolated DC bias voltage, and a control signal to the photo-coupler subcircuit. The schematic of the HIP2030EVAL shows the initial jumper and component configurations in Figure 4.

DC Input Power

The HIP2030EVAL is configured for 24V unregulated single supply DC bias operation. This bias scheme allows the HIP2030EVAL to operate reliably with a single isolated DC supply and will accept input bias voltages ranging from 24V to 30V. Dropping resistor R9 and an internal clamp (V_{CLMP}) are used in combination to provide a regulated 12VDC bias voltage for the HIP2030 logic circuitry. The DC voltage input connections, for this configuration, are applied to connector J2 between inputs P+ and P-.

Control Signal

HIP2030EVAL photo-coupler input can be driven with any signal generator that can supply a control signal with a pulse amplitude of 5V peak and provide 25mA of diode current. The input signal connections for the photo-coupled subcircuit, shown in Figure 4, are applied to connector J3 between inputs (+) and (-). The input signal requirements of the HIP2030EVAL are designed to be simple and allows the user to control the driver board with peripherals that contain either discrete logic or linear circuits.

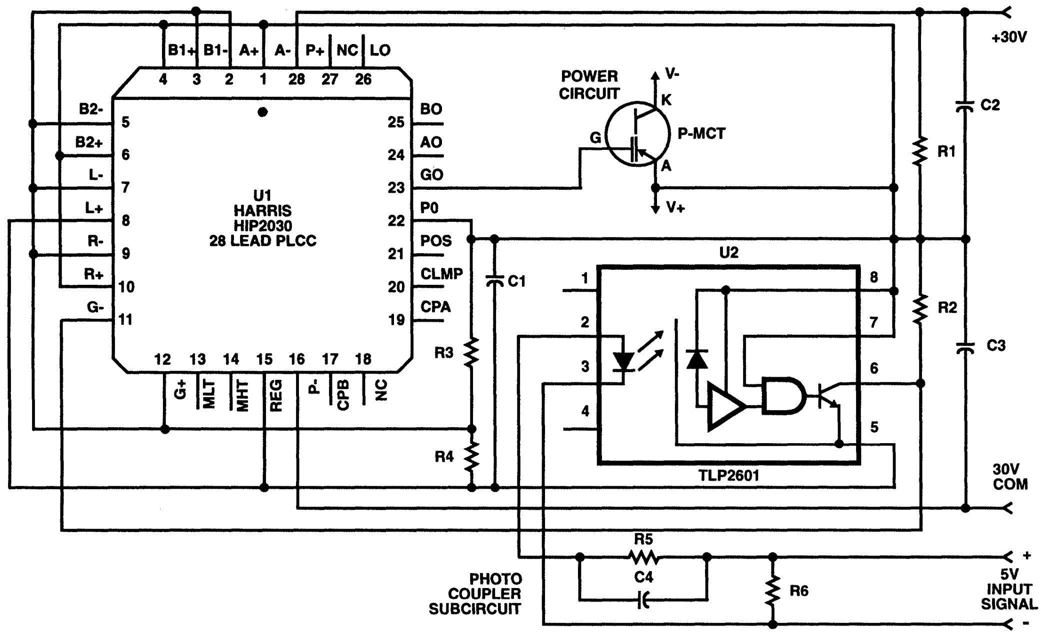


FIGURE 3. HARRIS PHOTO-COUPLER ISOLATED GATE DRIVE

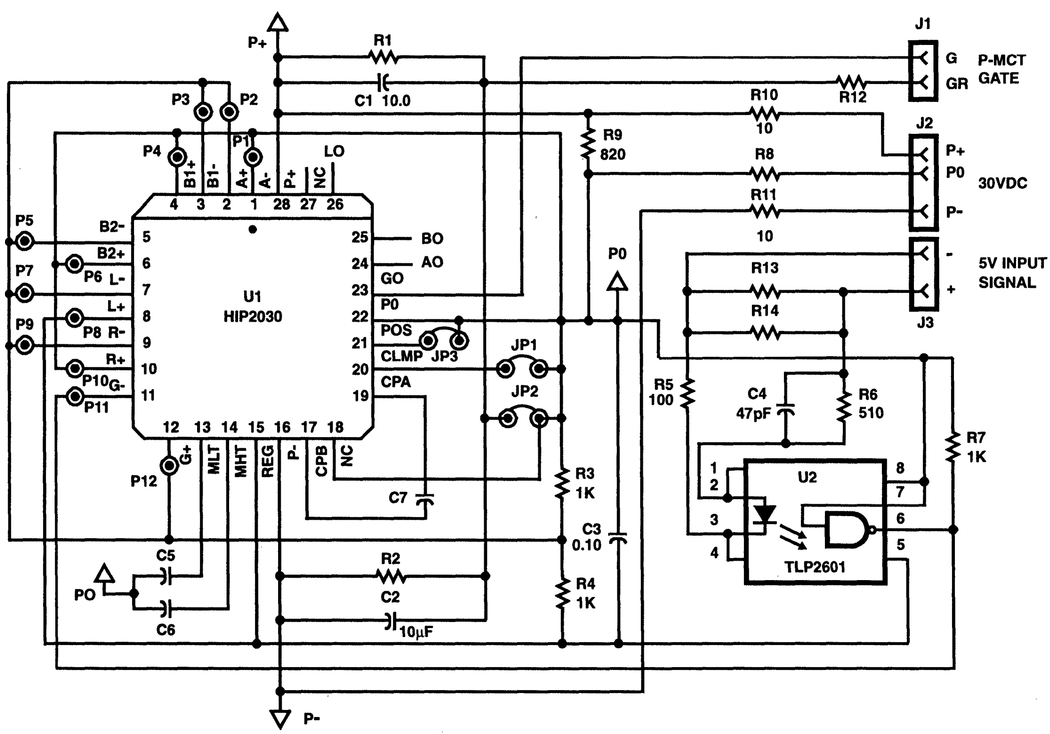


FIGURE 4. HIP2030 EVALUATION BOARD SCHEMATIC

Gate Output (GO)

The HIP2030EVAL is configured as a dual polarity gate driver with the gate return referenced to P0. In this mode of operation, the HIP2030 generates a negative 12V or a positive 18V output voltage when the input bias voltage equals 30V. The GO output connections, for -12V or +18V operation, are located at connector J1 between inputs G and GR.

Methods of DC Bias

The HIP2030EVAL can be biased in one of three configurations: a single supply (with a dropping resistor), a dual supply, and a single supply with a high side charge pump.

Single supply operation, using a dropping resistor (R9) and V_{CLMP}, uses one unregulated voltage supply which provides enough charging current to drive large capacitive loads at high frequencies. An example of this bias scheme is shown in Figure 4.

Dual supply biasing (DSB) is configured by adding one resistor and connecting two isolated power supplies. Follow steps 1 through 6 to use the DSB.

1. Apply voltage source #1 (V1) between P0 and P-.
2. Apply voltage source #2 (V2) between P+ and P0.
3. Install 10Ω resistor R8.
4. Remove dropping resistor (R9).
5. Adjust V1 to provide the desired negative gate drive voltage.
6. Adjust V2 to provide the desired positive gate drivevoltage.

NOTE: V1 is the DC bias voltage for the HIP2030's internal logic and must not fall below 8V at room temperature (+25°C).

The last DC bias method requires a single low voltage supply and utilizes a high side charge pump to provide the positive portion of the gate drive voltage. To use this configuration follow steps 1 through 5.

1. Install a 0.47μF capacitor for component C7.
2. Jumper pins POS and P0 to bias the charge pump circuitry (JP3 is initially shorted P0).
3. Install 10Ω resistor R8.
4. Remove dropping resistor (R9).
5. Provide a 12VDC bias voltage between P0 and P-.

Adjusting Gate Drive Output Polarity

The driver board is configured for driving a generic power switch and references the gate drive to P0; which is approximately half the voltage that is applied between P+ and P-. The HIP2030EVAL has provided the ability to adjust the gate drive output polarity to accommodate input voltage requirements for various power switches. Configurations for symmetric and asymmetric output polarities are given below:

Symmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference). Add R1 and R2 (select equal values of R1 and R2; typical values are between 1K and 10K).

Asymmetric Output Polarity

Open JP2 (configures the middle of the R1/R2 voltage divider for the gate return reference), select R2 with this equation:

$$R2 = \left[\frac{VR2\ R1}{(VP+) - VR2}\right]$$

Add R1 and R2 (typical values are between 1K and 10K).

Jumper Settings

Jumpers JP1, JP2, and JP3 are initially configured as shorts. Jumpers names and their functions are listed:

JP1 - Connect the internal 12V clamp, located inside the HIP2030, across P0 to P-.

JP2 - Use P0 for the gate return reference.

JP3 - Applies DC bias voltage to charge pump circuitry.

Minimum High and Low Time Functions

The HIP2030 provides two special functions that are unique to driving MCT power devices. These functions are called Minimum High Time (MHT) and Minimum Low Time (MLT). MLT and MHT are used to ensure that input control signals, with gate signals <1μs in duration, turn on and off the MCT devices reliability. The time settings for MHT and MLT are set as a function of MCT "ON" and "OFF" delay times. Both of these time settings can be independently programmed by installing a capacitor between its function pin (MHT and MLT) and pin P0. The value of either capacitor can be approximated by the equation:

$$C = \frac{(100\mu A)\ (\text{Delay Time})}{5V}$$

Monitor Channel Outputs

Channel outputs A, B, and L are accessed on the solder side of the HIP2030EVAL and are located above jumpers JP3 and JP4. The locations for AO, BO, LO, J1, and J3 are illustrated in the HIP2030 printed circuit board (PCB) assembly layer drawing.

On Board Prototyping Suggestions

The driver board includes a 1" x 0.6" prototyping area that provides 62 mil pads at a 100 mil spacing. Pads P1 through P12, located at the inputs of the voltage comparators, are used as access points to the channel inputs and may be jumpered over to the prototype areas. The pads are connected to the regulated voltage divider reference with 10mil traces and can be disconnected to prototype various circuits. These traces are easily cut with the use of an "exacto-knife".

Appendix A Exercises

Exercise 1.1

Q: How do I calculate the value of the series dropping resistor R1, shown in Figure 1?

A: The values for R1, R_Q, R_R, and R_{VP0} can be determined by using Equations 1, 2, 3, and 4.

$$R_Q = \frac{V_{P0}}{I_{QP0}} \quad \text{(EQ. 1)}$$

$$R_R = \frac{V_{P0}}{I_{OPTO} + I_{VDR} + I_{RP}} \quad \text{(EQ. 2)}$$

$$R_{VP0} = \frac{1}{\frac{1}{R_Q} + \frac{1}{R_R}} \quad \text{(EQ. 3)}$$

Where:
- V_{P0} = Voltage between pins P0 and P- (U1 - U22 and U1 - U16)
- I_{QP0} = Quiescent current flowing into pin P0.
- I_{QPTO} = Quiescent current of the HBR-2521 fiber-optic receiver.
- I_{VDR} = Current flowing through R3 and R4 (voltage divider reference).
- I_{RP} = Current flowing through pull up resistor R2 (in "ON" or "OFF" state)

The maximum value of R1 can easily be determined in four design steps:

1. Assume the following values:
   - V_{IN} = 30VDC
   - I_{QP0} = 2.75mA at V_{P0} = 15V
   - I_{OPTO} = 5mA
   - I_{VDR} = 2.5mA
   - $I_{RP(ON)}$ = 5mA, R2 = 1K, VR2 = 5V
2. Select a usable value of V_{P0} between 7V and 15VDC.

   Use V_{P0} = 15V
3. Solve for R_{VP0} using Equations 1, 2, and 3:

$$R_Q = \frac{15V}{2.75mA} = 5.45K$$

$$R_R = \frac{15V}{(5mA + 2.5mA + 5mA)} = 1.20K$$

$$R_{VP0} = \frac{1}{\frac{1}{5.45K} + \frac{1}{1.20K}} = 984$$

4. Solve for R1 using Equation 4:

$$R1 = \frac{R_{VP0}(V_{IN} - V_{P0})}{V_{P0}} \quad \text{(EQ. 4)}$$

$$R1 = \frac{984\,(30V - 15V)}{15V} = 984$$

For further information refer to the HIP2030, file number 3691; the HIP2030EVAL, file number 3918; and/or User's Guide, MOS Controlled Thyristor, DB307A.

Printed Circuit Board

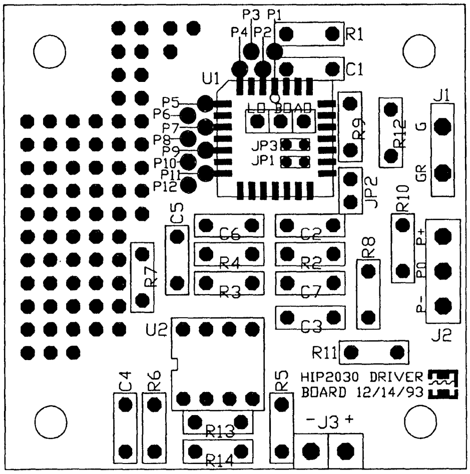


FIGURE 5A. HIP2030 ASSEMBLY LAYER

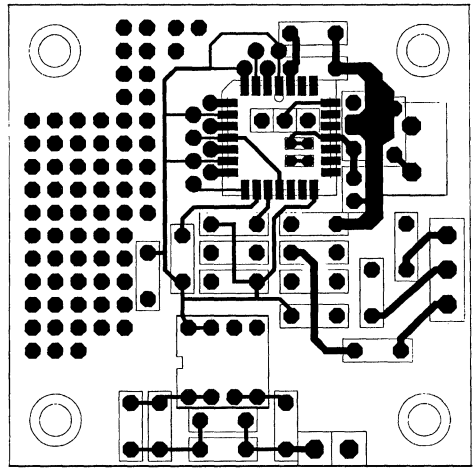


FIGURE 5B. HIP2030 BOTTOM LAYER

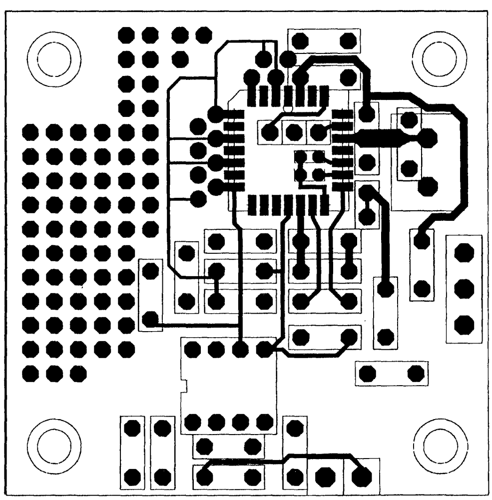


FIGURE 5C. HIP2030 TOP LAYER

HIP2030 Variable Duty Cycle Transformer Isolated Gate Driver Used In Controlling Power Devices

Author: J. K. Azotea

Introduction

Transformer coupling of low level voltages to control power devices has three main advantages: DC isolation, secondary voltages step up or step down ability, and variable output impedance. The conventional transformer switching methods are limited to AC signals; since the flux, in an ungappedcore, needs resetting every half cycle of the pulse period to prevent core saturation. Also, the primary of the transformer must maintain volt-second balance; meaning that the primary voltage times the seconds applied must equal negative primary voltage times the seconds applied. If the time of the reset pulse is short with respect to the on time pulse, for the same input voltage, a larger primary voltage will couple into the secondary.

Typically, each transformer has a distributed capacitance (C) from it's primary to secondary. When operating at high dv/dt's, the gate drive circuit is susceptible to noise currents (Cdv/dt). Although noise currents can be blocked with a bi-filer reactance, the cost of assembly, materials, and an increase in circuit volume deters the use of transformers in high voltage series device designs.

The object of this circuit design is to produce a low cost transformer-isolated gate drive, for power devices, which operates at both wide bandwidths of frequencies and variable duty cycles. This circuit must provide: DC isolation, reject Cdv/dt noise currents at high dv/dt's, require low input power, reduce ferrite core and circuit volume, and be suitable for mass production.

The Transformer-Isolated Variable Duty Cycle Gate Driver (TIVDGD) is a transformer isolated gate driver and is used to control power devices at variable duty cycles and frequencies. The TIVDGD shares all of the positive attributes of the conventional transformer coupling methods, but is designed to operate at variable duty cycles and a wide bandwidth of frequency. In particular, the small amount of volt-seconds required at the primary of the TIVDGD transformer allows a reduction in the following ferrite core parameters: maximum flux density (B), area of the core Acm2, and number of turns to support volt-seconds (N). The reduction in these parameters result in lower manufacturing cost in wire material, assembly time and B of core materials. Also, the total volume of the transformer can be reduced; making the TIVDGD a cost effective choice for compact power circuit designs. Distributed capacitance between the primary and secondary of the TIVDGD transformer is extremely low; which limits the magnitude of noise currents at high dv/dt's. In addition, low cost resistors are used to block all frequencies of Cdv/dt noise current and reduce the transformers input drive current requirements to 15mA at a primary voltage of 15V.

The TIVDGD circuitry is described in two circuit configurations: discrete ICs and using a single HIP2030 gate driver IC (using the HIP2030's internal comparators, latches, and power output MOSFETs).

Description

The TIVDGD circuitry is shown in Figure 1. It consists primarily of an isolation transformer, low power CMOS Operation Amplifier (OPAMP), Set/Reset Flip-Flop (RS Flip-Flop), MOSFETs, Resistors, and Capacitors. The circuit operation of the TIVDGD is described with four subsections: RL differentiator, polarity and level detector, latch and reset, and buffer stage.

The RL Differentiator consists of resistors R1, R2, and the primary inductance (L1) of voltage transformer T1. When a positive square wave (V_S) is applied to the input of R1 and R2, a differentiated voltage (V_{PRIM}) appears at the primary of T1 and is defined with Equation 1. This V_{PRIM} signal is coupled into the secondary windings (Vs) of T1 and is seen as a positive differentiated voltage at the input of IC1 (polarity and voltage level detector). If a negative square wave ($-V_S$) applied, the polarity of the voltage signal is reversed and is defined with Equation 2. Both positive and negative RL differentiated pulses are shown on Ch2 in Figure 3. The primary current (I_{PRIM}) of T1 is limited by Equation 3 which allows us to lower the power of our transformer drive requirements, prevent core saturation, and attenuate all frequencies of Cdv/dt current.

$$V_{PRIM} = V_S\left(e^{\frac{-Rt}{L}}\right) \quad \text{(EQ. 1)}$$

$$-V_{PRIM} = -V_S\left(e^{\frac{-Rt}{L}}\right) \quad \text{(EQ. 2)}$$

$$I_{PRIM} = \frac{V_{STEP}}{R1 + R2} \quad \text{(EQ. 3)}$$

The Voltage Polarity and Level Detector consists of R3, R4, R5, R6, C1, C2, and IC1 (CMOS OPAMP). The resistors R3, R4, R5, and R6 set the positive and negative voltage thresholds for IC1 and provides a referencing point for the secondary finish winding of T1. In Figure 1, R4 and R5 are biased for a ±5V threshold and initializes the inputs of IC2 to a logical 0 state. Components C2 and C3 are used to prevent Cdv/dt noise currents from instantaneously changing the threshold voltages. This subcircuit uses a voltage comparator (IC1) to detect the polarity and amplitude of differentiated pulses generated by T1 secondary. If a positive input signal exceeds the positive threshold voltage at the input of IC1, a two-bit binary word is generated at the output of IC2 that sets the Q output of IC2; which drives the noninverting buffer MCTDRV2 output to a high state voltage (10V across the DUT). If a negative input signal exceeds the negative threshold voltage at the input of IC1, a two bit binary word is generated at the output of IC2 that resets the Q output of IC2; which drives the noninverting buffer output to a low state voltage (-10V across the DUT).

The Latch and Reset subcircuit, shown in Figure 1, consists of IC2 (CMOS Flip-Flop), R7, and C4. IC2 is used as a 1-bit memory and allows the TIVDGD to operate at low frequencies and wide bandwidths (F_{MAX} - F_{MIN}). The upper and lower ranges of operating frequencies of the TIVDGD are shown in Equation 4 and Equation 5. Components R7 and C4 initializes the output pin of (IC2-Q) to a low state voltage; which drives the noninverting buffer output to a low state voltage (-10V across the DUT). To drive a N-type device into an on state, latching pin (IC2-Q) must be set to a high state voltage. To drive a N-type device into an off state, latching pin (IC2-Q) must be set to a low state voltage. A logic table to latch and rest IC2 is shown in Table 1.

$$F_{MAX} = \frac{0.1\,(R1 + R2)}{L1} \qquad \text{(EQ. 4)}$$

$$DC\left(F_{MIN}\right) \qquad \text{(EQ. 5)}$$

TABLE 1. IC2 LOGIC TABLE

SET	RESET	Q
0	1	0
1	0	1
1	1	0
0	0	Last State

The Buffer Stage, shown in Figure 1, consists of C5, C6, NFET, and PFET. C5 and C6 provide a local source of energy and deliver the peak current to slew voltage across the DUT gate capacitance. Since standard 4000 B-series CMOS chips are unable to provide sufficient current to drive the DUT capacitance, the noninverting buffer stage must be used.

In Figure 2, the TIVDGD is configured with the MCT Gate Driver II (MCTDRV2) and eleven discrete parts. The MCTDRV2 reduces IC and resistor count and has a rugged output buffer stage that supplies peak output currents of 6A or greater without the fear of shoot through current in the output stage. The MCTDRV2 contains the hardware logic features needed in the TIVDGD design; both circuits Figure 1 and Figure 2 contain comparators, an RS Flip-Flop, and Power Up reset.

In Figure 3, the variable duty cycle Vs signal (Ch2) crosses the ±thresholds of the MCTDRV2 (L+) and (R-) inputs; which forces the gate output pin GO to ±12V across the DUT gate capacitance (Ch1). Figure 4 shows a close up of V_{PRIM} (Ch2) and the L/R time constants that limit the maximum frequency of operation. Please note that in Figure 4 (Ch2), the threshold voltage was reached at the time L/R and is a 60ns delay time. Figure 4 (Ch1) shows a fast input signal V_{STEP} applied to the inputs of R1 and R2. Figure 5 shows the input to output delay times of the MCTDRV2. Variable duty cycle input voltage on Ch1 starts 240ns before the MCT output voltage changes from -10V to +10V. The current supplied from the buffer in this transition is shown in Equation 6. Figure 6 shows a delay time near 200ns, switching from ±10V, with the buffer sinking 3.6A.

$$I = 15nf\left(\frac{16V}{80ns}\right) = 3A \qquad \text{(EQ. 6)}$$

Reduction To Practice

We have established the following TIVDGD circuit concepts:

- We have demonstrated, in Figure 3, that a variable duty cycle input voltage (Ch1) can be coupled through a transformer and can generate a differentiated secondary voltage (Vs) that is uniform in amplitude and is independent of "volt-second balance."
- We have shown in Figure 5 and Figure 6, that a variable duty cycle input voltage (Ch1) controls the output of the MCTDRV2 (Ch2) while using all the required TIVDGD logic in the MCTDRV2.
- Finally we have demonstrated in Figure 4 (Ch2) that the transformer core, used in the TIVDGD circuit, needs to support a very low amount of volt-seconds with respect to the actual on or off voltages delivered to the gate drive. Equation 7 suggests that the product of volts times seconds is proportional to Equation 8 and that a significant reduction in one or all of these variables, especially at low frequency operation, is inevitable.

$$Vs = BAN \times 10^{-8} \qquad \text{(EQ. 7)}$$

Where:
Vs = Volt-Seconds, B = Flux Density,
A = Effective Core Area, N = Number of Turns

$$BAN \times 10^{-8} \qquad \text{(EQ. 8)}$$

Application Areas

The TIVDGD has many positive circuit attributes that allow for a wide array of applications in commercial gate drives for power devices. Some application areas of the TIVDGD circuitry are:

- Series Operation of Power Devices
- Inverters

The input circuitry in Figure 1 (R1, R2, T1) rejects Cdv/dt noise current that is usually a problem in series operation of power devices. When switching a string of series power devices, winding multiple secondaries on a pulse transformer is a good way to ensure that all series power devices are gated on at the same time.

DC isolated transformer designs with one primary input and four secondary outputs have the ability to drive power inverters. A transformer-isolated gate drive configuration, for a single-phase bridge inverter, is made with one primary input and four secondary outputs. Devices in the first half bridge will be driven with the secondary start windings. The second half bridge will be driven with the secondary finish windings. This allows the secondary outputs of the transformer to control each half bridge of the inverter with a common primary input voltage.

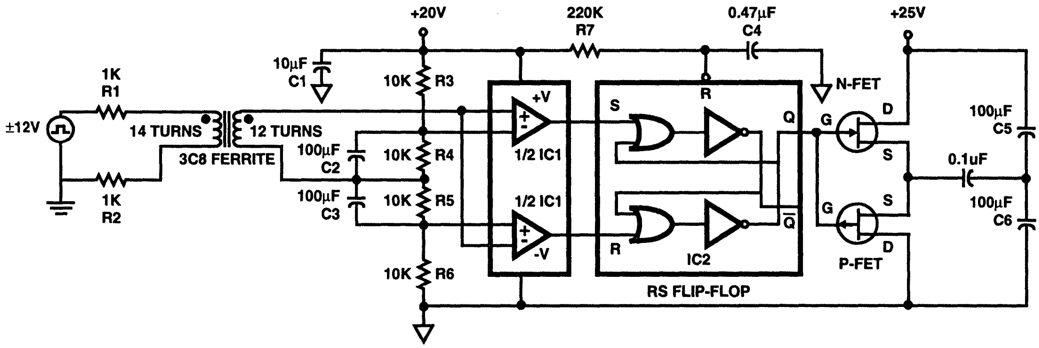


FIGURE 1. THE TIVDGD CIRCUITRY CONSISTS PRIMARILY OF AN ISOLATION TRANSFORMER, LOW POWER CMOS OPERATIONAL AMPLIFIER (OPAMP), SET/RESET FLIP-FLOP (RS FLIP-FLOP), MOSFETS, RESISTORS, AND CAPACITORS.

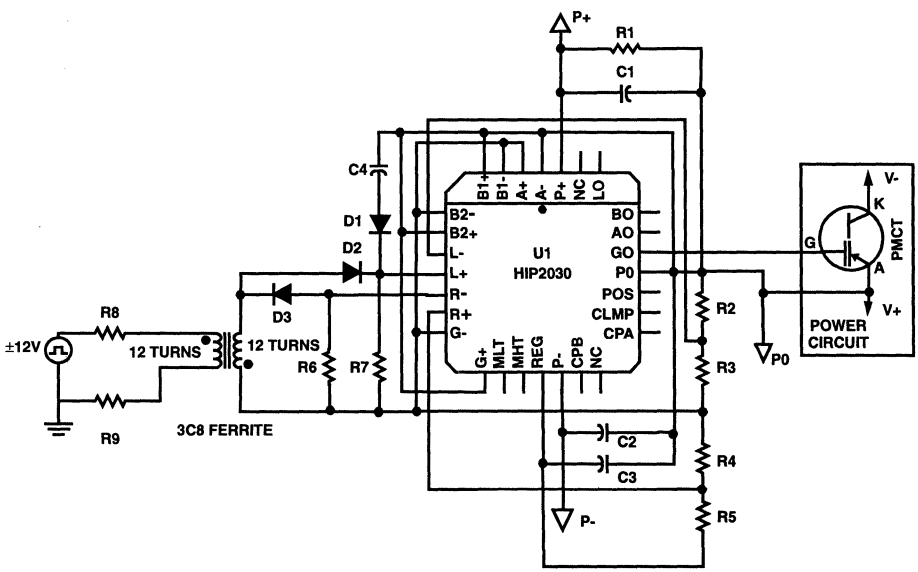


FIGURE 2. THE TIVDGD IS CONFIGURED WITH THE HIP2030 GATE DRIVER, 9 RESISTORS, 4 CAPACITORS, 3 DIODES AND A SMALL CORE POT TRANSFORMER. THE HIP2030 REDUCES IC AND RESISTOR COUNT AND HAS A RUGGED OUTPUT BUFFER STAGE THAT SUPPLIES PEAK OUTPUT CURRENTS OF 6A OR GREATER WITHOUT THE FEAR OF SHOOT THROUGH CURRENT IN THE OUTPUT STAGE.

Typical Performance Curves

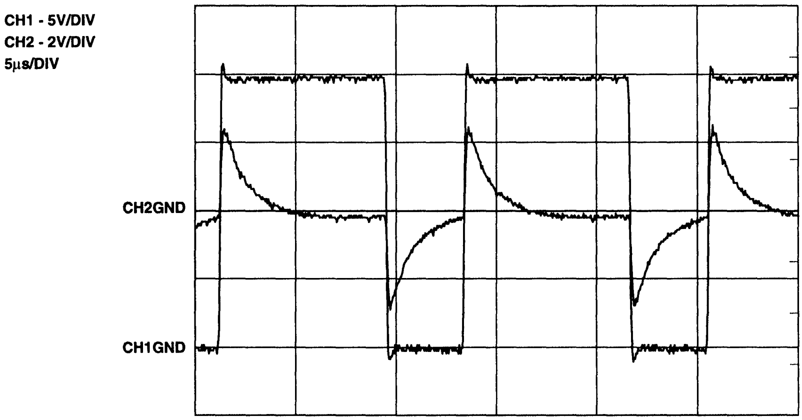


FIGURE 3. CH1 IS THE VARIABLE DUTY CYCLE INPUT VOLTAGE (VS) CH2 IS THE VOLTAGE AT L- AND R+ INPUTS OF THE HIP2030

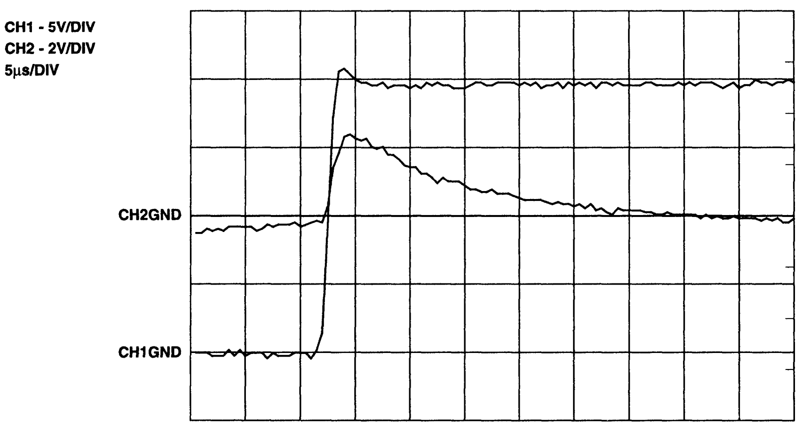


FIGURE 4 . CH2 SHOWS THE LOW AMOUNT OF VOLT-SECONDS THAT THE TRANSFORMER CORE (T1) NEEDS TO SUPPORT. CH1 DISPLAYS THE VOLT-SECONDS DELIVERED TO THE GATE DRIVER INPUTS.

MCT/IGBT/DIODES 11

HARRIS QUALITY AND RELIABILITY

Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for Power MOSFETs are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at Harris is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

Reliability Assurance

Harris Semiconductor has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability Program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development

During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design had been fine-tuned, multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB

Harris Semiconductor has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour +150°C bias life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI)

RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is performing product.

TABLE 1. TYPICAL MOSFET RTI TESTS

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	Plastic	10 - 15K Cycles
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	TO-3	20 - 50K Cycles
D-S Bias Life	T_A = +150°C 80% of Drain Source	All	168 Hours
G-S Bias Life	G - S = 16V T_A = +150°C	All	168 Hours

Requalification Program (RQP)

Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOSFET family to meet the original reliability design objectives. Table 2 is typical of the data generated for RQP.

TABLE 2. ACCELERATED POWER MOSFET TEST RELIABILITY SUMMARY

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated T_A = +150°C	500 Hours	300,000	0.33
All	Bias Life Gate-Source = 16V, T_A = +150°C	500 Hours	270,000	0.00
All	Operating Life T_A = +150°C, Free Air	500 Hours	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 Cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 Cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta T_J = +78°C PD = 56W (TO-3) or 2W (TO-39)	20,000 Cycles	5,480K	0.73
TO-220	Power Cycling Delta T_J = +135°C, PD = 4.75W	10,000 Cycles	1,850K	0.00
TO-220	Pressure Cooker	24 Hours	3,072	0.00

FAILURE RATE IN %/1000 HOURS AT 60% UCL			
TEST	T_A = +125°C	T_A = +90°C	T_A = +75°C
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on Nonfunctional performance in an operating mode, extrapolated from +150°C data using 1.0eV activation energy.

MCT/IGBT/DIODES 12

PACKAGING INFORMATION

PAGE

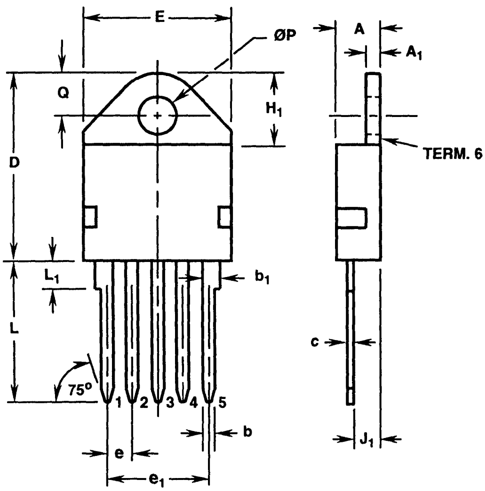
Handling Precautions for Insulated Gate Bipolar Transistors (IGBTs)

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "† ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.

† Trademark Emerson and Cumming, Inc.

Plastic Packages



MO-093AA

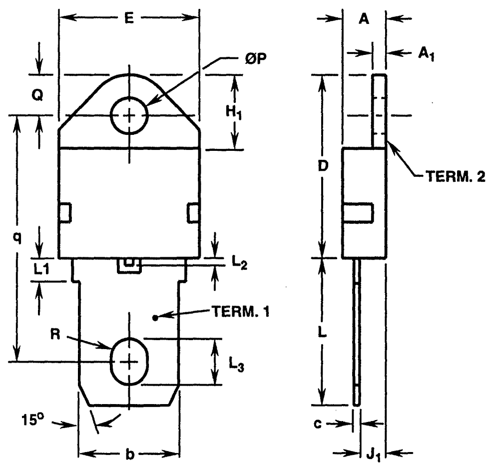
5 LEAD JEDEC MO-093AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.049	0.053	1.25	1.34	3, 4, 5
b_1	0.070	0.080	1.78	2.03	3, 4
c	0.018	0.022	0.46	0.55	3, 4, 5
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
e	0.110 TYP		2.80 TYP		7
e_1	0.438 BSC		11.12 BSC		7
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	8
L	0.575	0.600	14.61	15.24	-
L_1	-	0.130	-	3.30	3
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC MO-093AA outline dated 2-90.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Lead dimension and finish uncontrolled in L_1.
4. Lead dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder coating.
6. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
7. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
8. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
9. Controlling dimension: Inch.
10. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-218

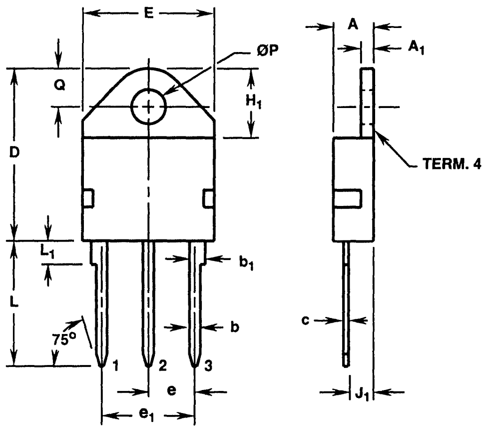
SINGLE LEAD JEDEC STYLE TO-218 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.433	0.443	11.00	11.25	-
c	0.018	0.022	0.46	0.55	-
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	4
L	0.635	0.655	16.13	16.63	-
L_1	-	0.130	-	3.30	-
L_2	-	0.034	-	0.86	-
L_3	0.195	0.205	4.96	5.20	-
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2
q	1.080	1.088	27.44	27.63	-
R	0.078	0.082	1.99	2.08	-

NOTES:

1. No current JEDEC outline for this package.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
4. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
5. Controlling dimension: Inch.
6. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-218AC

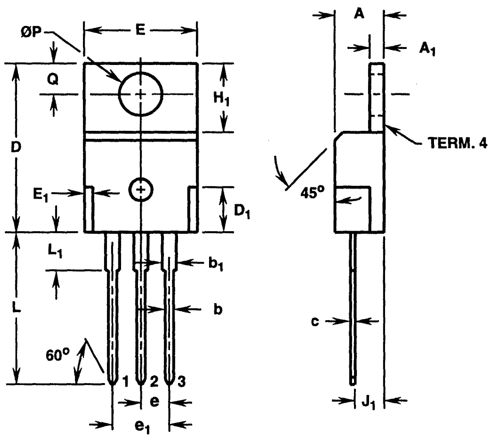
3 LEAD JEDEC TO-218AC PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.185	0.195	4.70	4.95	-
A_1	0.058	0.062	1.48	1.57	-
b	0.049	0.053	1.25	1.34	3, 4, 5
b_1	0.070	0.080	1.78	2.03	3, 4
c	0.018	0.022	0.46	0.55	3, 4, 5
D	0.800	0.820	20.32	20.82	-
E	0.615	0.625	15.63	15.87	2
e	0.219 TYP		5.56 TYP		7
e_1	0.438 BSC		11.12 BSC		7
H_1	-	0.330	-	8.38	-
J_1	0.115	0.125	2.93	3.17	8
L	0.575	0.600	14.61	15.24	-
L_1	-	0.130	-	3.30	3
ØP	0.159	0.163	4.04	4.14	-
Q	0.176	0.186	4.48	4.72	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. E of JEDEC TO-218AC outline dated 6-86.
2. Tab outline optional within boundaries of dimensions E and Q.
3. Lead dimension and finish uncontrolled in L_1.
4. Lead dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder coating.
6. Maximum radius of 0.050 inches (1.27mm) on all body edges and corners.
7. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
8. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
9. Controlling dimension: Inch.
10. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-220AB

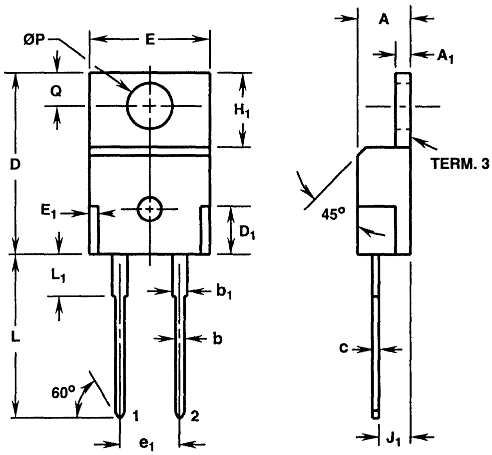
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-220AC

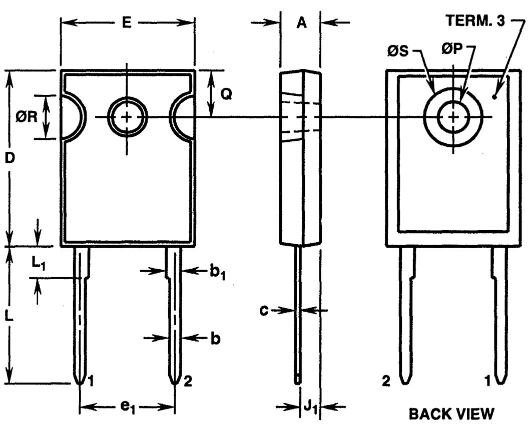
2 LEAD JEDEC TO-220AC PLASTIC PACKAGE (FOR RECTIFIERS ONLY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AC outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 12-93.

Plastic Packages (Continued)



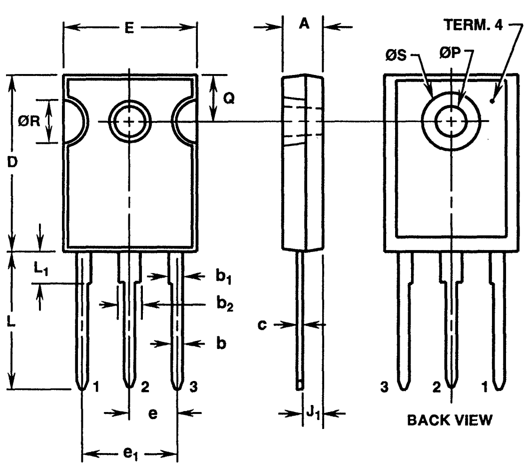
TO-247

2 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE (FOR RECTIFIERS ONLY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 2 dated 12-93.



TO-247

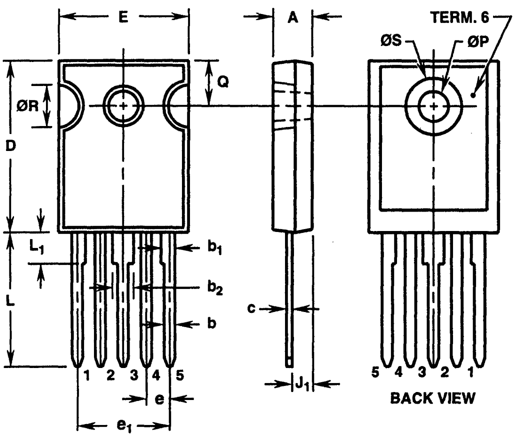
3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-247

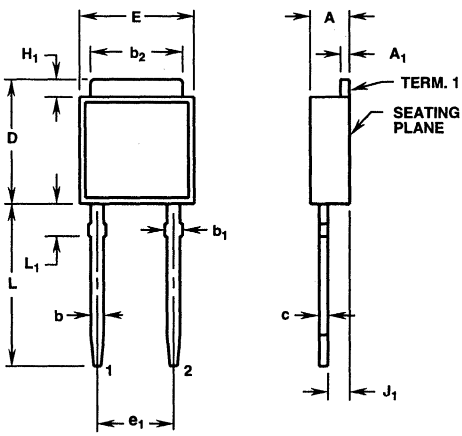
5 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.110 TYP		2.79 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages (Continued)



TO-251

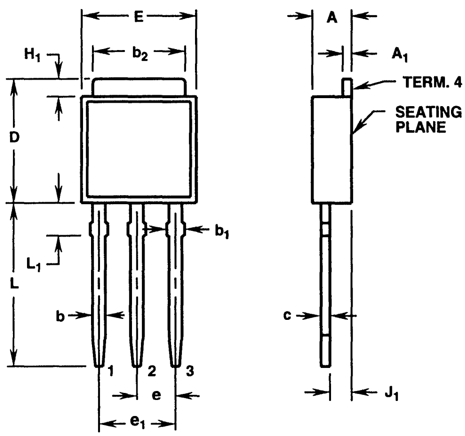
2 LEAD JEDEC STYLE TO-251 PLASTIC PACKAGE (FOR RECTIFIERS ONLY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. No current JEDEC outline for this package.
2. Solder finish uncontrolled.
3. Dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 6-93.

Plastic Packages (Continued)



TO-251AA

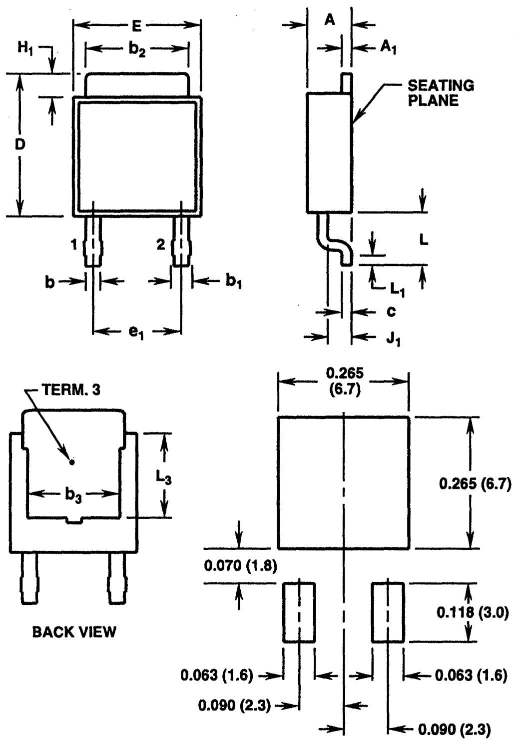
3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled.
3. Dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Plastic Packages (Continued)



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-252

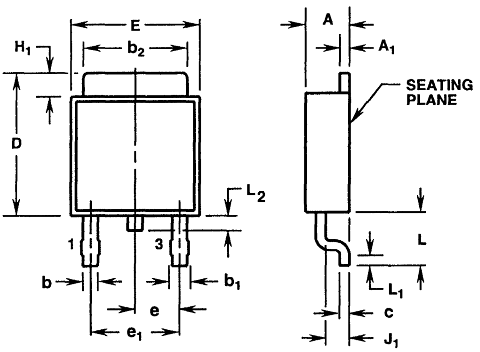
2 LEAD JEDEC STYLE TO-252 PLASTIC PACKAGE (FOR RECTIFIERS ONLY)

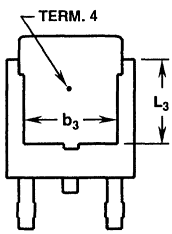
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_3	0.170	-	4.32	-	2

NOTES:

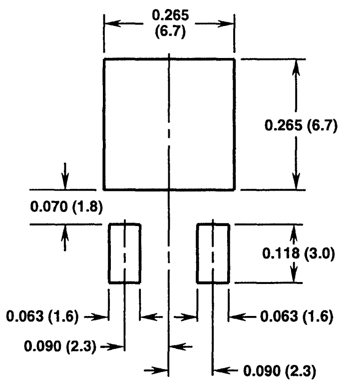
1. No current JEDEC outline for this package.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 3.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder coating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 2 dated 3-94.

Plastic Packages (Continued)





BACK VIEW



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-252AA

2 LEAD JEDEC TO-252AA PLASTIC PACKAGE

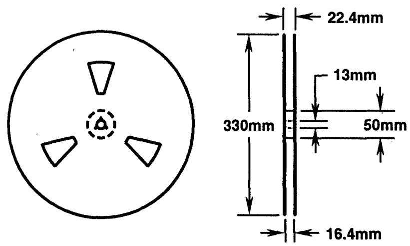
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	-
L_3	0.170	-	4.32	-	2

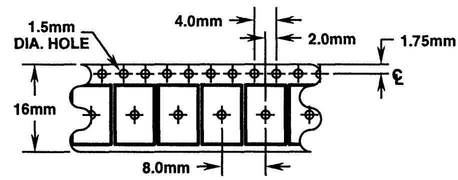
NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder coating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 4 dated 4-94.

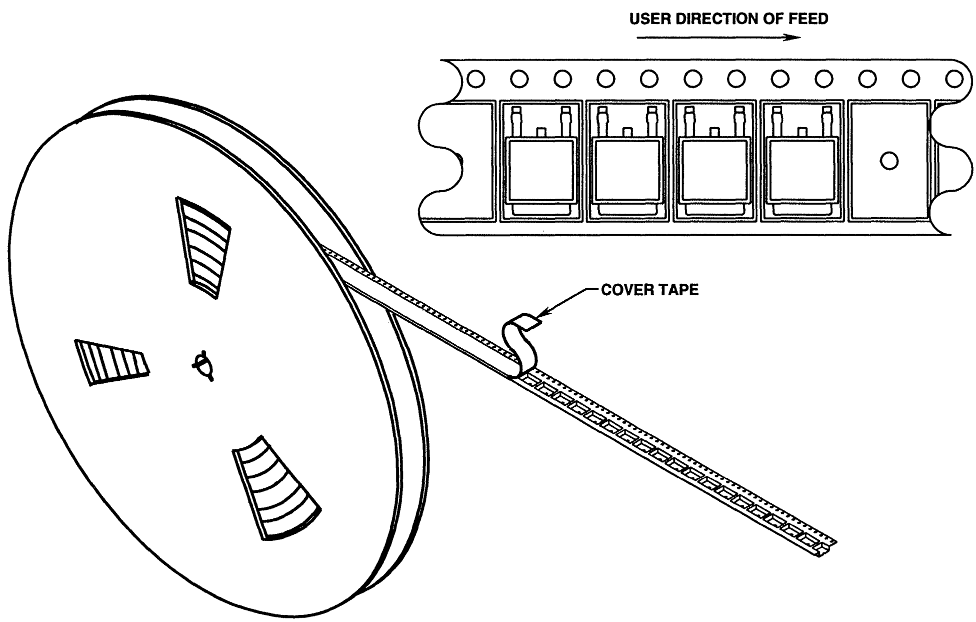
Plastic Packages (Continued)

TO-252AA
16mm TAPE AND REEL

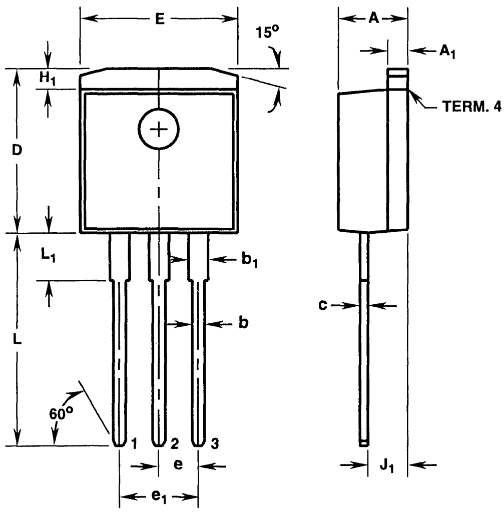




GENERAL INFORMATION
1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.



Plastic Packages (Continued)



TO-262AA

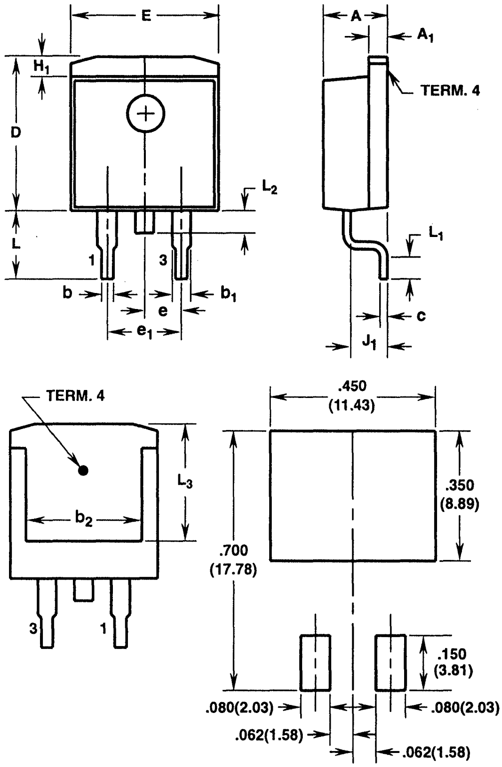
3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.018	0.022	0.46	0.55	2, 3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.0006 inches (0.015mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 2-95.

Plastic Packages (Continued)



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-263AB

2 LEAD JEDEC TO-263AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	-
L_3	0.315	-	8.01	-	2

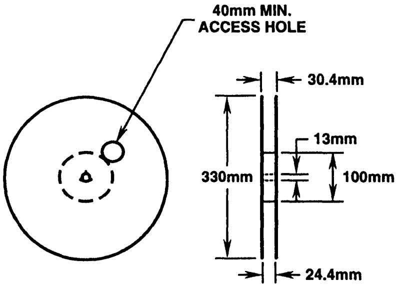
NOTES:

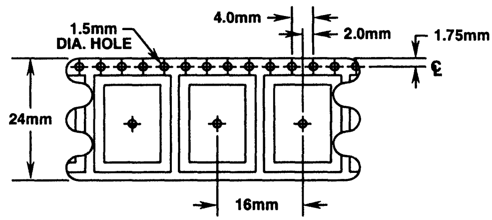
1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled.
4. Dimension (without solder).
5. Add typically 0.0006 inches (0.015mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 4-5-95.

Plastic Packages (Continued)

TO-263AB

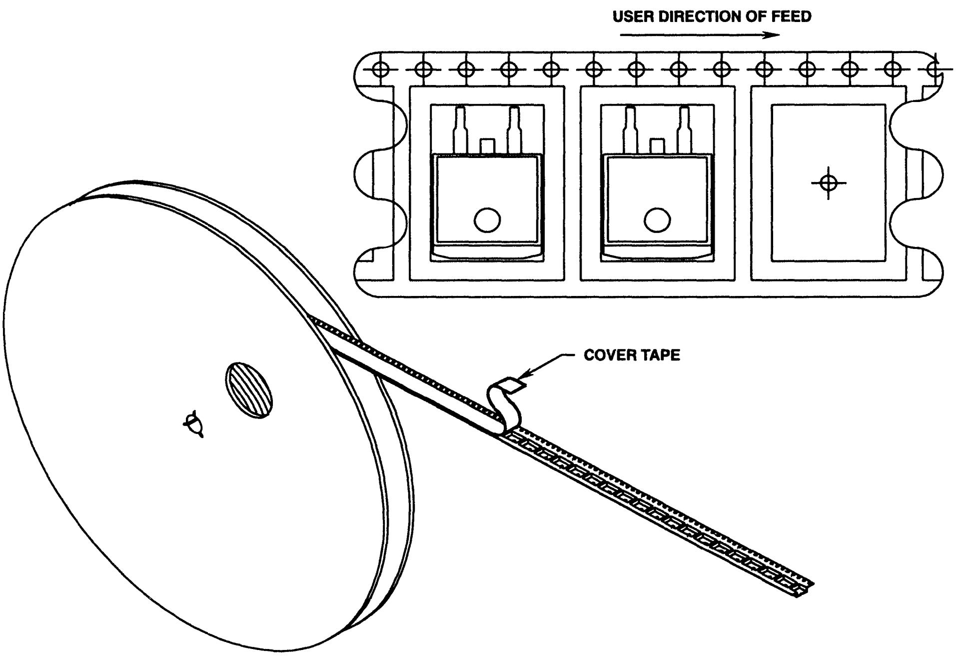
24mm TAPE AND REEL



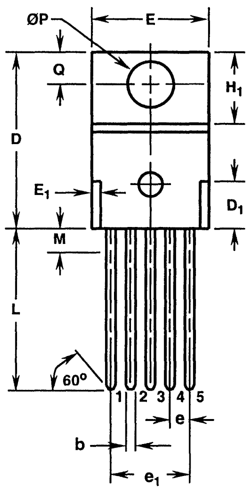


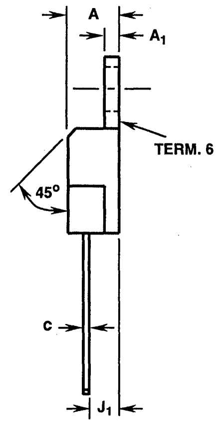
GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.



Plastic Packages (Continued)





TS-001AA

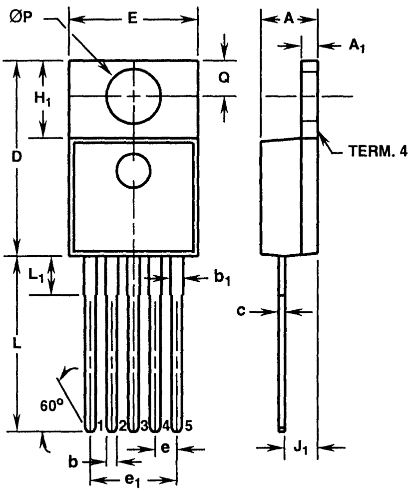
5 LEAD JEDEC TS-001AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.067 TYP		1.70 TYP		5
e_1	0.268 BSC		6.80 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
M	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TS-001AA outline dated 8-89.
2. Lead finish uncontrolled in zone M.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 3 dated 12-93.

Plastic Packages (Continued)



TS-001AA (ALTERNATE VERSION)
5 LEAD JEDEC TS-001AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	2, 3
b_1	0.031	0.041	0.79	1.04	2
c	0.018	0.022	0.46	0.55	2, 3
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.067 TYP		1.70 TYP		4
e_1	0.268 BSC		6.80 BSC		4
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	5
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	-
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TS-001AA outline dated 8-89.
2. Lead dimension (without solder).
3. Add typically 0.0006 inches (0.015mm) for solder plating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 12-20-94.

MCT/IGBT/DIODES 13

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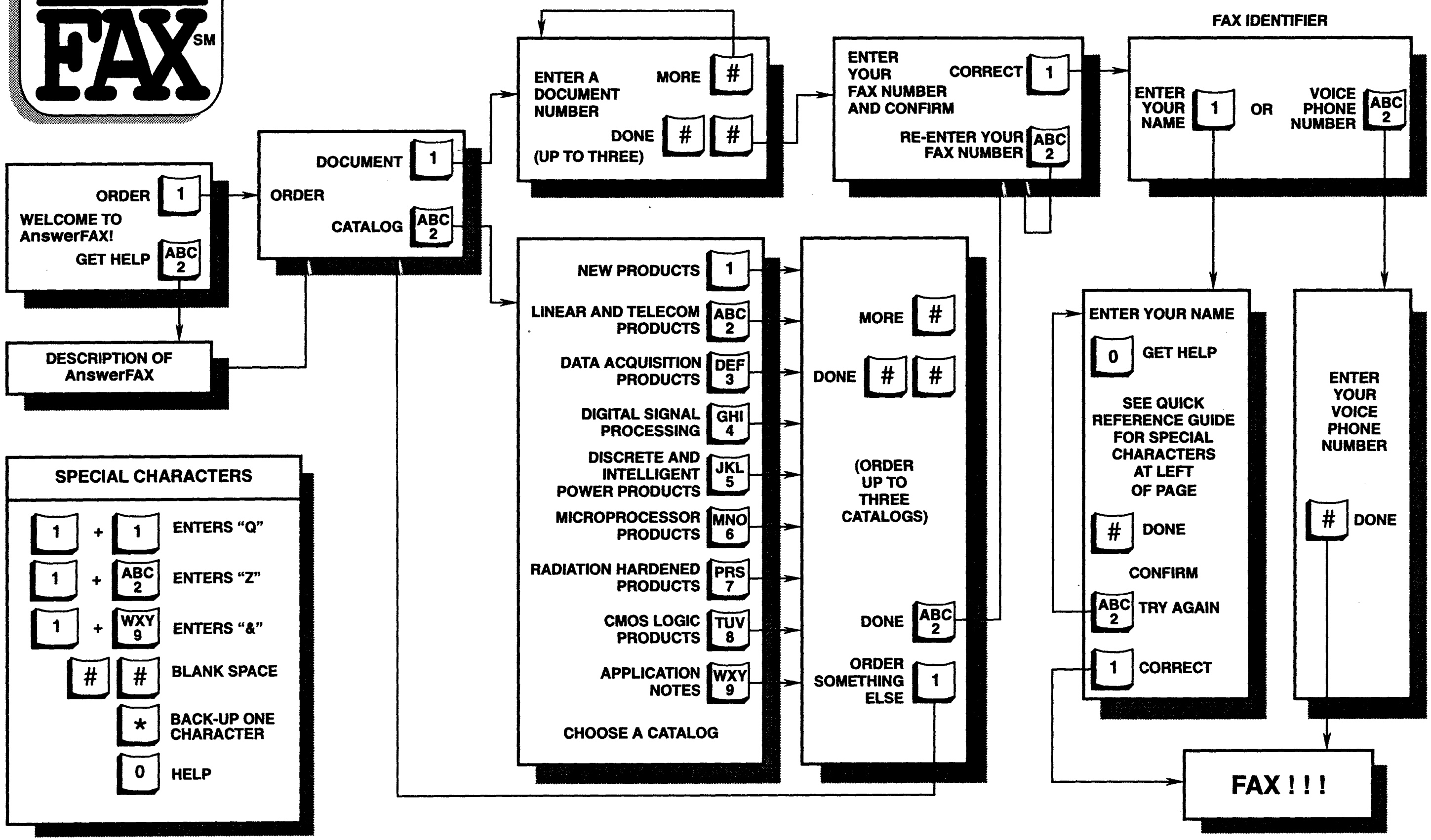

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	DB316	**POWER MOSFET DATABOOK SUPPLEMENT** (1996: 380pp) This databook contains the datasheets of recently introduced products and also updates some of the datasheets in the POWER MOSFET DATABOOK DB223B. These datasheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) Harris technologies used include dielectric isolation (DI), Silicon-on-Sapphire (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
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	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
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	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
	DB500B	**LINEAR AND TELECOM ICs** (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differential amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
	Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This data book describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 834pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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97254	AN7254	Switching Waveforms Of The L^2FET: A 5 Volt Gate-Drive Power MOSFET
97260	AN7260	Power MOSFET Switching Waveforms: A New Insight
97332	AN7332	The Application Of Conductivity-Modulated Field-Effect Transistors
98602	AN8602	The IGBTs - A New High Conductance MOS-Gated Device
98603	AN8603	Improved IGBTs with Fast Switching Speed And High-Current Capability
99318	AN9318	Insulated-Gate Transistors Simplify AC-Motor Speed Control
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99320	AN9320	Parallel Operation Of Semiconductor Switches
99408	AN9408	The HIP2030 MCT/IGBT Gate Driver Provides Isolated Control Signals To Switch Power Devices
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For more information, see the AnswerFAX map on page 13-2 and choose catalog item #5, "Discrete and Intelligent Power Products".

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North American Sales Offices, Representatives and Authorized Distributors June 3, 1996

ALABAMA

Harris Semiconductor
600 Boulevard South
Suite 103
Huntsville, AL 35802
TEL: (205) 883-2791
FAX: 205 883 2861

Giesting & Associates
Suite 15
4835 University Square
Huntsville, AL 35816
TEL: (205) 830-4554
FAX: 205 830 4699

Arrow/Schweber
Huntsville
TEL: (205) 837-6955

Hamilton Hallmark
Huntsville
TEL: (205) 837-8700

Wyle Electronics
Huntsville
TEL: (205) 830-1119

Zeus, An Arrow Company
Huntsville
TEL: (407) 333-3055
TEL: (800) 52-HI-REL

ARIZONA

Compass Mktg. & Sales, Inc.
11801 N. Tatum Blvd. #101
Phoenix, AZ 85028
TEL: (602) 996-0635
FAX: 602 996 0586

2480 W. Ruthrauff, Suite #140
Tucson, AZ 85705
TEL: (520) 292-0222
FAX: 520 292 1008

Alliance Electronics, Inc.
Scottsdale
TEL: (602) 483-9400

Arrow/Schweber
Tempe
TEL: (602) 431-0030

Hamilton Hallmark
Phoenix
TEL: (602) 437-1200

Wyle Electronics
Phoenix
TEL: (602) 804-7000

Zeus, An Arrow Company
Tempe
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

CALIFORNIA

Harris Semiconductor
* 1503 So. Coast Drive
Suite 320
Costa Mesa, CA 92626
TEL: (714) 433-0600
FAX: 714 433 0682

Harris Semiconductor
* 3031 Tisch Way
1 Plaza South
San Jose, CA 95128
TEL: (408) 985-7322
FAX: 408 985 7455

CK Associates
8333 Clairemont Mesa Blvd.
Suite 102
San Diego, CA 92111
TEL: (619) 279-0420
FAX: 619 279 7650

Ewing Foley, Inc.
185 Linden Avenue
Auburn, CA 95603
TEL: (916) 885-6591
FAX: 916 885 6594

10495 Bandley Avenue
Cupertino, CA 95014-1972
TEL: (408) 342-1220
FAX: 408 342 1221

Vision Technical Sales, Inc.
* 26010 Mureau Road
Suite 140
Calabasas, CA 91302
TEL: (818) 878-7955
FAX: 818 878 7965

Arrow/Schweber
Calabasas
TEL: (818) 880-9686

Fremont
TEL: (408) 432-7171

Irvine
TEL: (714) 587-0404

San Diego
TEL: (619) 565-4800

San Jose
TEL: (408) 441-9700

Hamilton Hallmark
Costa Mesa
TEL: (714) 789-4100

Los Angeles
TEL: (818) 594-0404

Sacramento
TEL: (916) 632-4500

San Diego
TEL: (619) 571-7540

San Jose
TEL: (408) 435-3500

Wyle Electronics
Los Angeles
TEL: (818) 880-9000

Irvine
TEL: (714) 789-9953

Sacramento
TEL: (916) 638-5282

San Diego
TEL: (619) 565-9171

Santa Clara
TEL: (408) 727-2500

Zeus, An Arrow Company
San Jose
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

Irvine
TEL: (714) 581-4622
TEL: (800) 52-HI-REL

CANADA

Blakewood Electronic Systems, Inc.
#201 - 7382 Winston Street
Burnaby, BC Canada V5A 2G9
TEL: (604) 444-3344
FAX: 604 444 3303

Clark Hurman Associates
Units #39, 40 & 41
16 Regan Road
Brampton, Ontario
Canada L7A 1C1
TEL: (905) 840-6066
FAX: 905 840-6091

308 Palladium Drive
Suite 200
Kanata, Ontario
Canada K2B 1A1
TEL: (613) 599-5626
FAX: 613 599 5707

78 Donegani, Suite 200
Pointe Claire, Quebec
Canada H9R 2V4
TEL: (514) 426-0453
FAX: 514 426 0455

Arrow/Schweber
Burnaby, British Columbia
TEL: (604) 421-2333

Dorval, Quebec
TEL: (514) 421-7411

Nepan, Ontario
TEL: (613) 226-6903

Mississagua, Ontario
TEL: (905) 670-7769

Farnell Electronic Services
Burnaby, British Columbia
TEL: (604) 606-8950

Calgary, Alberta
TEL: (403) 273-2780

Concord, Ontario
TEL: (416) 798-4884

Nepean, Ontario
TEL: (613) 596-6980

Pointe Claire, Quebec
TEL: (514) 697-8149

Winnipeg, Manitoba
TEL: (204) 786-2589

Hamilton Hallmark
Mississagua, Ontario
TEL: (905) 564-6060

Montreal
TEL: (514) 335-1000

Ottawa
TEL: (613) 226-1700

Vancouver, B.C.
TEL: (604) 420-4101

Toronto
TEL: (905) 564-6060

COLORADO

Compass Mktg. & Sales, Inc.
14142 Denver West Pkwy #200
Golden, CO 80401
TEL: (303) 277-0456
FAX: 303 277-0429

Arrow/Schweber
Englewood
TEL: (303) 799-0258

* Field Application Assistance Available

Hamilton Hallmark
Denver
TEL: (303) 790-1662

Colorado Springs
TEL: (719) 637-0055

Wyle Electronics
Denver
TEL: (303) 457-9953

Zeus, An Arrow Company
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

CONNECTICUT

Advanced Tech. Sales, Inc.
Westview Office Park
Bldg. 2, Suite 1C
850 N. Main Street Extension
Wallingford, CT 06492
TEL: (508) 664-0888
FAX: 203 284 8232

Alliance Electronics, Inc.
Milford
TEL: (203) 874-2001

Arrow/Schweber
Wallingford
TEL: (203) 265-7741

Hamilton Hallmark
Danbury
TEL: (203) 271-5700

Zeus, An Arrow Company
TEL: (914) 937-7400
TEL: (800) 52-HI-REL

FLORIDA

Harris Semiconductor
2401 Palm Bay Rd.
Palm Bay, FL 32905
TEL: (407) 729-4984
FAX: 407 729 5321

Harris Semiconductor
* 1025 W. Nasa Blvd. Bldg. F
Melbourne, FL 32919
TEL: (407) 729-4984
FAX: 407 729 3276

Sun Marketing Group
1956 Dairy Rd.
West Melbourne, FL 32904
TEL: (407) 723-0501
FAX: 407 723 3845

4175 East Bay Drive, Suite 128
Clearwater, FL 34624
TEL: (813) 536-5771
FAX: 813 536 6933

600 S. Federal Hwy., Suite 218
Deerfield Beach, FL 33441
TEL: (954) 429-1077
FAX: 954 429 0019

Arrow/Schweber
Deerfield Beach
TEL: (954) 429-8200

Lake Mary
TEL: (954) 333-9300

Hamilton Hallmark
Miami
TEL: (954) 484-5482

Orlando
TEL: (407) 657-3300

Largo
TEL: (813) 541-7440

Wyle Electronics
Fort Lauderdale
TEL: (954) 420-0500

St. Petersburg
TEL: (813) 576-3004

Zeus, An Arrow Company
Lake Mary
TEL: (407) 333-3055
TEL: (800) 52-HI-REL

GEORGIA

Giesting & Associates
* 2434 Hwy. 120, Suite 108
Duluth, GA 30136
TEL: (770) 476-0025
FAX: 770 476 2405

Arrow/Schweber
Duluth
TEL: (770) 497-1300

Hamilton Hallmark
Atlanta
TEL: (770) 623-4400

Wyle Electronics
Atlanta
TEL: (770) 441-9045

Zeus, An Arrow Company
TEL: (407) 333-3055
TEL: (800) 52-HI-REL

ILLINOIS

Harris Semiconductor
* 1101 Perimeter Dr., Suite 600
Schaumburg, IL 60173
TEL: (847) 240-3480
FAX: 847 619 1511

Oasis Sales
1101 Tonne Road
Elk Grove Village, IL 60007
TEL: (847) 640-1850
FAX: 847 640 9432

Arrow/Schweber
Itasca
TEL: (708) 250-0500

Hamilton Hallmark
Chicago
TEL: (847) 797-7300

Newark Electronics, Inc.
Chicago
TEL: (312) 907-5436

Wyle Electronics
Chicago
TEL: (708) 620-0969

Zeus, An Arrow Company
Itasca
TEL: (708) 250-0500
TEL: (800) 52-HI-REL

INDIANA

Harris Semiconductor
* 11590 N. Meridian St.
Suite 100
Carmel, IN 46032
TEL: (317) 843-5180
FAX: 317 843 5191

Giesting & Associates
370 Ridgepoint Dr.
Carmel, IN 46032
TEL: (317) 844-5222
FAX: 317 844 5861

Arrow/Schweber
Indianapolis
TEL: (317) 299-2071

EMC
Indianapolis
TEL: (317) 484-3050

Hamilton Hallmark
Carmel
TEL: (317) 575-3500

Zeus, An Arrow Company
TEL: (708) 250-0500
TEL: (800) 52-HI-REL

IOWA

Oasis Sales
4905 Lakeside Dr., NE
Suite 203
Cedar Rapids, IA 52402
TEL: (319) 377-8738
FAX: 319 377 8803

Arrow/Schweber
Cedar Rapids
TEL: (319) 395-7230

Hamilton Hallmark
Cedar Rapids
TEL: (319) 362-4757

Zeus, An Arrow Company
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

KANSAS

Advanced Tech. Sales, Inc.
2012 Prairie Circle Suite A
Olathe, KS 66062
TEL: (913) 782-8702
FAX: 913 782 8641

Arrow/Schweber
Lenexa
TEL: (913) 541-9542

Hamilton Hallmark
Kansas City
TEL: (913) 663-7900

Zeus, An Arrow Company
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

KENTUCKY

Giesting & Associates
339 Arrowhead Springs Lane
Versailles, KY 40383
TEL: (606) 873-2330
FAX: 606 873 6233

MARYLAND

New Era Sales, Inc.
890 Airport Pk. Rd, Suite 103
Glen Burnie, MD 21061
TEl: (410) 761-4100
FAX: 410 761-2981

Arrow/Schweber
Columbia
TEL: (301) 596-7800

Hamilton Hallmark
Columbia
TEL: (410) 720-3400

Wyle Electronics
Columbia
TEL: (410) 312-4844

Zeus, An Arrow Company
TEL: (914) 937-7400
TEL: (800) 52-HI-REL

MASSACHUSETTS

Harris Semiconductor
* Six New England Executive Pk.
Burlington, MA 01803
TEL: (617) 221-1850
FAX: 617 221 1866

Advanced Tech Sales, Inc.
348 Park Street, Suite 102
Park Place West
N. Reading, MA 01864
TEL: (508) 664-0888
FAX: 508 664 5503

Arrow/Schweber
Wilmington
TEL: (508) 658-0900

Gerber Electronics
Norwood
TEL: (617) 769-6000

Hamilton Hallmark
Peabody
TEL: (508) 532-9893

Wyle Electronics
Bedford
(617) 271-9953

Zeus, An Arrow Company
Wilmington, MA
TEL: (508) 658-4776
TEL: (800) HI-REL

MICHIGAN

Harris Semiconductor
* 27777 Franklin Rd., Suite 460
Southfield, MI 48034
TEL: (810) 746-0800
FAX: 810 746 0516

Giesting & Associates
34441 Eight Mile Rd., Suite 113
Livonia, MI 48152
TEL: (810) 478-8106
FAX: 810 477 6908

Arrow/Schweber
Livonia
TEL: (313) 462-2290

Hamilton Hallmark
Plymouth
TEL: (313) 416-5800

* Field Application Assistance Available

Zeus, An Arrow Company
TEL: (708) 250-0500
TEL: (800) 52-HI-REL

MINNESOTA

Oasis Sales
7805 Telegraph Road
Suite 210
Bloomington, MN 55438
TEL: (612) 941-1917
FAX: 612 941 5701

Hamilton Hallmark
Minneapolis
TEL: (612) 881-2600

Wyle Electronics
Minneapolis
TEL: (612) 853-2280

Zeus, An Arrow Company
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

MISSOURI

Advanced Tech. Sales
13755 St. Charles Rock Rd.
Bridgeton, MO 63044
TEL: (314) 291-5003
FAX: 314 291 7958

Arrow/Schweber
St. Louis
TEL: (314) 567-6888

Hamilton Hallmark
St. Louis
TEL: (314) 291-5350

Zeus, An Arrow Company
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

NEBRASKA

Advanced Tech. Sales, Inc.
601 North Mur-Len, Suite 8
Olathe, KS 66062
TEL: (913) 782-8702
FAX: 913 782 8641

NEW JERSEY

Harris Semiconductor
* Plaza 1000 at Main Street
Suite 104
Voorhees, NJ 08043
TEL: (609) 751-3425
FAX: 609 751 5911

Harris Semiconductor
724 Route 202
P.O. Box 591
Somerville, NJ 08876
TEL: (908) 685-6150
FAX: 908 685-6140

Tritek Sales, Inc.
One Mall Dr., Suite 410
Cherry Hill, NJ 08002
TEL: (609) 667-0200
FAX: 609 667 8741

Arrow/Schweber
Marlton
TEL: (609) 596-8000

Pinebrook
TEL: (201) 227-7880

Hamilton Hallmark
Cherry Hill
TEL: (609) 424-0110

Parsippany
TEL: (201) 515-1641

Pine Brook
TEL: (201) 882-8358

Zeus, An Arrow Company
TEL: (914) 937-7400
TEL: (800) 52-HI-REL

NEW MEXICO

Compass Mktg. & Sales, Inc.
4100 Osuna Rd., NE, Suite 109
Albuquerque, NM 87109
TEL: (505) 344-9990
FAX: 505 345 4848

Hamilton Hallmark
Albuquerque
TEL: (505) 293-5119

Zeus, An Arrow Company
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

NEW YORK

Harris Semiconductor
Hampton Business Center
1611 Rt. 9, Suite U3
Wappingers Falls, NY 12590
TEL: (914) 298-0413
FAX: 914 298 0425

Harris Semiconductor
* 490 Wheeler Rd, Suite 165B
Hauppauge, NY 11788-4365
TEL: (516) 342-0291 Analog
TEL: (516) 342-0292 Digital
FAX: 516 342 0295

Foster & Wager, Inc.
300 Main Street
Vestal, NY 13850
TEL: (607) 748-5963
FAX: 607 748 5965

2511 Browncroft Blvd.
Rochester, NY 14625
TEL: (716) 385-7744
FAX: 716 586 1359

7696 Mountain Ash
Liverpool, NY 13090
TEL: (315) 457-7954
FAX: 315 457 7076

Trionic Associates, Inc.
320 Northern Blvd.
Great Neck, NY 11021
TEL: (516) 466-2300
FAX: 516 466 2319

Alliance Electronics, Inc.
Huntington
TEL: (516) 673-1930

Arrow/Schweber
Farmingdale
TEL: (516) 293-6363

Hauppauge
TEL: (516) 231-1000

Melville
TEL: (516) 391-1276
TEL: (516) 391-1300
TEL: (516) 391-1633

Rochester
TEL: (716) 427-0300

Hamilton Hallmark
Long Island
TEL: (516) 737-0600

Hauppauge
TEL: (516) 434-7470

Rochester
TEL: (716) 272-2740

Wyle Electronics
Long Island
TEL: (516) 293-8446

Rochester
TEL: (716) 334-5970

Zeus, An Arrow Company
Pt. Chester
TEL: (914) 937-7400
TEL: (800) 52-HI-REL

NORTH CAROLINA

New Era Sales
1215 Jones Franklin Road
Suite 201
Raleigh, NC 27606
TEL: (919) 859-4400
FAX: 919 859 6167

Arrow/Schweber
Raleigh
TEL: (919) 876-3132

EMC
Charlotte
TEL: (704) 394-6195

Hamilton Hallmark
Raleigh
TEL: (919) 872-0712

Wyle Electronics
Raleigh
TEL: (919) 481-3737
TEL: 800-950-9953

Zeus, An Arrow Company
TEL: (407) 333-3055
TEL: (800) 52-HI-REL

OHIO

Giesting & Associates
P.O. Box 39398
2854 Blue Rock Rd.
Cincinnati, OH 45239
TEL: (513) 385-1105
FAX: 513 385 5069

6324 Tamworth Ct.
Columbus, OH 43017
TEL: (614) 792-5900
FAX: 614 792 6601

6200 SOM Center Rd.
Suite D-20
Solon, OH 44139
TEL: (216) 498-4644
FAX: 216 498 4554

Alliance Electronics, Inc.
Dayton
TEL: (513) 433-7700

Arrow/Schweber
Solon
TEL: (216) 248-3990

Centerville
TEL: (513) 435-5563

EMC
Columbus
TEL: (614) 299-4161

Cleveland
TEL: (216) 442-3441

Hamilton Hallmark
Cleveland
TEL: (216) 498-1100

Columbus
TEL: (614) 888-3313

Dayton
TEL: (513) 439-6735

Wyle Electronics
Cleveland
TEL: (216) 248-9996

Dayton
TEL: (513) 436-9935

Zeus, An Arrow Company
TEL: (708) 595-9730
TEL: (800) 52-HI-REL

OKLAHOMA

Nova Marketing
8421 East 61st Street, Suite P
Tulsa, OK 74133-1928
TEL: (800) 826-8557
TEL: (918) 660-5105
FAX: 918 357 1091

Arrow/Schweber
Tulsa
TEL: (918) 252-7537

Hamilton Hallmark
Tulsa
TEL: (918) 459-6000

Zeus, An Arrow Company
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

OREGON

Northwest Marketing Assoc.
4905 SW Griffith Drive Suite 106
Beaverton, OR 97005
TEL: (503) 644-4840
FAX: 503 644-9519

Almac/Arrow
Beaverton
TEL: (503) 629-8090

Hamilton Hallmark
Portland
TEL: (503) 526-6200

Wyle Electronics
Beaverton
TEL: (503) 643-7900

* Field Application Assistance Available

Zeus, An Arrow Company
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

PENNSYLVANIA

Giesting & Associates
471 Walnut Street
Pittsburgh, PA 15238
TEL: (412) 828-3553
FAX: 412 828 6160

Arrow/Schweber
Pittsburgh
TEL: (412) 856-9490

Hamilton Hallmark
Pittsburgh
TEL: (800) 332-8638

Wyle Electronics
Philladelphia
TEL: (609) 439-9110

Zeus, An Arrow Company
TEL: (914) 937-7400
TEL: (800) 52-HI-REL

TEXAS

Harris Semiconductor
* 17000 Dallas Parkway,
Suite 205
Dallas, TX 75248
TEL: (214) 733-0800
FAX: 214 733 0819

Nova Marketing
8310 Capitol of Texas Hwy.
Suite 180
Austin, TX 78731
TEL: (512) 343-2321
FAX: 512 343-2487

8350 Meadow Rd., Suite 174
Dallas, TX 75231
TEL: (214) 265-4600
FAX: 214 265 4668

Corporate Atrium II, Suite 140
10701 Corporate Dr.
Stafford, TX 77477
TEL: (713) 240-6082
FAX: 713 240 6094

Allied Electronics, Inc.
Ft. Worth
TEL: (800) 433-5700

Arrow/Schweber
Austin
TEL: (512) 835-4180
Dallas
TEL: (214) 380-6464
Houston
TEL: (713) 647-6868

Hamilton Hallmark
Austin
TEL: (512) 258-8848
Dallas
TEL: (214) 553-4300
Houston
TEL: (713) 781-6100

Wyle Electronics
Austin
TEL: (512) 345-8853
Dallas
TEL: (214) 235-9953
Houston
TEL: (713) 879-9953

Zeus, An Arrow Company
Carrollton
TEL: (214) 380-4330
TEL: (800) 52-HI-REL

UTAH

Compass Mktg. & Sales, Inc.
5 Triad Center, Suite 320
Salt Lake City, UT 84180
TEL: (801) 322-0391
FAX: 801 322-0392

Arrow/Schweber
Salt Lake City
TEL: (801) 973-6913

Hamilton Hallmark
Salt Lake City
TEL: (801) 266-2022

Wyle Electronics
Orem (Telesales)
TEL: (801) 226-0991
Salt Lake City
TEL: (801) 974-9953

Zeus, An Arrow Company
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

WASHINGTON

Northwest Marketing Assoc.
12835 Bel-Red Road
Suite 330N
Bellevue, WA 98005
TEL: (206) 455-5846
FAX: 206 451 1130

Almac/Arrow
Bellevue
TEL: (206) 643-9992

Hamilton Hallmark
Seattle
TEL: (206) 882-7000

Wyle Electronics
Seattle
TEL: (206) 881-1150

Zeus, An Arrow Company
TEL: (408) 629-4789
TEL: (800) 52-HI-REL

WISCONSIN

Oasis Sales
1305 N. Barker Rd.
Brookfield, WI 53005
TEL: (414) 782-6660
FAX: 414 782 7921

Arrow/Schweber
Brookfield
TEL: (414) 792-0150

Hamilton Hallmark
Milwaukee
TEL: (414) 780-7200

Wyle Electronics
Milwaukee
TEL: (414) 879-0434

Zeus, An Arrow Company
TEL: (708) 250-0500
TEL: (800) 52-HI-REL

Harris Semiconductor Chip Distributors

Chip Supply, Inc.
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
TEL: (407) 298-7100
FAX: (407) 290-0164

Elmo Semiconductor Corp.
7590 North Glenoaks Blvd.
Burbank, CA 91504-1052
TEL: (818) 768-7400
FAX: (818) 767-7038

Minco Technology Labs, Inc.
1805 Rutherford Lane
Austin, TX 78754
TEL: (512) 834-2022
FAX: (512) 837-6285

Puerto Rican Authorized Distributor

Hamilton Hallmark
El Senorail M/S Box 862
San Juan, PR 00926
TEL: (809) 760-1158
FAX: 809 754-4356

South American Authorized Distributor

Graftec Electronic Sales Inc.
One Boca Place, Suite 305 East
2255 Glades Road
Boca Raton, Florida 33431
TEL: (407) 994-0933
FAX: 407 994-5518

BRASIL

Graftec Brasil Ltda.
Rua Baronesa de Itu,
336 cj. 51/52 Sao Paulo - SP
CEP: 01231-000
TEL: 55-11-826-1666
FAX: 55-11-826-6526

North American Authorized Distributors and Corporate Offices

Hamilton Hallmark and Zeus are the only authorized North American distributors for stocking and sale of Harris Rad Hard Space products.

Alliance Electronics
(SAB Status)
7550 E. Redfield Rd.
Scottsdale, AZ 85260
TEL: (602) 483-9400
(800) 608-9494
FAX: (602) 443 3898

Allied Electronics
7410 Pebble Dr.
Ft. Worth, TX 76118
TEL: (800) 433-5700

Arrow/Schweber Electronics
25 Hub Dr.
Melville, NY 11747
TEL: (800) 777-2776

Electronics Marketing Corporation (EMC)
1150 West Third Avenue
Columbus, OH 43212
TEL: (614) 299-4161
FAX: 614 299 4121

Farnell Electronic Services
300 North Rivermede Rd.
Concord, Ontario
Canada L4K 3N6
TEL: (416) 798-4884
FAX: 416 798 4889

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
TEL: (617) 769-6000, x156
FAX: 617 762 8931

Hamilton Hallmark
10950 W. Washington Blvd.
Culver City, CA 90230
TEL: (800) 332-8638

Newark Electronics
4801 N. Ravenswood
Chicago, IL 60640
TEL: (312) 784-5100
(800) 367-3673
FAX: 312 275-9596

Wyle Electronics
(Commercial Products)
3000 Bowers Avenue
Santa Clara, CA 95051
TEL: (800) 414-4144
FAX: 801 226-0210

Zeus Electronics, An Arrow Company
100 Midland Avenue
Pt. Chester, NY 10573
TEL: (800) 524-4735

Obsolete Products:

Rochester Electronics
10 Malcom Hoyt Drive
Newburyport, MA 01950
TEL: (508) 462-9332
FAX: 508 462 9512

* Field Application Assistance Available

European Sales Offices, Representatives and Authorized Distributors

European Sales Headquarters

Harris Semiconductor
Mercure Center
Rue de la Fusee 100
B-1130 Brussels, Belgium
TEL: 32 2 724 21 11
FAX: 32 2 724 2205/...09

AUSTRIA

Avnet E2000
Waidhausenstrasse 19
A - 1140 Wien
TEL: 43 1 9112847
FAX: 43 1 9113853

EBV Elektronik
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